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SEU Performance Enhancement in BPJLT Devices by Channel Doping and Film Thickness

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Abstract*: The bulk planar junctionless transistor (BPJLT) is a potential candidate for future CMOS technologies due to its CMOS compatibility and scalability. In this paper, the impact of silicon film thickness and channel doping on single-event upset (SEU) radiation performance of BPJLT based SRAMs is studied using TCAD simulations. The simulation results show that BPJLT devices having higher channel doping and smaller film thickness provides the better SEU performance.

***Keywords* : BPJLT, SRAM, Threshold LET, SEU, TCAD.**

I. INTRODUCTION

Since its introduction in 2010, various structures of Junctionless transistors (JLTs) have been explored in the literature [1-8]. Among these structures, single gate bulk planar JLT (BPJLT) is the most attractive structure because of the CMOS process compatibility and reduced fabrication costs. SOI based JLT devices can also be considered for planar structures but a film thickness of 5 nm or below is needed, for a work function of 5.5 eV at 20 nm channel length. The BPJLT devices relax this tight constraint on film thickness due to their P-N junction present between the film/epi/channel and substrate. So it's becoming a popular technology to replace the existing CMOS technologies.

BPJLT device is a single-gate device with the same type of doping throughout the entire active silicon layer, including source, channel and drain regions. It has no junctions along the channel direction, but it has junctions in the vertical direction for isolation purposes. It leads to the two additional control parameters (substrate bias (V_{sub}) and substrate doping (N_{sub})) for tuning the device performance. These two control parameters define the effective thickness of the device layer. For example, the BPJLT with 10 nm device layer thickness has an effective device layer thickness of about 5 nm since the bottom 5 nm device layer is depleted by the built-in junction potential in the vertical junction.

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So the device layer can be controlled effectively [9]. Soft errors, one of the problems due to single event effects (SEE) have been a most important reliability concern in the technological advancement of memories, especially SRAMs, in radiation prone environments. The sensitivity of SRAMs to radiation has gone up with CMOS scaling [10].

Several studies on soft error performance of various JLT devices are available in the literature [11-14]. All these studies are done only in SOI based JLT devices. Only few studies are reported in bulk JLT devices in comparison with SOI JLT devices [15, 16]. In this work, we explore the SEU performance of the bulk planar junctionless devices with various channel doping (N_{ch}) and silicon film thickness (T_{Si}). The paper is organized as follows: section 2 provides the device structure and calibration, section 3 provides the simulation results and discussions. Finally, section 4 gives the conclusion.

II. DEVICE STRUCTURE AND CALIBRATION

Sentaurus TCAD simulator from Synopsys is used in this study [17]. Fig. 1 shows the structure of BPJLT device generated from SDE. The device parameters used in this study are given in Table I. The models used in the device simulation include SRH and Auger recombination models, mobility model with doping and field dependence. Quantum corrections are also taken into account. This BPJLT device is calibrated against the published results [9] using I_D-V_G simulations and is shown in Fig. 2.

Table-I: BPJLT Device parameters

Parameter	Value
Gate length (L_g)	20 nm
Gate oxide thickness (T_{ox})	1 nm
Junction depth (X_j) or Device layer thickness	12 nm
Gate work function (ϕ_m)	5.1 eV
Donor doping in device layer (N_d)	$2x10^{19}$ cm^{-3}
Substrate doping (N_{well})	$5x10^{18}$ cm^{-3}
Supply voltage (V_{DD})	1 V

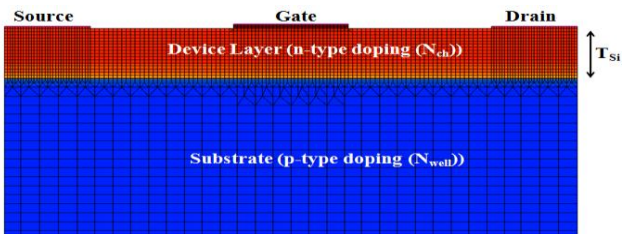

Fig .1. 2D-Structure of the BPJLT device with meshing

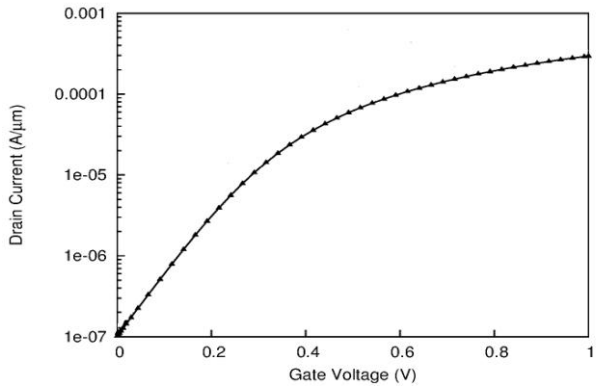

Fig. 2. I_D_V_G characteristics of the N-Type BPJLT device

III. RESULTS AND DISCUSSION

The design of JLT involves three critical design parameters channel doping (N_{ch}), silicon film thickness (T_{Si}) and gate electrode work function (WF) (refer Figure 3). Among these two important parameters (channel doping (N_{ch}), silicon film thickness (T_{Si})), which influences the radiation performance has been taken and the effect of these two parameters on BPJLT device SEU performance are studied using TCAD simulations in this section.

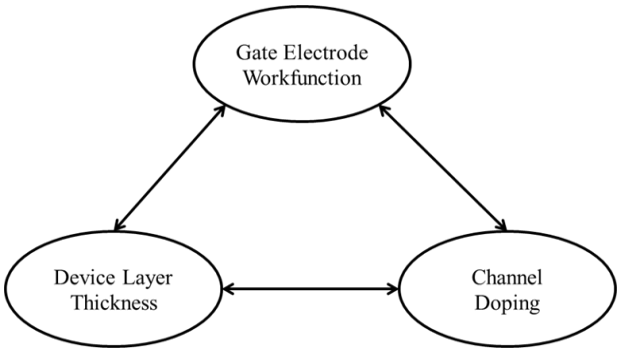

Fig .3. JLT design triangle

Before doing the radiation study, the impact of silicon film thickness (T_{Si}) and channel doping (N_{ch}) on the DC performance parameters (i.e. ON Current (I_{ON}) and OFF Current (I_{OFF})) of BPJLT device are studied and is given in Table II & III respectively.

Table II: I_{ON} and I_{OFF} of BPJLT devices with various T_{Si}

S.No	Silicon film thickness (TSi)(nm)	ON current (ION)(μA)	OFF current (IOFF)(A)
1	6	3.22	2.45E-16
2	8	60.5	1.00E-13
3	10	163	1.10E-10
4	12	295	1.02E-07
5	14	445	1.80E-05
6	16	605	1.21E-04

Table-III: I_{ON} and I_{OFF} of BPJLT devices with various N_{ch}

S.No	Channel doping (Nch) (per cm3)	ON current (I_{ON})(μA)	OFF current (I_{OFF}) (A)
1	1e19	8.69	4.28e-15
2	1.5e19	120	4.88e-11
3	2e19	295	1.02e-7
4	2.5e19	496	1.688e-7
5	3e19	709	116e-6

From Table II, it can be observed that as the silicon film thickness increases, both the ON and the OFF state currents are increases. The practical values of the film thicknesses are highlighted in Table II. Beyond this range, either the I_{ON} is too low or the I_{OFF} is too high. Similarly the increase in the channel doping increases both I_{ON} and I_{OFF}. Once again the practical values of doping values are highlighted in Table III. Beyond this range, either the I_{ON} is too low or the I_{OFF} is too high. Either the increase in the film thickness for the given channel doping or the increase in the channel doping for the given film thickness increases I_{OFF} due to the reduced electrostatic control resulting from poor depletion of the channel in the OFF state.

Since the I_{OFF} is affected drastically (Table II & III) when the film thickness or channel doping is changed, for the fair comparison I_{OFF} is maintained constant (i.e. I_{OFF} is constrained to 100 nA/μm which is the I_{OFF} of reference device). For the subsequent study carried out I_{OFF} is maintained constant. This constraint is met by changing the two other parameters as one parameter is not sufficient to achieve this constraint. Following cases are explored to study the impact of T_{Si} and N_{ch} on BPJLT DC performance.

- Case 1: Vary T_{si} and adjust WF and N_{ch} to constraint I_{OFF}
- Case 2: Vary N_{ch} and adjust WF and T_{si} to constraint I_{OFF}

In the Case 1, we have studied three different T_{Si} (12, 15, and 20 nm), and WF and N_{ch} are adjusted to achieve the I_{OFF} of 100 nA/μm.

In the Case 2, three different N_{ch} (2e19, 2.5e19, 3e19 (per cm^3)) are studied, and T_{Si} and WF are tuned to meet the I_{OFF} constraint (i.e. 100 nA/μm).

Table IV presents the ON to OFF current ratios of case 1 and case 2. It can be noticed that I_{ON}/I_{OFF} ratio gets degraded with the increase in film thickness while it improves with the increase

in channel doping. Reduced T_{Si} improves the electrostatic control of the channel in the OFF state whereas increased N_{ch} enhances the conductivity in the ON state. So the devices with increased N_{ch} and reduced T_{Si} (i.e. Case 2 devices) yields better I_{ON}/I_{OFF} ratio in the BPJLT devices. The access pulse (V(nacc)) of 10 ps of rise and fall times, and a pulse width of 250 ps is used to verify the SRAM functionality. After SRAM functionality verification, the soft error simulation is done by using heavy ion models in SDEVICE simulator. The heavy ion radiation model is

Table-IV: I_{ON}/I_{OFF} ratio of various BPJLT devices used in this study

Name	Varying Parameter	Silicon film thickness (TSi)	Channel doping concentration (Nch)	Gate work function (WF)	$I_{ON}/^{*}I_{OFF}$ ratio
Case 1	Film Thickness (T_{Si})	12 nm	2e19 cm^{-3}	5.1 eV	2894
		15 nm	1.715e19 cm^{-3}	5.4 eV	2180
		20 nm	1.15e19 cm^{-3}	5.4 eV	1501
Case 2	Channel Doping (N_{ch})	12 nm	2e19 cm^{-3}	5.1 eV	2894
		10 nm	2.5e19 cm^{-3}	5.04 eV	3316
		8 nm	3e19 cm^{-3}	4.98 eV	3738

* I_{OFF} = 100 nA/um

For further study (radiation study) on BPJLT devices we have taken only the devices with better I_{ON}/I_{OFF} ratio (i.e. Case 2 devices in Table IV).

A. SEU study on BPJLT based 6T-SRAMs

The SEU study is carried out using TCAD simulations. The 6T-SRAM cell used in this SEU study is shown in Fig. 4. The BPJLT devices with better I_{ON}/I_{OFF} ratio are used for creating SRAMs. The 3D structure of the simulated BPJLT 6T-SRAM is given in Fig. 5.

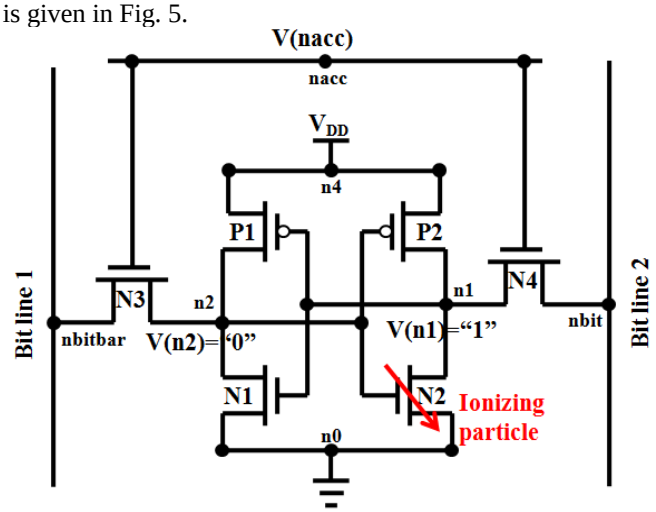

Fig. 4. 6T-SRAM cell schematic structure used in this SEU study

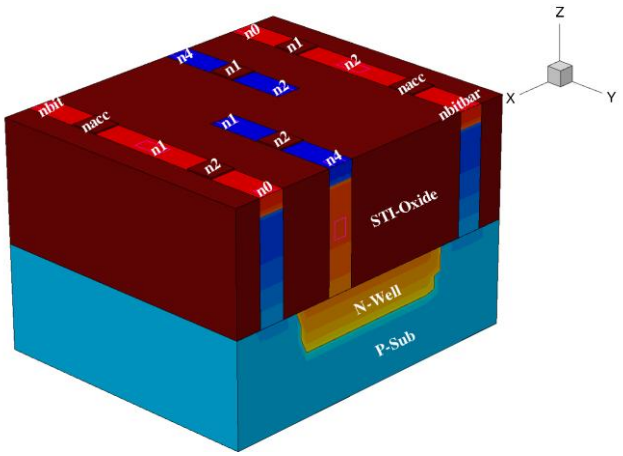

Fig. 5. Structure of the simulated BPJLT 6T-SRAM

characterized by the particle direction (perpendicular to the device), characteristic radius (20 nm), dose value or Linear Energy Transfer (LET in pC/μm or MeV/(mg/cm^2)), location of the strike, length of the ion track, temporal and spatial variation of generation rate (Gaussian function is used in this study) [17]. The radiation strikes at the sensitive node (the node which stores logic 1) of SRAM cell when the access pulse is zero (V(nacc) in Fig. 6).

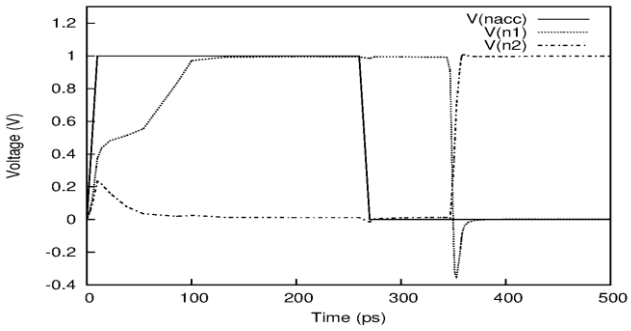

Fig. 6. Variation of node voltages with respect to time (Heavy ion strikes at 350 ps with the LET value of 0.137 MeV/(mg/cm^2)

Figure 6 illustrates the node voltages (V(n1) and V(n2)) of the BPJLT SRAM cell for the LET value (0.137 MeV/(mg/cm^2)) which flips the SRAM cell. The SEU threshold LET (LET_{th} - The minimum LET value needed to flip the SRAM cell) is obtained by varying the ion strike LET until the SRAM cell flips. It is done for all the cases considered in this study and its LET_{th} values are given in Table V. It can be observed from Table V that the BPJLT devices with the higher doping and smaller film thickness show better SEU performance i.e. higher LET_{th}. The LET_{th} of SRAM is decided by the drive current of PMOS (I_{PMOS}) and collected charge at the strike node [12]. On one hand devices with smaller film thickness provides the better electrostatic control which results in smaller collected charge. It is clearly depicted in Fig. 7. Figure 7 shows the 2-D profile of electrostatic potential across the BPJLT SRAMs during the peak radiation for a LET value of 0.1 MeV/(mg/cm^2), this LET value does not flip the BPJLT SRAM structures. The electrostatic potential at the strike location for various BPJLT SRAMs (T_{Si} = 12 nm, 10nm, 8nm and N_{ch} = 2e19 cm^{-3}

Table-V: LET_{th} of various BPJLT based SRAMs

S.No	Gate work function (WF)	Silicon film thickness (T_{Si})	Channel doping concentration (N_{ch})	Collected Charge (fC)	I_{PMOS} (µA)	LET_{th} (MeV/(mg/cm^2))
1	5.1 eV	12 nm	2e19 cm^{-3}	1.027	229	0.137
2	5.04 eV	10 nm	2.5e19 cm^{-3}	0.958	263	0.365
3	4.98 eV	8 nm	3e19 cm^{-3}	0.919	297	0.546

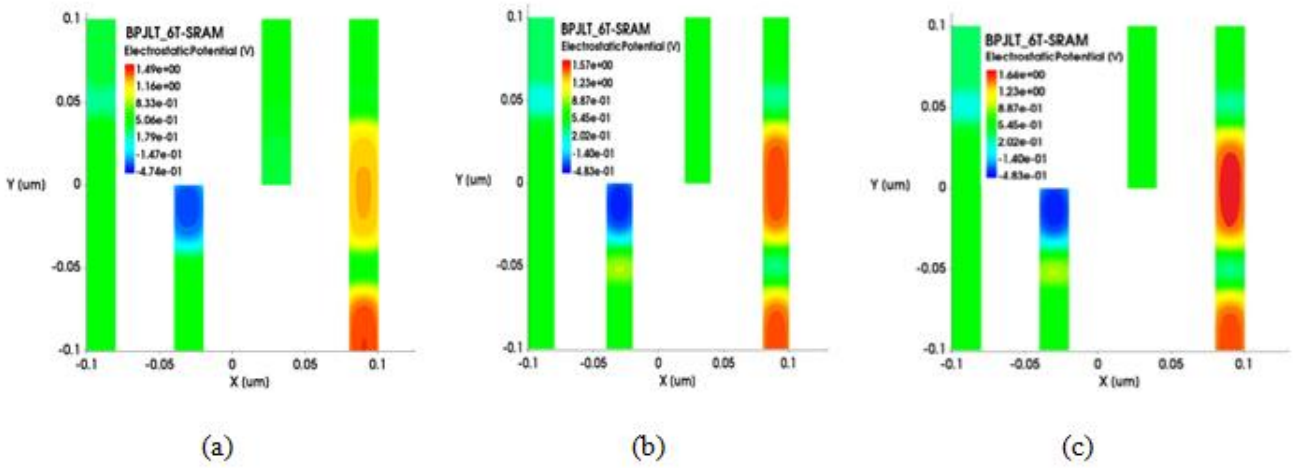

Fig. 7. 2-D profile of BPJLT SRAMs electrostatic potential (V) during peak radiation at 350 ps for various cases considered in this study i.e. T_{Si} = 12 nm, 10 nm, 8 nm and N_{ch} = 2e19 cm^{-3}, 2.5e19 cm^{-}3, 3e19 cm^{-3} respectively for a LET value of 0.1 MeV/(mg/cm^2)

2.5e19 cm^{-}3, 3e19 cm^{-3}) considered in this study is 1.49 V, 1.57 V and 1.64 V respectively. On the other hand increased N_{ch} helps in improving the PMOS drive current. These improvements resulting in the SEU performance enhancement of the SRAM cells i.e. higher LET_{th} for BPJLT SRAM which is having smaller film thickness and the higher doping.

IV. CONCLUSION

The impact of silicon film thickness and channel doping on SEU radiation performance of bulk planar Junctionless devices based SRAMs have been studied using TCAD simulations. Simulation results reveal that the BPJLT devices having higher doping and smaller film thickness provides the better SEU performance.

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