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Area and Power Potent VLSI Architecture for Modified CSLA with A Logic Optimization Technique

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Abstract*: Through generations, in an endeavor to pioneer innovative circuit designs, an adder is having the greatest importance as it is a basic building block to decide the system's overall performance. Wide varieties of adders are used for a plethora of applications in the field of Signal Processing and VLSI systems. Most predominantly used Speed efficient architecture for performing n-bit addition in VLSI applications is Square Root Carry Select Adder (SQRT-CSLA) as it pre-computes the carry and sum by assuming input carry as 'zero' and 'one'. But the overall area usage is high as it uses more number of full adders when compared to Ripple Carry Adder. Though, the existing adder designing techniques are area efficient, there is still scope to achieve area efficiency as area decides the cost of the VLSI Systems. Not only area-efficient but also power potent architectures are required to accelerate the overall performance of the VLSI systems. To meet these objectives, this paper proposes an efficient VLSI architecture for carry select adder by using logic optimization technique addressing performance constraints. The proposed architecture is designed and implemented using cadence encounter tool for different data widths ranging from 16 bits to 128 bits. The performance of the proposed 128-bit architecture achieves an area improvement of 63.43% and a power improvement of 71.00923% when compared to 128-bit SQRT-CSLA architecture

Keywords: Area Efficiency, CSLA, Logic Optimization, VLSI Adder.

I. INTRODUCTION

The digital electronics era is based on the digital data processing of the information signal that is being communicated over, and among the processing functions, addition is the most abundantly used primitive arithmetic function. While processing the data, filters are essential to reduce the noises [1] .In this regard, Finite-Impulse-Response (FIR) filter accomplished attention for its appealing characteristics such as stability and linear phase property. An adder and multiplier structure in FIR Filter implementation increases the cost when compared with IIR Filter while approaching the equal magnitude response specifications.

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Most frequently used adders adopting several performance metrics are Ripple Carry Adder (RCA), Linear Carry Select Adder (Linear CSLA), Square Root Carry Select Adder (SQRT CSLA). Amongst these, the area occupancy for RCA is less; however the speed of this adder is very less. Enhancement in speed is achieved by Carry Select Adder(CSLA)[2] but the area occupancy is very high. The area can be further reduced by using different minimization techniques at gate level design with slight rise in delay. One such technique is replacing Ripple carry adder with input carry is equal to 'one' with Binary to Excess-1 converter in SQRT-CSLA[3]. The area is further reduced by minimization of gates in the design which can be designed by the usage of Zero Finding Logic (ZFC) [4]-[5]. But the area optimization is still considered as it decides the cost of the design. Over the most recent decades, Extreme prominence has given for the circuit architectures design, realization and implementation to perform binary addition focusing a wide range of performance constraints .However, it has been inspected that the design of adder architecture becomes essential for the continually rising productivity in VLSI design. In this Paper, Low Power and Area-Efficient VLSI Architecture for Carry Select Adder using Logic optimization is proposed. The rest of the paper is structured as follows. Section II deals with Preliminaries. Section III deals with CSLA using Logic optimization technique. Section IV presents the results and discussions. Finally, the work is concluded in Section V.

II. PRELIMINARIES

This section presents the basic building blocks used in the design of the Carry select adder. Carry select adder is purported to be one of the fastest adder as it pre-computes the 'Sum' and 'Carry' for the two possible cases i.e. when input carry Ci is 'zero' and Ci is 'one'. The pre-computed sum and carry is given as data inputs to a multiplexer and the carry obtained from the former stage is given as selection input. Depending on the selection input, exact outputs 'sum' and 'carry' are computed. This pre-computation of Sum and carry decreases the delay of rippling of Carry. 2-bit RCA is designed by cascading two full adders as shown in Fig.1.If the input carry is 'zero', Full adder (FA0) is replaced by half adder. Similarly ,if input carry is 'one',FA0 is replaced by half adder, XOR gate and an OR gate, since the inputs of XOR gate in the design 2-bit RCA with input carry is equal to 'one' are 'one' and sum1(0) which is shown in Fig.2.

Thus the output s(0) can also be taken as ~sum1(0).where ~ indicates not gate.

$$S(0) = A(0)\ xor\ B(0) xor\ 1\ = A(0)\ xor\ \overline{B(0)} \quad (1)$$

$$C(0) = A(0)B(0) + A(0)\overline{B(0)} + \overline{A(0)}B(0) = A(0) + B(0) \quad (2)$$

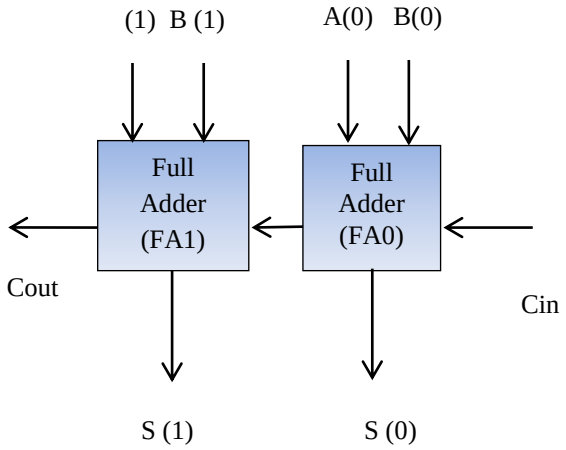

Fig.1 .2-bit RCA

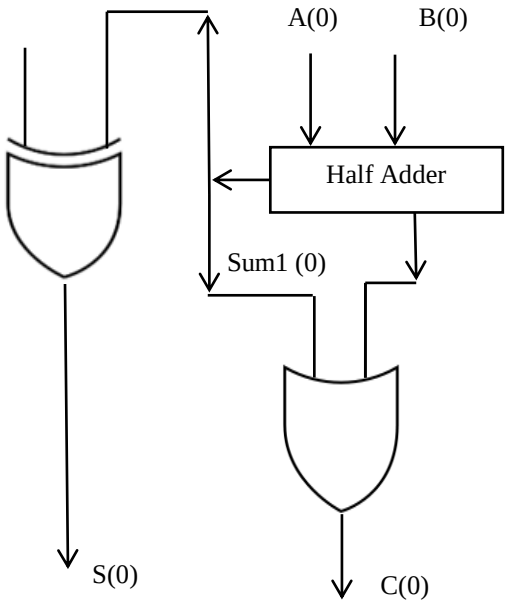

Fig.2.Conventional Full Adder with cin= '1'

From equations (1) and (2),the main digital modules required in the design of conventional full adder with input carry is equal to 'one' are Half-Adder(HA), OR gate and a NOT gate. By using these digital modules, the digital component count for various 2-bit RCA is shown in Table.1.Table.2 represents the basic digital components of Cadence Encounter Slow Library. The design for XOR gate is carried out by using two NOT gates, two AND gates and one OR gate. 2:1 MUX is designed by using one NOT gate, two AND gates and one OR gate. Half adder is designed by using XOR gate and an AND gate. Full adder is designed by using two half adders and an OR gate. The theoretical area calculations are evaluated using AOI logic [3] and tabulated in Table.3.

Table.1.Digital Components Count for Adder modules for conventional Architecture.

Main modules	OR (A)	NOT (B)	Half Adder (C)	Full Adders (D)
2-bit RCA				2
2-bit RCA with input carry cin= '0'			1	1
2-bit RCA with input carry cin= '1'	1	1	1	1

Table.2. Area of basic digital components of Cadence Encounter slow library of 90nm standard cell technology

Digital Components	Area(μm^2)
OR- gate (a)	4.541
NOT-gate (b)	2.271
AND-gate (f)	4.541
NAND-gate (h)	3.028

Table.3. Area evaluated using AOI logic for basic digital components

Digital Components	Area(μm^2)
2:1 Multiplexer (e)	15.894
XOR-gate (g)	18.165
Half-Adder(HA) (c)	22.706
Full-Adder(FA) (d)	49.953

III. CARRY SELECT ADDER USING LOGIC OPTIMIZATION TECHNIQUE

The design of 16-bit CSLA using logic optimization technique comprises of total 8 groups. The size of input data width for first input A is of two bits and of B is also two bits and output 'sum' data width for each and every group is two bits and carry size is 'one bit' as shown in Fig.3. Group0 consists of 2-bit RCA with input carry cin .The design from Group1 onwards consist of two sets of 2-bit RCA and three 2:1multiplexers and the detailed structure from Group1 onwards is shown in Fig.4.Cp is the carry out from preceding group which acts as selection line for multiplexer.

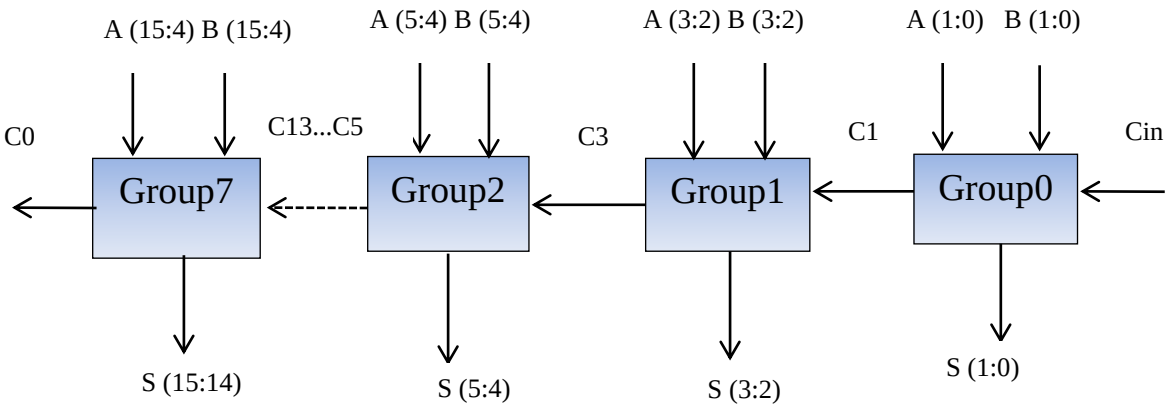

Fig.3. 16-bit Carry Select adder with groups

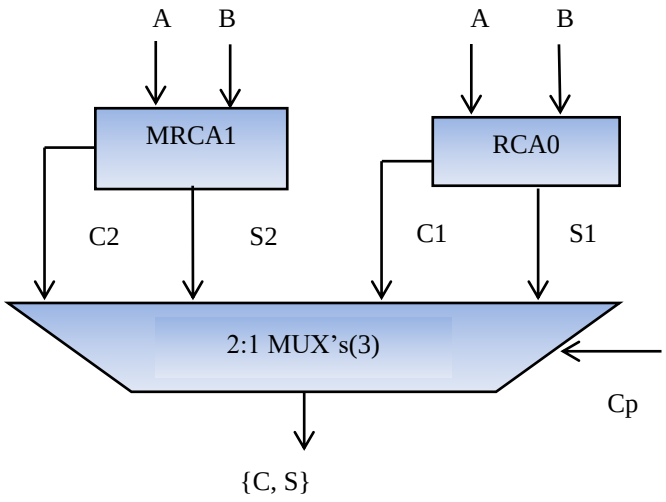

Fig.4. Group 'n' Overview

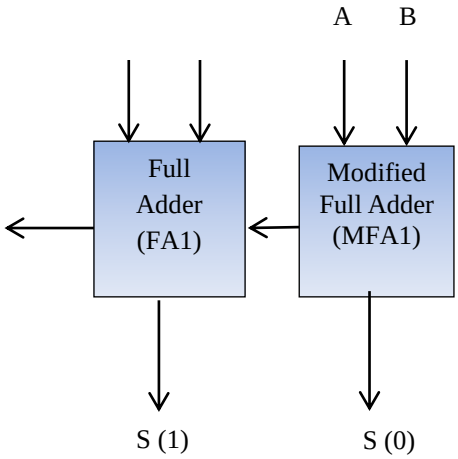

Fig.5. MRCA1

A.Group-n Architecture

The detailed architecture from Group1 onwards is explained in this section. It consists of two sets of 2-bit RCA. First set Consists of 2-bit Ripple Carry Adder with input carry is equal to 'zero'(RCA0) which is given with inputs A and B of size 2-bits and input carry is equal to 'zero' and outputs are sum (S1) and carry (C1).Second set consists of Modified Ripple Carry Adder with input carry is equal to 'one'(MRCA1) which is given with inputs A and B of size 2-bits and input carry is equal to 'one' and outputs are sum (S2) and carry (C2).The size of S1,S2 is of 2-bits.let the MSB is denoted as n and LSB is denoted as n-1.S1(n),S2(n) are given as inputs to 2:1 Mux and the obtained sum is S(n). S1 (n-1), S2(n-1) are given as inputs to 2:1 Mux and the obtained sum is S(n-1). C1 and C2 are given as inputs to 2:1 Mux and the obtained carry is C. The carry obtained from the preceding group is given as the selection input for all the three 2:1 MUX's which is denoted as Cp as shown in Fig.4.Thus if the value of Cp is 'zero' ,it selects RCA0 outputs. Otherwise it selects MRCA1 outputs.

The detailed structure of MRCA1 is as shown in Fig.5. MRCA1 is designed by using MFA1 and FA1.The major difference between conventional ripple carry adder and modified ripple carry adder is the first stage full adder with input carry is equal to 'one' is modified by using MFA1,thus the total area is optimized.From Group1 onwards,each and every group is designed using MRCA1 using logic optimization technique which inturn reduces the overall all area.As the addition operation for data width ranging from 16-bit to 128-bit,the overall optimization in area and reduction in power is achieved by using the MRCA1. The detailed structure of Modified Full Adder with input carry is equal to 'one' (MFA1) is explained in next section.

B.Modified Full adder with input carry cin= '1' (MFA1).

By using Logic optimization technique, Conventional Full adder with cin= '1' is modified as shown in Fig.6.The total area is reduced by using this modified full adder structure.

Thus the total digital count required for 2-bit MRCA1 is two NAND gates, one OR gate and one one full adder.

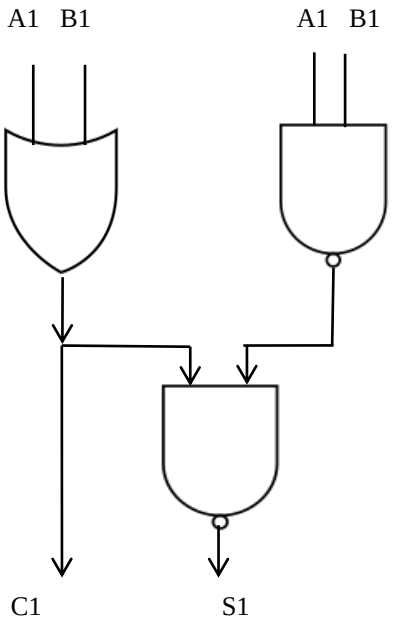

Fig.6.Modified Full Adder with cin= '1'(MFA1)

A, B, C and D represent the total digital component count for OR gate, NOT gate, Half Adder and Full adder respectively which are tabulated in Table.1. Similarly a ,b ,c ,d and h represent the area of basic digital components such as OR gate, NOT gate, Half Adder, Full adder and NAND gate respectively which are tabulated in Table.2 and Table.3

$$Area = a.A + b.B + c.C + d.D \quad (3)$$

$$Area = 2.h + 1.a + 1.d \quad (4)$$

By using equation (3), area for 2-bit RCA, 2-bit RCA with cin= '0' and 2-bit RCA with cin= '1'adder modules is evaluated and tabulated in Table.4. By using equation (4), area for 2-bit MRCA1 with cin= '1' is evaluated and tabulated in Table.4.

Table.4. Area evaluated for2-bit adder modules

Main modules	Area(μm^2)
2-bit RCA	99.906
2-bit RCA with cin= '0'	72.659
2-bit RCA with cin= '1'	79.471
2-bit MRCA1 (with cin= '1')	59.036

IV. RESULTS & DISCUSSIONS

In this section, theoretical evaluation of area for various conventional adder architectures and for the proposed architecture is evaluated and compared with practical results

A. *SQRT-CSLA Architecture area estimation using theoretical approach*

Theoretical digital count for 16-bit SQRT CSLA[3] for each and every group is evaluated and tabulated in Table.5.A, B, C, D and E represent the total digital component count for OR gate, NOT gate, Half Adder, Full adder and 2:1 Multiplexer respectively. Similarly a ,b ,c ,d and e represent the area of basic digital components such as OR gate, NOT gate, Half Adder, Full adder and 2:1 Multiplexer which are tabulated in Table.2 and Table.3. SQRT-CSLA architecture consists of five groups [3].Group1 consists of 2-bit RCA. Group2 consists of 2-bit RCA with cin='0' i.e.one full adder and one half adder and 2-bit RCA with cin ='1' one full adder ,one half adder and one OR gate and one NOT gate and three 2:1 Mux's for selection purpose.Group3 consists of 3-bit RCA with cin= '0' i.e. two full adders and one half adder and 3-bit RCA with cin = '1'i.e. two full adders ,one half adder and one OR gate and one NOT gate and four 2:1 Mux's. Group4 consists of 4-bit RCA with cin= '0' i.e. three full adders and one half adder and 4-bit RCA with cin = '1'i.e. three full adders, one half adder , one OR gate and one NOT gate and four 2:1 Mux's. Group5 consists of 5-bit RCA with cin= '0' i.e. four full adders and one half adder and 5-bit RCA with cin = '1'i.e. four full adders ,one half adder , one OR gate and one NOT gate and five 2:1 Mux's.

Table.5. Digital Component Count for SQRT CSLA

Main modules	A	B	C	D	E
Group1				2	
Group2	1	1	2	2	3
Group3	1	1	2	4	4
Group4	1	1	2	6	5
Group5	1	1	2	8	6
Total	4	4	8	22	18

$$Area = a.A + b.B + c.C + d.D + e.E \quad (5)$$

By using equation (5), total area for 16-bit SQRT CSLA is calculated as 1593.954 μm^2.

B. *Area estimation for CSLA using Logic Optimization technique by using theoretical approach*

Table.6. Digital Component Count for CSLA using Logic Optimization technique

Main modules	A	C	D	E	H
Group0			2		
Group1	1	1	2	3	2
Group2	1	1	2	3	2
Group3	1	1	2	3	2
Group4	1	1	2	3	2
Group5	1	1	2	3	2
Group6	1	1	2	3	2
Group7	1	1	2	3	2
Total	7	7	16	21	14

$$Area = A.a + c.C + d.D + e.E + h.H \quad (6)$$

Theoretical digital count for 16-bit CSLA using Logic optimization technique for each and every group is evaluated and tabulated in Table.6. A,C, D,E and H represent the total digital component count for OR gate, Half Adder, Full adder, 2:1 Multiplexer and NAND gate respectively.

Similarly a, c, d ,e and h represent the area of basic digital components such as OR gate, Half Adder, Full adder ,2:1 Multiplexer and NAND gate respectively which are tabulated in Table.2 and Table.3.By using equation (6), total area for proposed architecture is calculated as 1366.143 μm^2.Thus as the bit size increases, the area is drastically reduced.

C.ASIC Synthesis Results

The Proposed design and the conventional architectures are coded in Verilog HDL.

Table.7. Comparison of Area and Power for 128-bit adders

Architecture	Area (μm^2)	Total Power (nW)
SQRT-CSLA[3]	7888.412	379428.727
SQRT-CSLA-BEC[3]	5868.246	300078.847
SQRT-CSLA-ZFC[5]	5269.538	227574.940
KSA–SQRT-CSLA[4]	7011.165	392390.364
KSA – SQRT-CSLA-BEC[6]	5641.933	325000.917
KSA- SQRT-CSLA-ZFC[7]	4928.933	255401.279
CSLA using Logic Optimization technique	**4856.270**	**221876.170**

The performance parameters such as area and power obtained from cadence Encounter RTL compiler architectures. .By using 90nm standard cell technology for slow library with 1w power, 0.9 voltage and 125k temperature specifications the following results are reported and tabulated in Table.7, Table. 8 and Table.9 for 128-bit architectures Dynamic power depends on switching activity of the gates[8]. It has been proved that the switching activity of NOR gate is less when compared to XOR –gate. In SQRT-CSLA-BEC and SQRT-CSLA-ZFC,more number of XOR gates are used which increases the dynamic power consumption. Leakage power depends on Leakage current. Since NAND –gate is used in the design of CSLA using Logic Optimization technique, leakage power is also reduced which in turn decreases the total power consumption.

Table.8. Comparison of Leakage and Dynamic Power for 128-bit adders

Architecture	Leakage Power (nW)	Dynamic Power (nW)
SQRT-CSLA[3]	59663.442	319765.286
SQRT-CSLA-BEC[3]	39668.082	260410.765
SQRT-CSLA-ZFC[5]	34088.968	193485.972
KSA–SQRT-CSLA[4]	47092.555	345297.809
KSA – SQRT-CSLA-BEC[6]	36763.245	288237.672
KSA- SQRT-CSLA-ZFC[7]	30255.984	225145.295
CSLA using Logic Optimization technique	**26941.097**	**194935.073**

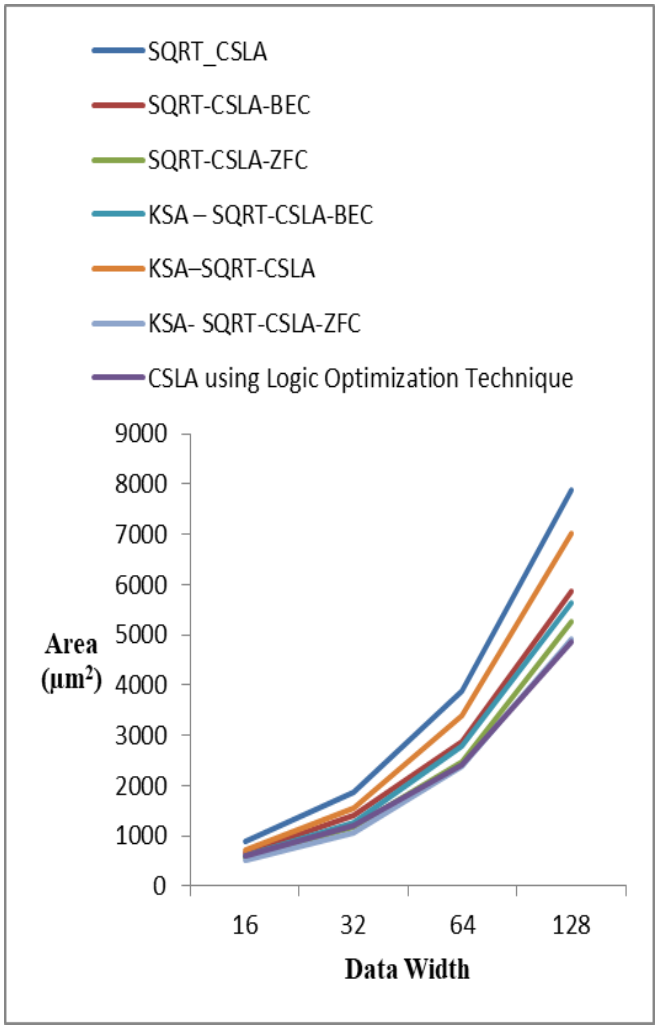

Fig.7.Comparison of Area in μm^2 for different adder architectures

The area and power values obtained from Cadence Encounter RTL compiler for the proposed design and the conventional architectures for data width ranging from 16-bit to 128-bit are shown in Fig.7 & Fig.8.

Table.9. Comparison of Combinational delay(pSec) for 128-bit adders

Architecture	Combinational delay (pSec)
SQRT-CSLA[3]	8594
SQRT-CSLA-BEC[3]	6982
SQRT-CSLA-ZFC[5]	27627
KSA–SQRT-CSLA[4]	8602
KSA – SQRT-CSLA-BEC[6]	8817
KSA- SQRT-CSLA-ZFC[7]	28034
CSLA using Logic Optimization technique	**24590**

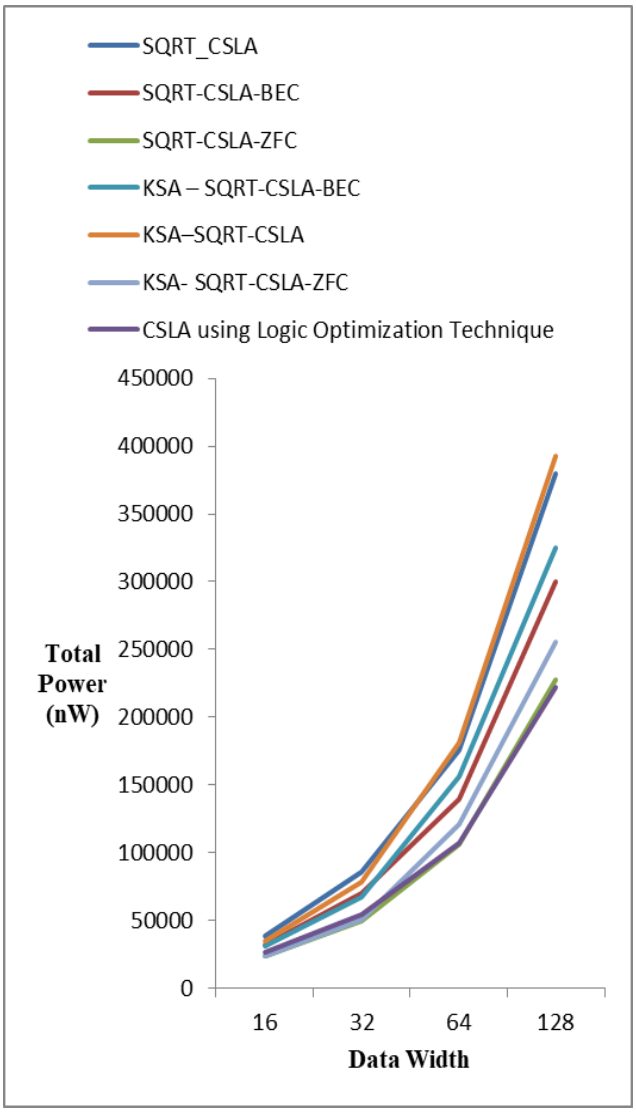

Fig.8.Comparison of total power in nW for different adder architectures

Area for CSLA using Logic optimization technique for 128-bit is reduced by 62.43767%,20.83854%, 8.509988% , 44.37346% , 16.17832% and 1.496% when compared to SQRT-CSLA, SQRT-CSLA-BEC, SQRT-CSLA-ZFC, KSA–SQRT-CSLA, KSA–SQRT-CSLA-BEC and KSA- SQRT-CSLA-ZFC architectures. As the width of the proposed architecture increases there is drastic decrease in area as shown in Fig.7. Power consumption for proposed adder for 128-bit is reduced by 71.00923%, 35.24609%, 2.56846%, 76.85106% ,46.47851% and 15.10983% when compared to SQRT-CSLA, SQRT-CSLA-BEC, SQRT-CSLA-ZFC, KSA–SQRT-CSLA, KSA– SQRT-CSLA-BEC and KSA-SQRT-CSLA-ZFC architectures.

V. CONCLUSION

In this paper, area efficient VLSI Architecture for modified CSLA using logic optimization technique is designed Simulation and synthesis is carried on cadence tools. The Performance metrics for the proposed architecture is evaluated in terms of area, delay and power for data width ranging from 16-bit to 128-bit . Area for CSLA using Logic optimization technique for 128-bit is reduced by 62.43767%, 20.83854%, 8.509988%,44.37346% ,16.17832%and 1.496% when compared to SQRT-CSLA, SQRT-CSLA-BEC, SQRT-CSLA-ZFC, KSA–SQRT-CSLA, KSA – SQRT-CSLA-BEC and KSA- SQRT-CSLA-ZFC architectures. Power consumption for CSLA using Logic optimization technique for 128-bit is reduced by 71.00923%,35.24609%,2.56846%,76.85106% ,46.47851% and 15.10983% when compared to SQRT-CSLA, SQRT-CSLA-BEC, SQRT-CSLA-ZFC, KSA–SQRT-CSLA, KSA – SQRT-CSLA-BEC and KSA- SQRT-CSLA-ZFC architectures .Thus the CSLA using Logic optimization technique is area and power potent adder which can be apt for VLSI and Signal Processing applications.

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