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Compact QCA based JK Flip-Flop for Digital System

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Abstract: ***Considering the roadmap of silicon, the high rate of shrinkage in dimensions of typical MOS circuits, genuine difficulties endanger this innovation. A quantum-dot cellular automaton (QCA) is an outstanding and conceivable answer for substitution of CMOS technology. Sequential circuits contain combinational circuits and memory elements which store binary information. Latches and Flip-flop circuits are the basic components of computerized circuits, along these lines. The area and energy of the sequential circuits has to be minimal for speed applications. Traditional implementation of JK flip-flop circuits requires more cells and consumes more energy. This paper proposes a compact and low energy JK Flip-flop, designed in CAD tool, QCADesigner. Analysis of energy was performed using the CAD tool, QCADesigner-E. The experimental results obtained in the proposed paper demonstrate the reduction in the cell count which in turn brings down the complexity of the circuit when compared to the reference QCA based JK Flip-flop circuits and it also shows a reduction in energy and area.***

Keywords: Cells, Energy, JK flip flop, QCA, QCA Designer.

I. INTRODUCTION

In the last few years, CMOS technology has facilitated the exponential growth in increase of processing power and feature size; however, the emerging technologies are the need of hour to overcome the physical limitations of CMOS devices. Few of the recent low power technologies include Reversible logic, Adiabatic logic, and Quantum-dot Cellular Automata (QCA) technology [7]. Reversible logic circuits must have one-to-one mapping between input vectors and output vectors; thus the vector of output states can always be used to reconstruct the vector of input states. Limitation of reversible logic is that pre-defined reversible logic gates have to be created before implementation of actual circuits, which is both time consuming and critical for the design [12]. Adiabatic circuits reduce power, but occupy large area and delay is also a critical factor [13].

QCA designs offer lower energy consumption and area solutions to existing CMOS logic and suitable for fabrication of nanoscale devices.

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QCA has been developed as an innovation to substitute's current MOSFET technology with certain advantages. Reducing the transistor chip size in CMOS technology will eventually cause the transistors to reach its physical limits. In 1993, [1] developed a new technology using QCA. QCA designs offer lower energy and area solutions to the existing CMOS logic. QCA based designs are suitable for fabrication of nano-scale devices. QCA based adders and multipliers are more efficient compared to CMOS based adders and multipliers as far as area and energy consumption are concerned. QCA holds an advantage of low energy utilization and has a high computational capability and switching speed.

In the current scenario of electronic gadgets, energy utilization is one of the bottlenecks for performance. Diminishing energy utilization has become a challenging issue, particularly for elite versatile gadgets such as Mobiles, telephones, PCs, tablets and so on. Low power configuration can be classified at different levels, to state a few, at system level, architecture level, circuit level and component level [2]. One mainstream method for grouping is static and dynamic. Aside from short circuit, even leakage adds to fixation of energy consumption in a circuit.

Silicon area along with power consumption has become the key factor in the chip design, especially in the digital circuits. A critical part of the power utilization in high speed digital circuits in submicron technology is dominated by leakage power. To reduce the leakage power, approaches such as transistor stacking and self-movable voltage level circuit are used. The unique characteristics and clock zones help QCA possessing a low power technology, is a field exceedingly under research. QCA has many features for processing; some of them being, timing and clocking, high density, regularity and low power dissipation. The QCA is area and power efficient in contrast to the low power techniques because all the processes are seen at the quantum level [9]. QCA technology is a suitable technology for the implementation.

QCA is a rising nanotechnology, with small component size and low energy utilization. The QCA is not only answer for scaling the feature size of transistors, but adds another method for information transformation. QCA is a field that is under extensive research. QCA offers high logic integration because of small size of dots. The QCA is more area and power efficient in contrast with the low power techniques because all the processes are seen at the quantum level. Interestingly, QCA utilizes the location of electrons in quantum dot to show binary values of 0 and 1. Sequential circuits are constructed using combinational element with a feedback (memory element in the feedback). Sequential circuits can be asynchronous and synchronous. Synchronous circuits have a single clock for all the sequential components while this is not the case in asynchronous sequential circuits.

Flip-flops are the storage components which have been utilized in the clocked sequential circuits. Capacity of each flip-flop is one bit. When a bit of information is being lost, the conventional sequential logic circuits dissipate heat because of the above reason the data once lost can't be recuperated in any terms. Flip-flops circuits are essential as they are used for implementing larger sequential circuits. The usage of QCA with clock zones for the design of JK flip-flop results in compact circuit. QCADesigner tool is used to check the usefulness of the edge-activated flip-flop. Utilizing the QCA for analysis of sequential circuits expands the efficiency in contrast with the conventional sequential circuits [4].

Transistor count and power are the real challenges in the VLSI circuits design. As number of transistors required for the circuit diminishes, the power utilization and area diminishes. Thus to limit the transistor count different procedures can be consolidated. Gate diffusion interface (GDI) being one among them. To make the circuits more area and power effective, the GDI method is observed in [1] to be the best. As specified earlier there are many low power strategies. The exploration on these methods is being done. Henceforth to give an examination among QCA and other low power methods this survey focuses on low power techniques like adiabatic, reversible logic and so on. VLSI design mainly focuses on the Power consumption.

New ways to design T and JK flip-flops are discussed in [2]. Flip-flops are the significant blocks of advanced circuits, the major concern is about the design of JK and T flip-flops. This introduces the concept of feedback path in the design of flip flops. Falling edge triggered clocking scheme is used instead of level triggered. Area constraint is the major issues in designing JK flip-flop.

Sheikhfaal et al [3] proposed two novel and imaginative outlines for sequential circuits. A productive design for RAM cell with set and reset capacity which depends on the D-flip flop and in addition, a high switching speed JK flip flop which is suitable for usage of various QCA based sequential circuits and realization of a 2-bit synchronous counter utilizing the latches was realized. Designed circuits have enhancements in terms of speed, efficiency, and complexity.

The organization of the paper is as follows: Section II discusses the basic information of QCA technology. In section III, realization and simulation of JK flip-flop circuit in QCADesigner tool is discussed. In section IV, the results obtained (waveforms, cell count, area and energy) are discussed and a comparison has been done with regards to area, cell count and energy dissipation. Section V provides conclusions and discusses the possible future work.

II. BASICS OF QCA

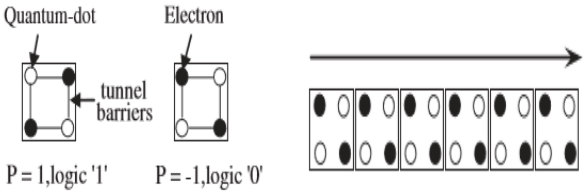
The basic element of QCA cell is exhibited in Fig. 1 (a). QCA cell comprises of four quantum dots in a square, exhibit coupled by passage obstructions, two electrons are infused into the cell. Coulombic repulsion leads to the two electrons dwelling in the inverse corners exhibiting two polarizations [4]. QCA does not require a physical voltage source and the logic value is decided by the positions of electrons. QCA computation is based out of electrostatic interaction that exists amongst all QCA cells [14]. Some essential components for QCA are wire, inverter, and majority gate voter (MV) [7] as appeared in Fig. 1. QCA wire is framed by sequence aligning of QCA cells as in Fig. 1 (b), provides information transfer depending on Coulombic interactions. The inverter is created by simply arranging QCA cells diagonally as in Fig. 2 (a); the basic inverter is constructed using seven cells as in Fig. 2 (b). The QCA cells output polarization is the inverse of the QCA cells input polarization.

Logic gates such as NOT, OR, and AND are realized by joining QCA cells together in accordance with varied configurations. The basic structure of QCA logic generally comprises of a three input majority voter M, whose output can be defined with the MV of the three inputs:

$$M(A, B, C) = A \cdot B + B \cdot C + A \cdot C \quad (1)$$

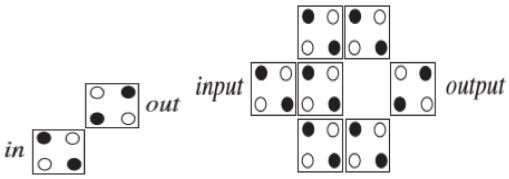
Logical OR is performed as M(A, B, 1) analogous the logical AND can be defined as M (A, B, 0).

QCA MV and its rationale image are as in Fig. 3 (a), depicts the logic function of MV and can be executed by five QCA cells. The input cells are A, B, and C and the output cell cell D is enraptured to polarization with respect to the input cell polarization. For instance, because two (of three) input cells are polarized to -1, the output cell is also being polarized to -1 as seen in Fig. 3 (a). Logical AND and OR can be executed with the help of MV by representing one input as a constant binary 0 and 1, respectively [4]. Majority logic is primarily used as a part of logical functions as opposed to using Boolean logic operators. A two bit AND is realized with a three bit MV by setting one of its contributions as logic zero as presented in Fig. 4, one of the MV is set to logical '1' it behaves as two input OR gate.



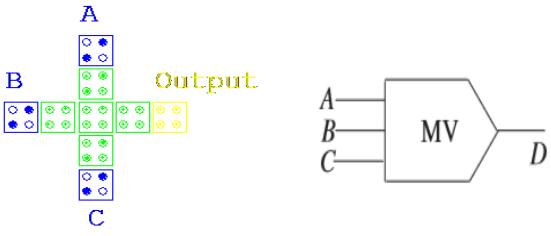
(a) (b)

Fig. 1. (a) QCA Cell. (b) QCA wire



(a) (b)

Fig. 2. (a) and (b) QCA based Inverter



(a) (b)

Fig. 3. (a) QCA majority voter (b) Equivalent majority voter structure

Clocking in QCA is used to propagate the signals and QCA based inverter realization are discussed next. The clock zones which are available in QCA are demonstrated by clock-1 (green), clock-2 (pink), clock-3 (blue) and clock-4 (white). The clock stages [8] which are available in QCA are switch, hold, release and relax as illustrated in Fig. 5. In the switch stage, QCA cells starts to become unpolarized and their interdot potential barriers are low. The hindrances are raised amid the stage and the QCA cells tend to become polarized enraptured to the condition of their input cell. In this clock stage, the switching happens. At the hold stage, boundaries are held high so the yields of the sub-array can be utilized as contributions to the following stage. Up next at the release stage, barriers are brought down and cells are permitted down to unwind to an unpolarized state [8, 9]. In the last clock stage (relax), cell boundaries are brought down and cells remain in an unpolarized state. Meanwhile, the huge scale QCA circuit is divided into four clock zones; Fig. 6 demonstrates the signal of each clock zone with the pipeline mechanism. The QCA clock flag controls all cells in a specific zone. Data moves in a pipelined design.

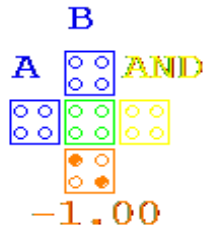


Fig. 4: QCA AND gate

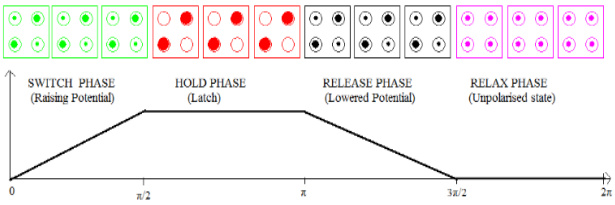


Fig. 5: Polarization of QCA Cells for different Clocking zones [10].

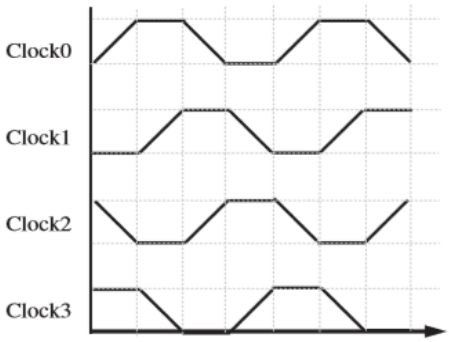


Fig. 6. Clock zone signal

III. PROPOSED QCA BASED JK FLIP-FLOP CIRCUIT

JK flip-flop is a bistable circuit used to store one bit information. When both J and K are low, the outcome is unaltered to the prior stage. In the event that the information sources have changed, at that point result sticks to J i.e., if J is high and K is low, output is set to high and if J and k values are reversed, output is reset. When J and K are high then the output is toggled.

The proposed QCA based JK flip-flop circuit is illustrated in the Fig. 7. From the JK flip-flop circuits available in literature, it was noticed that there were many redundant cells. The proposed configuration requires only 26 cells and an area of 0.06 μm^2. The proposed JK flip-flop can be used in the design of digital system, which results in compact digital system with less energy dissipation.

In first majority gate Input J is given and other input is inverted feedback from the OR gate, AND operation will be performed. Input K is inverted and is given as one of the inputs to the majority gate and the other input is feedback from output of the OR gate. Output from both gates is given as input to the middle majority gate and the OR operation is performed. Output of the OR gate will be inverted to get the JK flip-flop output. Simulation results of JK flip-flop circuit is illustrated in Fig. 8. Inputs are J and K which is shown in blue color and output is shown in yellow color.

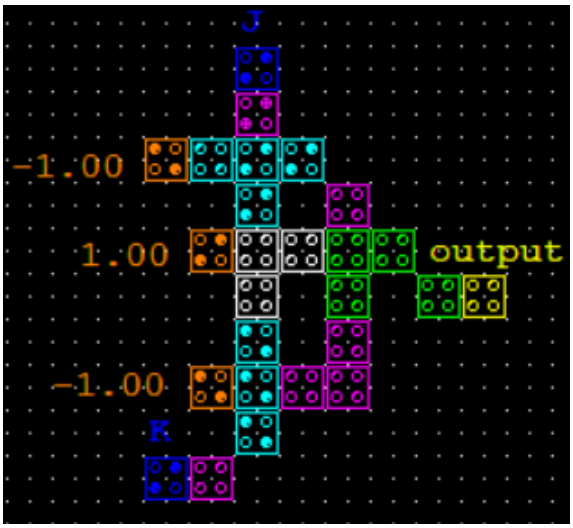


Fig. 7. QCA Design of proposed J K flip flop

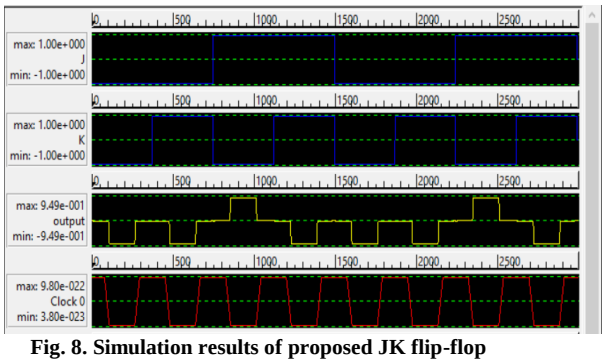


Fig. 8. Simulation results of proposed JK flip-flop

IV. RESULTS AND DISCUSSION OF JK FLIP-FLOP CIRCUITS

Simulation results obtained using the CAD tool QCADesigner and QCADesigner-E of the designed QCA based JK flip-flop circuits are presented in this section. The proposed QCA based JK flip-flop circuit is compared with the reference QCA based architectures in the literature w.r.t. cell count, area and energy dissipation. The results w.r.t. cells, area and energy are tabulated in the Table I.

It can be inferred from the Table I, that JK flip-flop in [5] consists of cell count of 31, occupies 0.08μm^2 area and an energy dissipation of 1.94e^{-02} eV. Redundant cells in the JK flip-flop circuits were reduced, because of this reduction, the area as well as energy dissipation has been brought down. Analyzing the JK flip-flop circuit in [5], redundant cells are removed which results in the reduction of cell count, area and energy dissipation. The proposed JK Flip-flop circuit requires 26 cells and occupies 0.06 μm^2 area with an energy dissipation of 1.13e^{-02} eV. The Fig. 9 illustrates area and energy comparison of various JK Flip-flop circuits. There is a 16.12 % reduction in cell count, 25% reduction in area and 41.75 % reduction in dissipation of energy in proposed architecture compared with [5]. The results informed that the proposed circuit is compact.

Table I. Comparison of QCA based JK flip-flops w.r.t. cell count, area and energy dissipation.

JK flip flop	Cell count	Area (μm)^2	Energy Dissipation (eV)
[4]	119	0.15	5.46e^{-02}
[6]	80	0.11	2.29e^{-02}
[2]	56	0.10	2.10e^{-02}
[5]	31	0.08	1.94e^{-02}
Proposed	26	0.06	1.13e^{-02}

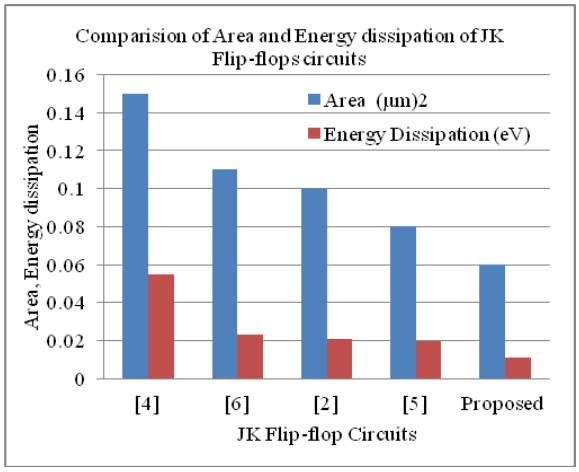


Fig. 9. Comparison of various QCA based JK flip-flop circuits.

V. CONCLUSIONS

The sequential circuits are often used in digital circuits consume more area and power. Compact sequential circuits are preferred for high speed circuits. In this paper, effective QCA based JK flip-flop circuit have been proposed and implemented in QCADesigner. CAD tool QCADesigner-E is used for estimating the energy. QCADesigner tool is used for analyzing the proposed JK Flip-flop circuits functionality. The JK flip-flop circuit proposed has lesser circuit complexity and with energy consumption compared to reference circuits. The results demonstrate an improvement of the proposed circuit w.r.t. cell count, area and energy consumption when contrasted with previous outlines. In future the proposed JK flip-flop design can be used in the construction of T flip-flop, counters etc., which results in lesser cell count and dissipates less energy.

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