Automatic Evaluation of Analog Circuits using e-Sim EDA Tool

Poonam J. Dang, Harshal A. Arolkar

Abstract*: *E-learning and online exams have become norm of the day. E-learning and evaluation of what user has learnt through it, now spans all the disciplines of learning like science, arts, commerce, business, engineering and computer science. Online exams are used as tool for assessing large number of students at a faster pace. Automatic evaluation of concepts is one of the major part of online exams. In this paper the researchers have proposed an online examination system for creating and evaluating analog circuits. The researchers have taken into account electronic circuits that generates analog output and have evaluated and graded these circuits automatically based on its logical and functional aspects. The proposed system will save time and efforts put by faculty in evaluation of large number of students.

Keywords* : *Analog Circuits, Automatic Evaluation, EDA, E-learning, Electronic Circuits, E-Sim, Half Wave Rectifier, Netlist.

I. INTRODUCTION TO AUTOMATIC EVALUATION

E-learning is seen as a future application worldwide as it promotes lifelong learning by enabling learners to learn anytime, anywhere at the learner's pace [6]. E-learning platforms are used by some educational institutions to handle administrative work, attendance, assignments, results, exams, chat interface, forum discussion, feedback activity, evaluation of tests/assignments and many more. LMS (Learning Management System) is an e-learning platform. Today LMS is paving a new road by changing the existing ways of teaching and learning, from a traditional in class way to totally synchronous or asynchronous distant one [2]. E-learning platforms are normally located on a computer on the Internet and are typically accessed by means of a Web browser. E-learning platform also supports online examinations and evaluations. Many educational organizations already have the infrastructure required to support online tests and have also started experimenting with such tools in their teaching learning activities.

Examinations contain open ended and close ended questions. Evaluation of close ended questions are quite simple and easy. When we talk about evaluation of open ended questions, it can be tricky, difficult and time consuming.

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Math problems, programming definitions of various programming languages, electronic circuit designs, digital circuit designs and many more are logical questions.

These type of questions can be solved by many ways. Faculties must put lot of concentration and time to evaluate these type of problems. As the number of permutations and combinations for input in problem grow so does the complexity in evaluation. This research thus is concentrated on reducing the time and effort required by an evaluator for such complex evaluation.

II. RELATED WORK

Zachary Kurmas has used JLS (Java Logic Simulator) digital logical simulator to design a JLSCircuitTester tool that is used to test the simulated digital logic circuits. Complex digital circuits have multiple input combinations and corresponding expected outputs. It is not possible to check student circuit design with all input combination. Generally faculty give some of the inputs and check output, then accepts the design and provide marks. To solve this problem author provides file with various combinations of input and their corresponding outputs. This tool simulates the circuit design for each of the input test cases in the file and reports a mismatch. This tool does not automatically assign grade to circuit design [10].

Gutierrez et. al introduced a new MOODLE (Modular Object Oriented Dynamic Learning Environment) module called CTPractical which evaluates VHDL (Very High Speed Integrated Circuit Hardware Description Language) assignments automatically. This module is divided in two parts, one is control block and other is activity module. Control block module provides access to teachers and students according to their role. Activity module provides various practical lists. Student team submit zip file of their submission of assignments. Zip file contains project source file that is related to VHDL descriptions of the digital circuits corresponding to the assignment. To create VHDL descriptions students are using CAD design tool Xilinx. This module provides two types of checking. First type is formal checking such as bad file name, missing files or erroneous signal names. Once this checking is completed then functional testing is started. For this testing module externally uses VHDL simulator. In this system Modelsim VHDL simulator is used. It can be run in command line mode also. In this checking, simulation of students VHDL file is started and if no error is generated in simulation then simulation output file is compared with teacher's reference file. If both files are equal then practical will be graded accordingly. The system has capacity to provide feedbacks also [3].

M. Nemec et. al shows the automatic evaluation of basic electrical circuits. System is divided in three tasks. In first task, faculty provides circuit design and places the question of calculation of current and voltages across the components given in the circuit. Evaluation is provided on the basis of comparison of corresponding components' current and voltage values of teacher and students. In second task, students are given predefined components and they have to create circuit design. Circuit can be created in many ways. Here faculty designs a question in such a way that there is only one correct circuit for the question. Then evaluation is done by comparison of faculty graph file and student graph file. In third task, students have options to choose any component to create circuit design. There is no faculty file available for comparison. So this task is formulated reasonably and evaluation is done automatically [5].

III. PROPOSED RESEARCH WORK

The analog electronic circuits are designed and implemented physically using electronic components. Physical implementation require costly equipment and recourses, which are otherwise available to limited number of students due to constrains of time. It is not possible to do practice at home for students due to expensive resources. To solve these problems institutions today use software tools which allow designing and simulation of circuits. These software tools are called Electronic Design Automation (EDA) tools [1]. Vijay Nehra et. al have documented some open source EDA tools [8]. Few other EDA tools available in the market are LTSpice [7], QUCS [4] and e-Sim [9]. Many more such tools are available in the market. These tools allow only drawing and simulation of circuits without testing options.

This paper proposes an online platform that helps a faculty to design and evaluate analog electronic circuits. The platform provides an interface that allows a faculty to create a test which can be attempted by 'n' number of students. Each of these students are provided an interface wherein they can design a circuit and upload it for evaluation. The system evaluates all uploaded circuits and grades them as per the predefined rules given by faculty. We have selected e-Sim EDA tool for designing of circuit. This research provides various levels of automation and assistance for exams related tasks such as creation of circuit design question paper, conduction of online exam, drawing of circuit designs and online evaluation of circuit designs automatically. Fig. 1 shows the use case diagram of proposed online platform.

IV. PRACTICAL IMPLEMENTATION

The researchers have designed a web interface that can be used by a faculty and students. To design electronic circuits e-Sim EDA tool has to be integrated in the web interface. As can be seen in use case, the interface allows us to create and store questions, test and grades. The system can be divided in three parts. The first part is question and test creation, which is performed by faculty. The second part is test attempt, in which students create and upload the answers to question asked. The final part is automatic evaluation and grading that is done based on the business logic defined in the question. The system is capable of evaluating the circuit in functional and logical aspects. To perform both these evaluation faculty will have to upload two files on server. One is netlist file and other is text representation of graph file. In functional evaluation, the system compares faculty's graph file and students' graph file. These files are in .txt format. According to comparison, system will provide marks. In logical evaluation, the system compares netlist file uploaded by faculty with netlist file uploaded by students'. Here the grading is done relatively based on number of components used by student and the way components have been connected.

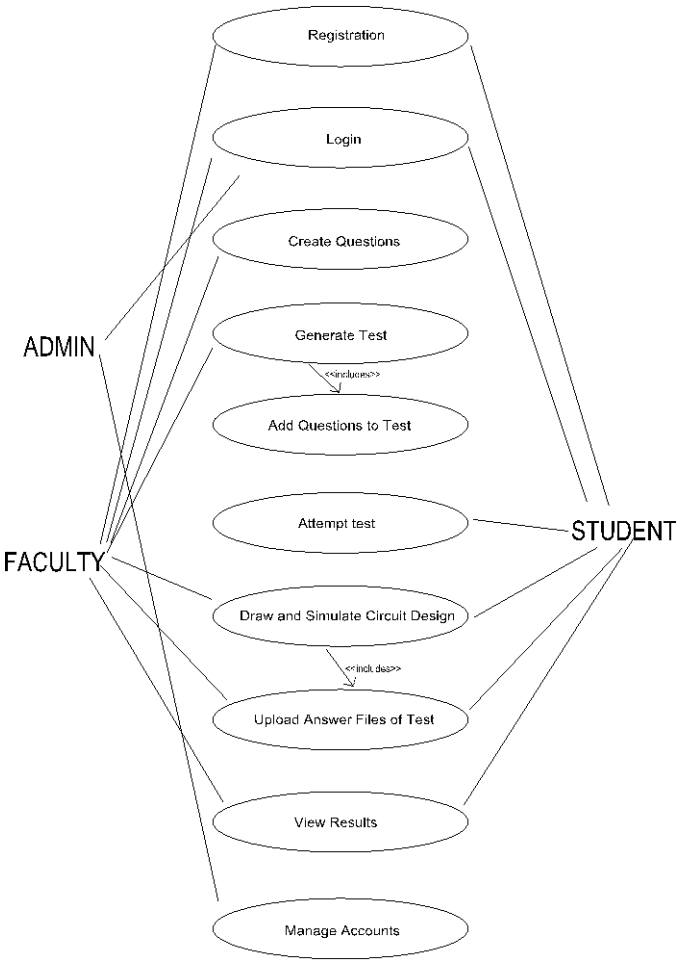


Fig. 1. Use case diagram of Online Platform LoC (Lab of Circuit)

The working of system is as shown below. Steps for creation of question and test by faculty.

Step 1: Faculty has to login

Step 2: Create question with components list, components properties and simulation type with properties.

Step 3: Assign marks for logical and functional evaluation of the question.

Step 4: Draw correct circuit design. A sample circuit design drawn by faculty is shown in Fig. 2.

Step 5: Enter simulation values as mentioned values as mentioned in question.

Step 6: View and upload netlist file (.txt) of drawn circuit design. Fig. 3 shows a netlist file of circuit design drawn by faculty. Simulator of e-Sim describes components, interconnection of components and simulation information in text format.

Step 7: View graph file of drawn circuit design. If graph file visible is correct as per faculty then question is created. E-Sim creates a text file that stores data simulation regarding the graph in the system. Fig. 4 and Fig. 5 show the graph file and text file of circuit created by faculty.

Step 8: Create test and add question to test.

Step 9: Logout.

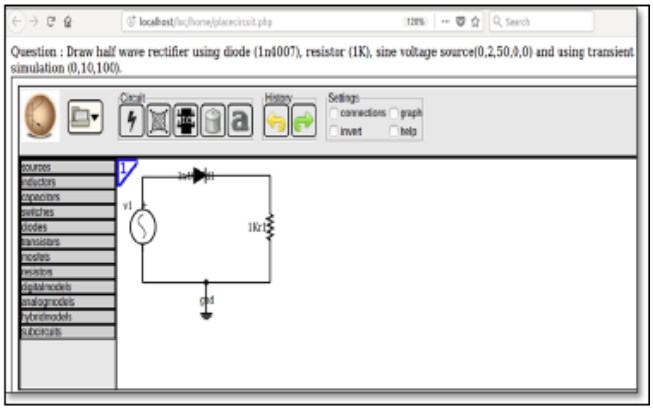


Fig. 2. Circuit Design Drawn by Faculty

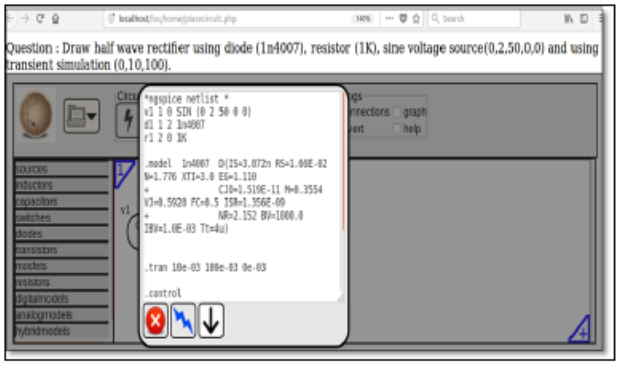


Fig. 3. Netlist File of Circuit Design Drawn by Faculty

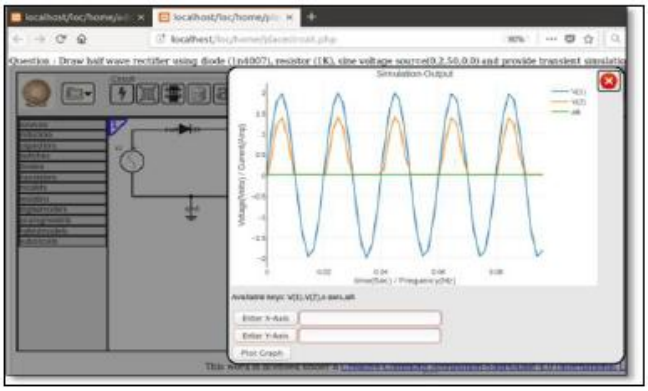
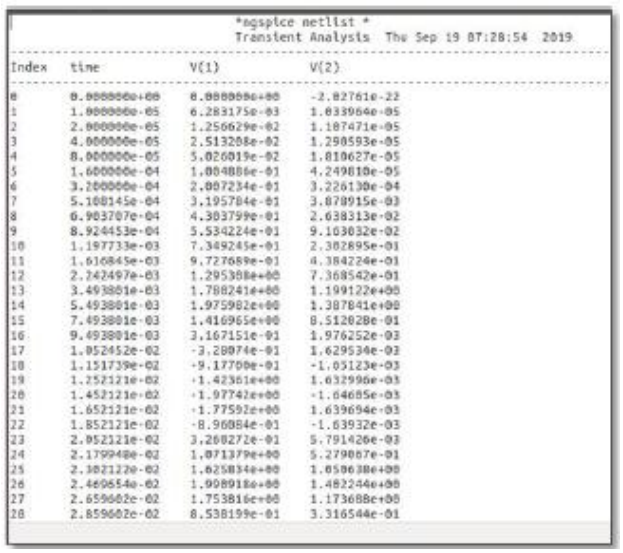


Fig. 4. Graph File of Circuit Design Drawn by Faculty



*ngspice netlist *
Transient Analysis Thu Sep 19 07:28:54 2019

Index	time	V(1)	V(2)
0	0.000000e+00	0.000000e+00	-2.82761e-22
1	1.000000e-05	6.283175e-03	1.033964e-05
2	2.000000e-05	1.256629e-02	1.107471e-05
3	4.000000e-05	2.513288e-02	1.290593e-05
4	8.000000e-05	5.026019e-02	1.810627e-05
5	1.600000e-04	1.004886e-01	4.249810e-05
6	3.200000e-04	2.007234e-01	3.226130e-04
7	5.108145e-04	3.195784e-01	3.878915e-03
8	6.983707e-04	4.383799e-01	2.638313e-02
9	8.924453e-04	5.534224e-01	9.103032e-02
10	1.197733e-03	7.349245e-01	2.302895e-01
11	1.616845e-03	9.727689e-01	4.384224e-01
12	2.242497e-03	1.295388e+00	7.368542e-01
13	3.493801e-03	1.788241e+00	1.199122e+00
14	5.493801e-03	1.975982e+00	1.387841e+00
15	7.493801e-03	1.416965e+00	8.512028e-01
16	9.493801e-03	3.167151e-01	1.976252e-03
17	1.052452e-02	-3.28074e-01	1.629534e-03
18	1.151739e-02	-9.17709e-01	-1.05123e-03
19	1.252121e-02	-1.42361e+00	1.632996e-03
20	1.452121e-02	-1.97742e+00	-1.64685e-03
21	1.652121e-02	-1.77593e+00	1.639694e-03
22	1.852121e-02	-8.96084e-01	-1.63932e-03
23	2.052121e-02	3.260272e-01	5.791426e-03
24	2.179948e-02	1.071379e+00	5.279087e-01
25	2.302122e-02	1.625834e+00	1.650638e+00
26	2.469654e-02	1.998918e+00	1.482244e+00
27	2.659602e-02	1.753816e+00	1.173688e+00
28	2.859602e-02	8.538199e-01	3.316544e-01

Fig. 5. .txt File of Graph File of Circuit Design Drawn by Faculty

Step 1: Student has to login.

Step 2: Attempt test.

Step 3: Draw circuit design of question which is given in test. The students are also provided e-Sim interface to draw circuit design.

Step 4: Enter simulation values as mentioned in question.

Step 5: View netlist file and upload netlist file.

Step 6: View graph file of drawn circuit design.

Step 7: Submit test.

Step 8: Automatic evaluation of submitted answer is done by system

Step 9: Marks shown to student.

Step 10: Logout.

Steps for attempting the test by students.

V. RESULTS AND OUTCOME

For testing the system a sample half wave rectifier circuit has been created by faculty based on the question specification mentioned below.

Draw half wave rectifier using diode (1n4007), resistor (1k), sine voltage source (0,2,50,0,0) and provide transient simulation (0,10,100).

Fig. 2,3 and 4 shows the designs created by faculty for this system. For this question the total grade of 100 is to be assigned, which has further been divided as 30 grades for functional evaluation and 70 grades for logical evaluation. The functional evaluation is further divided in two parts as 30% marks (21 marks) for component list and 70% marks (49 marks) for component connectivity. Table - I shows the evaluation result of 10 students who attempted the test. The table has used following conventions for representing component connectivity.

Sine Voltage Source : SVS

Resistor: R

Diode: D

Gnd: G

Table- I: Evaluation result of attempt by 10 students

Students	Logical Evaluation		Correct Graph Generated in Functional Evaluation	Grades Obtained		
	Components Used	Components Connectivity (in series order)		Marks of Logical Evaluation (70 Marks)	Marks of Functional Evaluation (30 Marks)	Total Marks
Student 1	SVS, R, D, G	SVS->D->R-> G	Yes	70.0	30.0	100
Student 2	SVS, D, G	SVS->D->G	No	50.17	9.19	59.36
Student 3	SVS, R, G	SVS->R->G	No	26.83	9.41	36.24
Student 4	SVS, R, D	SVS->D->R	No	0.0	0.0	0.0
Student 5	SVS, R, D, G	SVS->R ->D-> G	No	53.67	15.36	69.03
Student 6	SVS, R, D, G	D->SVS->R->G	No	53.67	13.76	67.43
Student 7	SVS, R, D, G	SVS->D->R-> G (Changes the polarity of voltage source)	Yes	61.83	12.97	74.80
Student 8	R, D, G	D->R-> G	No	0.0	0.0	0.0
Student 9	SVS, R, D, G	SVS->D->R-> G (Reverse Diode)	Yes	61.83	13.42	75.25
Student 10	SVS, R, D, G	SVS->D-> R- >G (Reverse Diode and changes the polarity of voltage source)	Yes	53.67	18.20	71.87

In Table - I, student 1 has attempted circuit design question with all four components and proper interconnection. so student 1 has got 100 marks. Student 2 has attempted question with three components and interconnection is wrong, hence his score is accordingly. Student 3 has attempted with three components, here diode is not used. In this scenario input graph is equivalent to output graph. Student 4 has not taken gnd, in this scenario netlist file and graph file is not created, hence the student gets zero marks. Student 5 and 6 have taken all components but their interconnections are different. Student 7 has taken all components and interconnection is also correct but he/she has changed the polarity of power source. His/her graph file is different than faculty file. Student 8 has not taken power source, in this case graph is not generated. Student 9 has changed polarity of diode so reverse graph is generated which is correct but different from faculty graph file. Student 10 has changed diode and power source polarity so again graph file changes.

VI. CONCLUSION AND FUTURE SCOPE

The proposed system seems to have a huge potential in becoming a mainstream online automatic evaluation system. The results obtained using the system are promising. It will help a faculty to create repository of question and evaluate them with less efforts and in less time. The students can also use this system for the purpose of self evaluation. As of now the system uses crude evaluation mechanism. The future scope here is to involve self test case creations of the question entered by faculty and provide all permutation and combination of design the circuit. The work for the same is in progress and will presented soon.

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