14 Transistors CNTFET and CMOS Full Adder Cell for Modified GDI Technique

Priyanka Tyagi, S.K Singh, Piyush Dua

Abstract: Adder Is Basic Unit For Any Digital System, Dsp And Microprocessor. The Main Issue In Design High Speed Full Adder Cell With The Low Power Dissipation. As We Know Cmos Technology Used For Vlsi Designing Cmos Has Many Drawbacks As High Power Short Channel Effect Etc. Then Cntfet (Carbon Nanotube Field Effect Transistor) Has Been Developed Which Has Same Structure As Cmos. The Difference Between Structure Of Cmos And Cntfet Is Their Channel. In Cntfet Channel Is Replaced By Carbon Nanotube. In This Paper We Compare Full Adder Circuit Using Cntfet With Gdi Technique And Cmos Implementation Of Adder Which Gdi Technique. Gdi Technique Is Used For Speed And Power Optimization In Digital Circuit. This Can Also Reduce The Count Of Transistor Which Affects The Size Of Device.

Keywords:CNTFET, CMOS, GDI , PTL , C^2MOS ,MGDI, Delay, PDP

I. INTRODUCTION

In today VLSI technology area, speed and power consumption are the important factor. With advancement of technology the need of device scaling is increase. But scaling down in CMOS has many side effects such as high power density, short channel effect and drain induced barrier lowering. [1] The number of transistor increase on integrated circuit in couple of years . As count of transistor increase on IC it will reduce the size of device. The size and area of digital devices is important factor in their performance. To overcome the scaling effect in CMOS technology we have been delivered CNTFET in place of CMOS [2]. CNTFET structure is same as CMOS. In CNTFET the silicon channel was replaced by the Carbon Nanotubes[14]. CNTFET is most promising technology because its operating principle is similar to CMOS. The electrical properties of the CNTFET are much better than the CMOS because the mobility of the Carrier are faster than the silicon[15].The fabrication is also similar for both CNTFET and CMOS. The twin well process is used for fabrication. The CNTFET has current carrying capacity.

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CNTFET is most promising component in today digital world. Many logics were developed using CNTFET such are Arithmetic unit memories and multivalve logic. In many VLSI applications as Microprocessors and image processing use the arithmetic logic. The one bit full adder circuit is the basic unit for all the digital circuits. By improving the performance of full adder can improved the overall performance of the modules. Less complex adder cell can give the effective results in the field of area, power dissipation and delay. To improve the performance of arithmetic functions research a design various logic style such as CMOS complementary logic Pseudo NMOS, Dynamic CMOS, Clocked CMOS logic(C^2MOS), CMOS domino logic, cascade voltage switch logic and past transistor logic[6-8].

Transistor gate provide low voltage swing but need more area as compare to past transistor. Pseudo NMOS is fast but reduce noise margin. [5] PTL design has advantages such as less area low dissipation and less delay. But PTL is only better for few digital circuits such as multiplexers and Adders. On the other hand PTL design found slow and consumes more power as compare to CMOS implementation [4-5].

To solve the problem of PTL we approach to GDI technique. GDI used to implement low power logical circuit and also simplify the complex logic with less count of transistor. In our paper we compare the performance of full adder for two different technique first GDI for CMOS and Second CNTFET with MGDI technique.

II. PROPOSED GDI TECHNIQUE

Gate diffusion input cell is 3 terminal device same as CMOS. The 3 terminals are Gate, P node and N node. G is common input for PMOS and NMOS. The body terminal of PMOS and NMOS are connected to their diffusion to minimize the body effect [9]. Figure 1 shows the basic GDI cell [13].

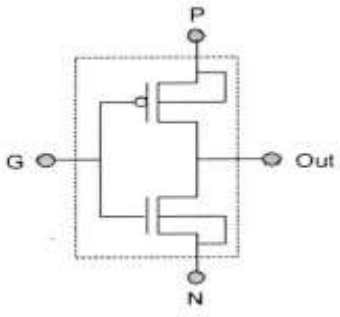

Figure1 : Basic GDI Cell

GDI cell are introduced to resolve the problem of the low voltage swing. Other logics had the low swing problem because of drop in the threshold voltage in the channel.GDI cell decrease gate leakage current and sub thrashed hold current as compare to the CMOS implementation [9] . This factor is disadvantage of GDI cell. To improve the GDI Modified GDI cell has been developed.

III. MODIFIED GDI TECHNIQUE:

Modified Gate diffusions input cell is also three terminal devices. MGDI cell has three input G(Gate), P(PMOS), N (NMOS) for CMOS. Gate is common input for PMOS and NMOS. In CNTFET structure will remain same but there are PCNT an NCNT. As figure shows P node is for input of PMOS/PCNT and N node is input of NMOS/NCNT. MGDI cell is similar to GDI circuit but bulk of transistor PMOS and NMOS are connected to VDD and GND respectively [12]. The working of MGDI cell is similar to inverter logic .PMOS/PCNT work on logic'0' and NMOS/NCNT work on logic '1'. Figure 2 and figure 3 shows the basic MGDI cells for CMOS and CNTFET respectively.

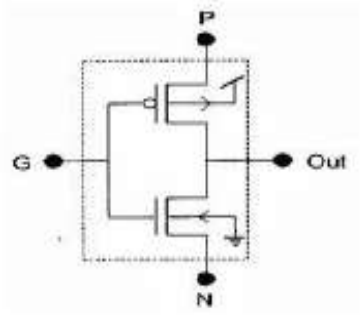

Figure2: MGDI Cell of CMOS

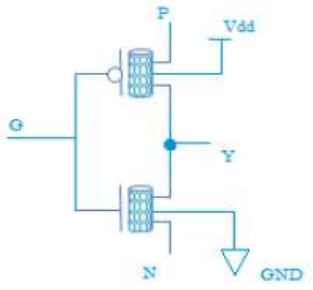

Figure3: MGDI Cell of CNTFET

MGDI cell overcome the disadvantages of GDI cell. In MGDI cell the G,P,N terminals can be varied but B_p and $B_n$nodes will remain connected to VDD and GND respectively. MGDI has the advantages over the GDI in terms of the area , Power dissipation and delay.

GDI cell fabricate in twin well progress. GDI technique is used to simplify the complex logic. GDI cell is best structure for high speed and low power logic. GDI also reduce the chip area by decrease the count of transistor [10-11]. GDI structure has less delay and power consumption.

IV. PROPOSED FULL ADDER STRUCTURE

Adder is the arithmetic logic unit which has the capability to add two numbers. In digital electronics the adder is the combinational circuit i.e it is the combination of different logics and has no memory unit. Full adder can be used in arithmetic logic units(ALU), processors and other digital modules. In these modules adder used for address calculation and other functions. By modify the adder circuit many circuits can be modified. CNFET based full adder has many advantages as compare to the CMOS. Now CNTFET adder combines with MGDI technique to improve the performance of the Full adder.

There are three inputs terminals A ,B ,C in the full adder. These three inputs are I bit for 1-bit full adder. There are many Full adder circuit according to the input as 4 bit, 8 bit, 16 bit, 32 bit etc. There are two output for the full adder that is S (SUM), Carry.

For conventional adder the equation of Sum and carry are as represented in equation 1&equation 2:

$$Sum = A \oplus B \oplus C \quad [1]$$

$$Carry = AB + BC + CA \quad [2]$$

For better performance we have to simplify the logic for MGDI technique. The equations are modified such as given below [4].

$$Sum = ABC + AB'C' + A'BC' + A'B'C$$
$$C(AB + A'B') + C'(AB' + A'B)$$
$$C(A \oplus B) + C'(A \oplus B)'$$
$$Sum == A \oplus B \oplus C \quad [3]$$
$$Carry = AB + BC + CA$$
$$AB + BC(A' + A) + AC(B' + A)$$
$$AB + A'BC + ABC + AB'C + ABC$$
$$AB(1 + C) + C(A'B + AB')$$
$$Carry = AB + C(A \oplus B) \quad [4]$$

According to the equation 3 & 4 the function can be design using two XOR gate, two AND gate and one OR gate. For sum XOR gates are connected serially. For carry function we use OR, AND & XOR gate according to equation.

The equation 3 and 4 use to implement. 14T MGDI full adder. The figure 4 show MGDI implementation of CMOS and figure 5 show the MGDI implementation of CNTFET.

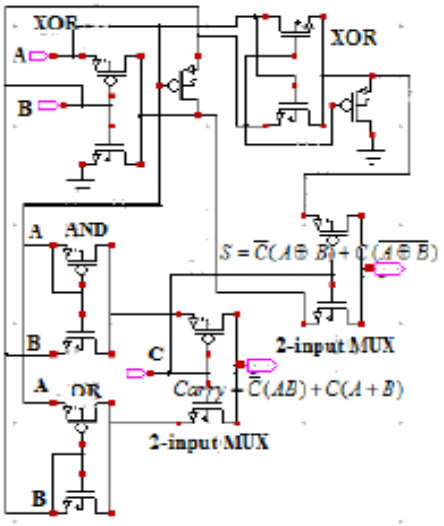

Figure4: 14T MGDI CMOS Full Adder

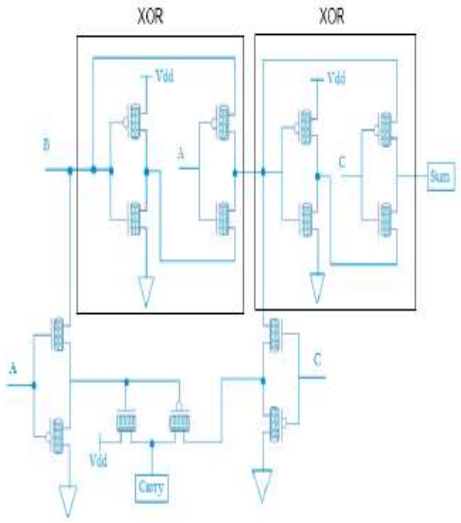

Figure5: 14T MGDI CNTFET Full Adder

V. RESULTS ANALYSIS

The Performance of full adder cell has been analyzed at different parameter like delay power dissipation. The transistor count had also reduced. In this paper we compare these parameters for CMOS MGDI technique and CNTFET with MGDI Technique. The simulation of CMOS done at 1V to 5V with 0.5V step voltage. The simulation of CNTFET adder simulated on 0.8V. The overall performance of the adder shown in table 1 [4-5]. The table represents the power dissipation, delay and power delay product (PDP) for both techniques. Power delay calculated by multiplying power dissipation and delay of circuit.

Table1 : Performance of Full Adder in MGDI Technique

Parameter	CMOS using MGDI	CNTFET using MGDI
Delay (ns)	0.02912	.0059
Power Dissipation (µw)	10.56	0.00151
Power Delay Product (Joule)	3.07×10^{-16}	8.91×10^{-21}

VI. CONCLUSION:

In this paper CNTFET fill adder circuit is presented with MGDI technique. Then this circuit compared with CMOS MGDI implementation. The various parameters are compared in both implementations. The parameters are delay power dissipation and power delay product. The result shows that CNTFET implementation is better as compare to the CMOS MGDI implementation. The conclusion of the paper is CNTFET is better and most promising component in today'sVLSI technology. For betterment of CNTFET performance we use it with MGDI technique for high speed and less power consumption. It has less delay as compare to the other full adder architecture. So the paper conclude that the MGDI technique with CNTFET reduce the size of devices increase the speed and provide high performance circuit.

REFERENCES

1. P. Saini and R.Mehra. " Leakage Power Reduction in CMOS VLSI Circuits," International Journal of Computer Application, pp. 42-48, vol-55- no. 08 , October 2012.
2. Ali Ghorbani and Ghazaleh Ghorbani., "Energy Efficient full adder cell design with using carbon nanotube field effect transistors in 32 nanometer technology", International Journal of VLSI design & Communication Systems (VLSICS) vol.5, no.5, October 2014.
3. J. Deng, "Device Modeling and Circuit Performance Evaluation for Nanoscale Devices: Silicon Technology beyond 45 nm Node and Carbon Nanotube Field Effect Transistors", doctoral dissertation, Stanford University, 2007.
4. P Chanderashekar,R Karthik and Ardhi Bhavana," Design of low threshold Full Adder Cell Using CNTFET" International journal of Applied Engineering Research vol 12,no.12, 2017.
5. R.UMA and P. Dhavachelvan," Modified Gate Diffusion Input Technique: A New Technique For Enhancing Performance In Full Adder Circuit" 2nd International Conference On Communication , Computing & Security[ICCCS-2012],2012, pg-74-81.
6. Oh-Hyeong Kwon," A Boolean Extraction Technique for Multiple Level Logic optimization" - IEEE 2003
7. R.Uma, "Bit Fast Adder Design: Topology and Layout with Self Resetting Logic for Low Power Vlsi Circuits", International Journal of Advanced Engineering Sciences and Technology, Vol No. 7, Issue No. 2, 197 205, 2011.
8. R.Uma and P. Dhavachelvan ,"Analysis on Impact of Behavioral Modeling in Performance of Synthesis Process", The secondInternational Conference on Advances in Computing and Information Technology, July 2012, Published in Advances in IntelligentSystems and Computing book series of Springer, Pg-593-602.
9. Divya Soniand Mihir V.Shah, " Review On Modified Gate Diffusiobn Input Technique" , International Research Journal of engineering And Technology(IRJET), vol.4 no.4,April-2017.
10. A. Morgenshtein, A.Fish and I.A. Wagner "Gate-diffusion input (GDI) - A power efficient method for digital combinatorial", IEEE Trans. VLSI Syst. pp.566-581, 2002.
11. A. Morgenshtein, A.Fish and I.A. Wagner., "Asynchronous gate-diffusion-input (GDI) circuits", IEEE Trans. VLSI Syst. pp.847-856, vol.12, no.8, 2004
12. Padmanabhan Balasubramanian and Johince John, " Low Power Digital design using modified GDI method", International Conference on Design and Test of Integrated Systems in Nanoscale Technology, IEEE, pp.190-193, September 2006
13. A. Morgenshtein, Alexander Fish and Israel A. Wagner, "Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 5, October 2002.
14. P. Prakasha,∗, K. Mohana Sundarama, M. Anto Bennetb "A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications", Renewable and Sustainable Energy Reviews, 2018, 194-203
15. Mehrabani YS, Mirzaee RF, Zareei Z, Daryabari SM. "A novel high-speed, low-power CNTFET-based inexact full adder cell for image processing application of motion detector. J Circuits System Computation 2017;26(05):1750082

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Priyanka Tyagi had obtained M.tech degree from MDU, Rohtak in 2011 in VLSI DESIGN. She had teaching experience in various reputed institutions like Manav Rachana University, Farid-abad, Priyadarshinicollege of computer sciences, Gr.Noida and ABESIT college of engineering, Ghaziabad. My research interest is in LOW POWER VLSI Circuits and NANO-ELECTRONICS.

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