Development of Multilevel Cascaded H-bridge Inverter Based Dynamic Voltage Restorer (DVR)

Bondili Saibindu Bai, Vinay Kumar Awaar, Jugge Praveen

Abstract: ***The objective of this study is to present the development of a dynamic voltage restorer (DVR) which employs a cascaded H-bridge multilevel inverter. DVR is a power electronic converter based on custom power device used to compensate for voltage variations. DVR does not need active energy storage systems like batteries as the zero energy compensation method is used. The control system may lead to challenges as compared with other DVR systems. To overcome this challenge a control method is used. In addition to minimize the delay of DVR and to mitigate the voltage sags, a three phase estimation method is used. The estimation method and control scheme is performed by using MATLAB/SIMULINK.***

Keywords: ***Cascaded H-bridge Multilevel Inverter Dynamic Voltage Restorer.***

I. INTRODUCTION

Power Quality is getting rapid growth day by day by utility as well as by both the commercial and the industrial electric users. Power quality has become very important in day by day aspect by increasing the no. of sensitive load in the power network. There are various kinds of power quality problems such as voltage swell, voltage sag, imbalance of the voltage and flickers [1]. Probably as it is said that the most common power quality problems i.e., is the voltage sags are affecting industrial and commercial customers. These sags are associated from the various faults on the power system. Energy storage capabilities of the uninterruptable power supply (UPS) becomes cost effective for higher power sensitive loads, in such situation dynamic voltage restorer (DVR) provides a cost effective solution [6].

DVR is employed to mitigate the voltage sag by the restoration of the dropped supply voltage to it's usual level and a series injection of voltages [3]. The fig.1 shows the DVR operation, to add the voltage to the supply when the sag is detected DVR uses series connected topology [8].

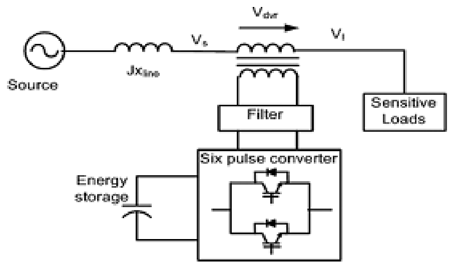

Fig.1: Schematic diagram of a typical DVR

The main aim of MLI is to approximate the sine-wave to step/ stair case wave form comprising several steps [7]. These steps which are fed from various D.C level can be supported by the series connected capacitors or battery-storage systems or any other type of renewable energy source like solar or wind units. Normally, multilevel inverter can be categorised into three different types as shown in fig.2.[10].

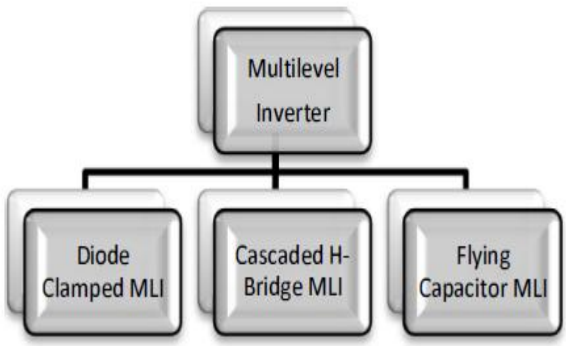

Fig.2: Various types of multilevel inverter

Unlike diode clamped inverters, CHB neither need any voltage clamping diodes nor capacitors for balancing the voltage like flying capacitors multilevel inverter. The main purpose of this paper is to decrease the total harmonic distortion by CHB MLI [5]. The models are simulated in Matlab for analyzing the results i.e., related to calculated total harmonic distortion (THD) of inverters.

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Bondili Saibindu Bai, M-Tech in Power Systems EEE department, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India. Email: bindu05bubby@gmail.com
Vinay Kumar Awaar, Electrical and Electronics Engineering department, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India. Email: vinaykumaar.a@gmail.com
Dr. Praveen Jugge, Electrical and Electronics Engineering department, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India.

Table 1: Comparison of components required for producing N levels using multilevel inverter.

MLI configuration	MLI topologies		
	Diode clamped	Flying capacitor	Cascaded H-bridge
Switching devices	2(m-1)	2(m-1)	2(m-1)
Freewheeling diodes	2(m-1)	2(m-1)	2(m-1)
Claping diodes	(m-1)(m-2)	0	0
Flying capacitors	0	(m-1)(m-2)	(m-1)(m-2)
DC-sources	(m-1) Dc supply or capacitors	(m-1) Dc supply or capacitors	(m-1)/2 Dc supply or capacitors

II. VOLTAGE COMPENSATION IN DISTRIBUTION SYSTEM-

DVR is specially power apparatus used for joining with VSI which pumps in voltage in series with power distribution system through series injection trans-former while voltages sag is present. A schematiic structure of DVR is as shown in fig.3. Energy source needed for DVR can be drawn through the ssupply source via bridge rectifier, which would make this design good price [2]-[4].

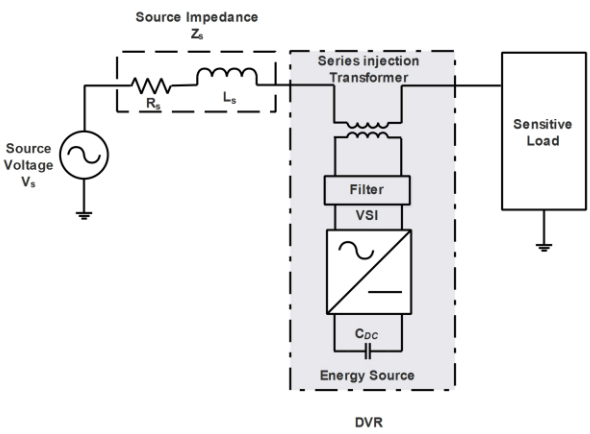

Fig.3: Representation of DVR

III. CASCADED H-BRIDGEINVERTER-

The development of several modified topologies resulted more attention in the direction of CHB MLI after 1997 though these inverters were appeared in 1988 and got older during 1990s. Many industries related to medium voltage high power drives use this sort of topology because of its PQ qualities and highly modular structure [11]. Cascaded H-bridge multilevel inverter is made of series connection of A.C terminal of single phase H_bridge inverter which has separate isolated D.C source as shown in fig.3. It is the basic circuit configuration of cascaded H-bridge inverter.

Fig.4 shows basic unit of cascaded H-bridge inverter which can be extended up to many levels by the addition of few more cells on each leg and the no. of levels can be found by

$$m=2n+1.$$

Where,

m = No. of levels.
n = No. of basic units in each leg of the inverter.

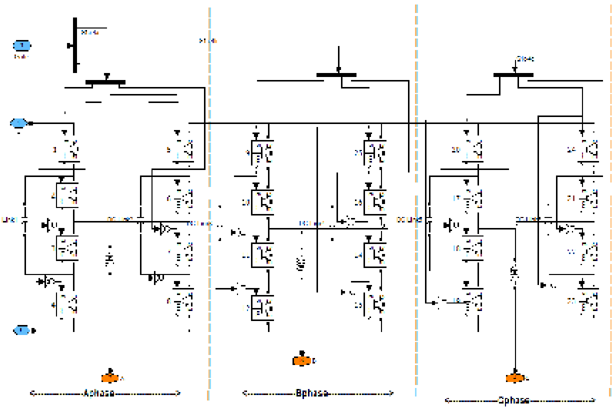

Fig.4: Three phase cascaded H-bridge multilevel inverter

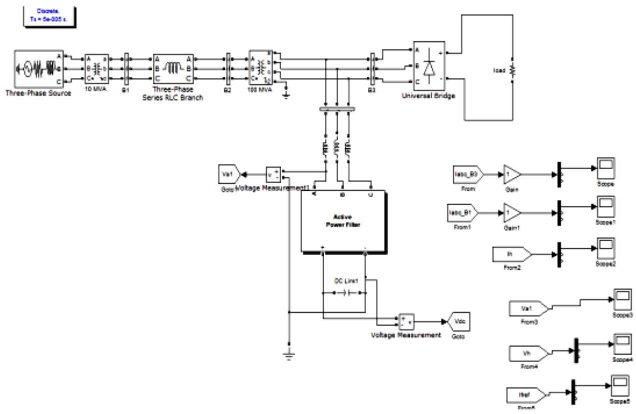

Fig.5: Matlab model of n-level inverter

IV. THE CHALLENGES OF THE MULTILEVEL INVERTERS AND ITS BENIFITS

The structure of the DVR that is utilized in this paper is as shown in the fig.5. DVR employs CHB MLI. This sort of change is extremely modular and produces voltage wave-forms and low THD. Different voltage and power levels can be extended due to series connection and also fault tolerant algorithms can be performed during the failure of power switches [1]. A cascaded H-bridge inverter with n number of Hbridge units is capable to synthesize 2n+1 level at it's A.C terminal. Because of this synthesized multilevel wave-form, the CHB inverter requires minute apparatus at it's out-put terminal to maintain total harmonic distortion with in applicable range and in addition the out-put filter leads to systems costs and lower losses due to reduction in size [9].

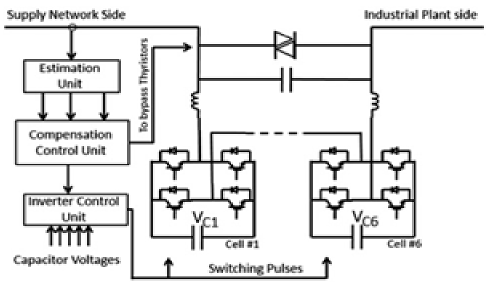

Fig.6: DVR structure (CHB based DVR)

V. VOLTAGE BALANCING ALGORITHM

This method states that the H-bridge unit is based up on their DC connection measured in volts at the initial state of each balancing period according to the fig.6. Operating most frequent number of each unit depend on it's degree in finding and the levels of voltage which are to be synthesized [1]. It is important to note that in the k^{th} division, voltage levels change between k-1 V_{CRef} & kV_{CRef}, where k=1, 2,…., n.

The voltage which is needed to be changes is selected for the operation in '+1' mode and the 'k^{th}' unit in pulse width modulation & the remaining in the 0mode if charging current is held with low voltage in k-1 units. Similarly, the voltage which is highest has to be sent out when the current is sent out by using the condition in '+1' mode and the k^{th} in pulse width modulation & remaining in zeromode..

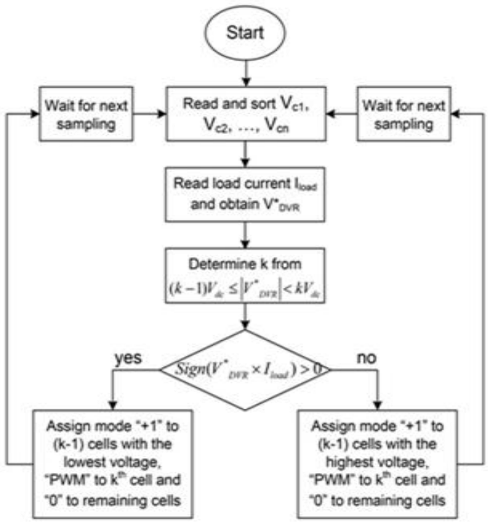

Fig.7: Flow chart of the balancing voltage algorithm in cascaded H-bridge inverter.

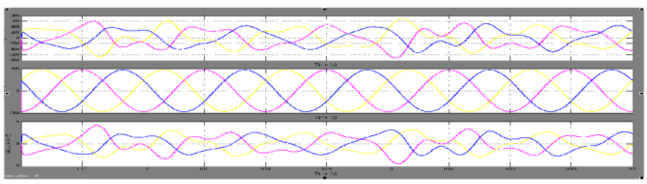

Fig.8: 3 phase voltage sag.

Network voltage
Injected voltage by DVR
Voltage at the load side

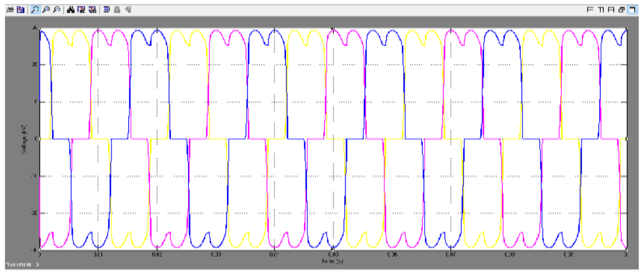

Fig.9: Unbalanced voltage sag at 20% sag on phase A

Total harmonic distortion of line voltages wave-form and phase voltages wave-form is done by using power-gui tool using sim-powersystems library and is also shown in fig.10. It can be analyzed that total harmonic distortion present in wave-form is 10.95%.

For the reduction of total harmonic distortion under the quality (standard) limit voltage levels are increased and the out-put wave-form is formed. In the same way line voltage can be determined and the analysis of harmonics can be performed using power-gui tool of MATLAB.

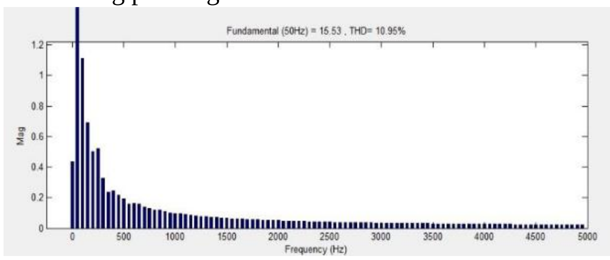

Fig.10: FFT analysis of three phase cascaded H-bridgemultilevel inverter.

VI. SIMULATION RESULTS

Line and phase voltages are analyzed and harmonic analysis is performed by the powergui tool in the simpowersystems library of Matlab and THD is calculated.

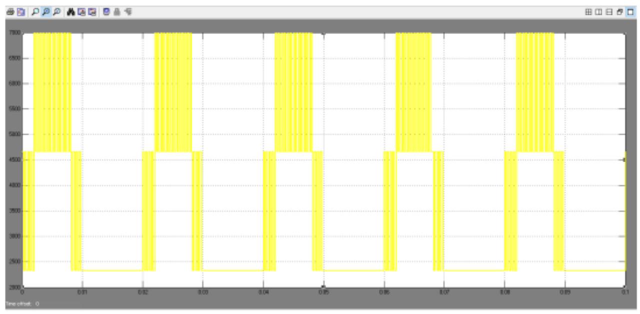

Fig.11: Voltage of the D.C. link capacitor

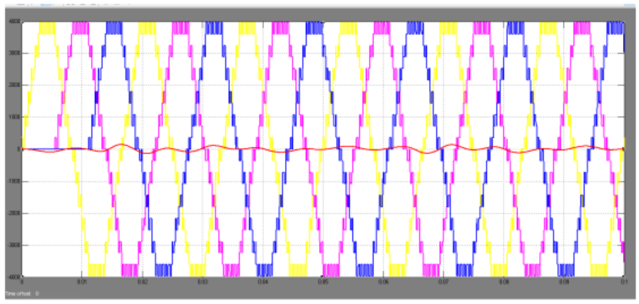

Fig.12: 3ph 20% voltage-sag with harmonic

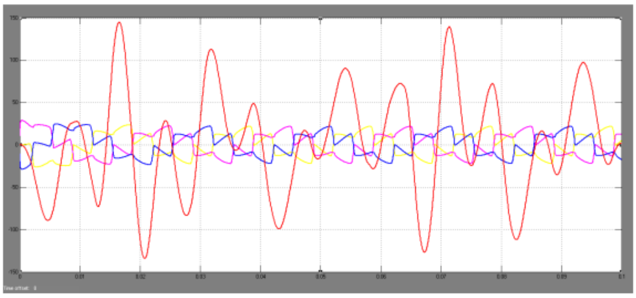

Fig.13: DVR AC terminal voltage (result of the simulation).

The three simulation orders of events are formed and done to assess the operation of new dynamic_voltage_restorer under different voltage-sags. List of simulation parameters is as shown in the Table.2.

Table 2: System parameters under simulation study.

Network	
Parameter	Value
network voltage	20 kV
load power	35 MW
load power factor	0.78 inductive
CHB converter	
voltage of DC link capacitor	1.33 kV
number of H-bridge cells per phase	6
line filter inductor	1.1 mH
line filter capacitor	90 μF
switching frequency	2 kHz

A 3ph balanced voltage sag with the depth of 20% which takes place at t = 0.2sec and stops/lasts up to 10 fundamental cycles. The supply voltage, the DVR voltage and the network voltage is as shown in fig.7. During the simulation, 20% of the voltage sag was given on the network voltage which was lasted for few cycles. The DVR voltage, load supply voltage and the network voltage are stated in fig.10. In addition, figure shows the seven levels DVR voltage along with the line current during the voltage sag.

VII. CONCLUSION

In this paper the operation of Dynamic Voltage Restorer and the design is based on the voltage sag is presented. Using a MLI, the offered Dynamic Voltage Restorer was able to directly connected to the medium level voltages networks with-out series_ injection transfermer. Because of losses in the internal system of Hbridge units and it probably errors in measurement, voltage of D.C links capacitor can be different, which keeps the operation of the inverter in proper way.

Inverters which are of higher level may be used in high/medium power applications which are applicable to electrical vehicle industries, power drives and it is most right form for the use of natural resources of energy like wind/solar. Here clamping diodes are not used, as the flying capacitor clamped and the diode clamped MLI. CHB multilevel inverter can be used as active power apparatus which are used to compensate voltage and current harmonics.

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AUTHORS PROFILE

Bondili Saibindu Bai M-Tech student in Power Systems (EEE), Gokaraju Rangaraju Institute of Engineering and Technology (JNTUH) , B.Tech from B. V.Raju Institute of Technology, Narsapur, bindu05bubby@gmail.com

Vinay Kumar AWAAR was born in India. He received his B.E. from Gandhi Institute of Technology And Management, Andhra Pradesh, India in 2003 and M-Tech from J N T U Kakinada, India in 2007. He is working as Associate Professor in the department of Electrical & Electronics Engineering at GRIET. Power Quality, Power Electronics, Electric Vehicles and Embedded Systems are his interesting areas of research work.

Dr. Praveen JUGGE has done Ph.D. in Power Electronics, Electrical Engg, from Osmaniauniversityy, Hyd. His interest research areas are Power Electronics and Power Quality. He published hundreds of papers in journals and conferences. He is a Senior Member of IEEE and working as a Professor at GRIET, EEE dept, Hyderabad, India.