

# Implementation of Efficient Architecture of Fine Grain Pipelined Lifting Scheme Based Two Dimensional Discrete Wavelet Transform



Anbumani V, Geetha V, Murugesan G

**Abstract:** Many Discrete Wavelet Transform (DWT) based VLSI architectures have been projected to meet the necessities of the synchronized signal processing. It includes image processing, speech processing, signal and video processing, etc. The practical implementation of DWT has fewer hitches in terms of hardware complexity and memory requirement since it needs to process huge volume of data. The traditional convolution based system needs more multipliers and larger memory and is also not suitable to provide speed or power efficient image or video processing designs. The lifting scheme involves very few mathematical computations compared to the convolution-based DWT. In this paper, we propose an architecture that performs Discrete Wavelet Transform (DWT) using a lifting-based scheme with fine grained pipelined architecture. The basic DWT filters used in image compression are 5/3(lossless) and 9/7(lossy) filters. In fine grain pipelining, multiplier is split into two units by placing the latches on the horizontal cutset across the multiplier. Thus the critical path is reduced to half of the multiplier delay. As a result, it is a speed efficient architecture and is symmetrical with a lower hardware complexity. The architecture is designed using verilog HDL and implemented on Xilinx Spartan 3E FPGA.

**Keywords:** DWT, lifting scheme, 5/3 filter, 9/7filter, fine grain pipelining.

## I. INTRODUCTION

Conversion of an image into digital representation and execution of some operations for the enhancement of the image and extraction of some useful information from that is possible with image processing. The source of input may be image or video frame or photograph and output may be image or it may have the associated characteristics. Image processing system treats images as two dimensional signals and processes them to obtain some significant data from an image. Image compression is one of the significant image processing techniques and is dropping the bytes of a graphics file size without corrupting the excellence of the image to a disagreeable level.

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The fall in file size permits more images to be accommodated in storage with the specified quantity of disk space or memory space. It furthermore diminishes the time needed for images to be sent and there are numerous methods in which image files can be compressed. The intention of image compression is to decrease insignificance and redundancy of the image data to facilitate storage or transmission of data in a well-organized form. Thus redundancy could be spatial, spectral or temporal redundancy. The correlation between the neighboring pixels provides spatial redundancy, the correlation among dissimilar color planes provides spectral redundancy and the correlation of order of image of different frames such as in video conferencing application provides temporal redundancy. The image compression techniques are commonly categorized into lossless and lossy depending whether or not an accurate model of the original image could be remodelled using the compressed form of image. Medical imaging desires lossless compression which is used only for a few uses with rigid requirements. Lossy compression technique aims to achieve high compression ratio by letting some adequate degradation in the image. Wavelets and filter banks have been used independently in image compression and signal processing. Fourier Transform (FT) cannot be used for the analysis of non-stationary signals which provides only the existence frequency components. Whereas Discrete Cosine Transform (DCT) gives the timing information and is a significant transform in 2D signal processing. Since DCT function is fixed and it cannot be adapted to source data there is undesirable blocking artifacts. Also DCT is block based and it neglects the pixels of the neighboring blocks and it is difficult to entirely decorrelate the blocks at their boundaries. Therefore, Discrete Wavelet Transform (DWT) is chosen for the proficient image compression standard JPEG2000. The data is decomposed into components of different frequencies which has both time and frequency components. By low pass and high pass filter analysis, the image is filtered initially through x axis and later the image is filtered in y dimension. Finally image is split into four sub bands namely HH, HL, LL, and LH. The present VLSI 2-D DWT architectures be able to classify into convolution-based designs [3]–[11] and lifting-based designs [12]–[32]. Few architectures sort from greatly parallel to programmable DSP-based architectures to folded architectures [16] and [17]. Among this, FIR filter banks are used in the implementation of convolution based architectures whereas factorizing the filter banks into more than a few lifting steps is adapted in the implementation of the lifting-based architectures [28].



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These architectures consist of strong arithmetic resource like multipliers, weak arithmetic resource like adders, few multiplexers, and minimum memory requirement. Reduction in computational complexity and increase in memory efficiency with increase in critical path is the net result with the lifting architectures.

To diminish the critical path of the lifting scheme flipping method is planned by Huang et al. [13]. To reduce the memory requirement many data scanning techniques have been proposed namely line-based designs, modified version of line-based designs, block-based designs and stripe-based designs.

The remaining sections of the paper are planned as follows: Section II analyses the mathematical grounds of the lifting design and the structure of 5/3 filter and 9/7 filter. Then, Section III describes the proposed fine grain method for 2D DWT architectures with 5/3 filter and 9/7 filter. Section IV analyses the performance of the intended design and the multiplier based architectures and in the end Section V concludes the work.

## II. THE BASIC CONSTRUCTION OF LIFTING SCHEME SUBMISSION OF THE PAPER

The essential steps in lifting scheme includes, Split step followed by Predict step and finally Update step. The basic construction of lifting scheme is given in Fig 1.

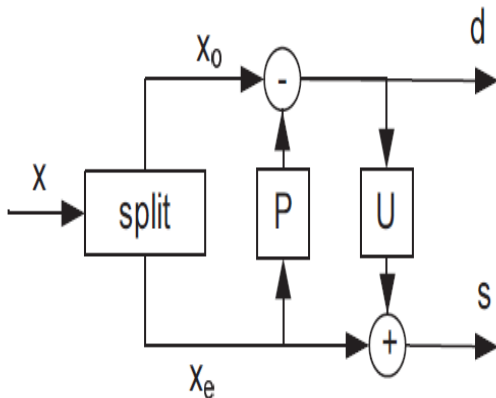


Fig 1. The Basic Construction of Lifting Scheme

In the split stage, signal splits into two disjoint sets of samples namely even indexed samples  $x_{2i}$  and odd indexed samples  $x_{2i+1}$ . This is shown in equation (1) and (2),

$$d_i^0 = x_{2i+1} \quad (1)$$

$$s_i^0 = x_{2i} \quad (2)$$

In the predict stage, the even subsets and odd subsets are combined. If the signal has local correlation plan, then the even subsets and odd subsets will be greatly related. This is shown in equation (3),

$$d_i^1 = d_i^0 + \alpha \times (s_i^0 + s_{i+1}^0) \quad (3)$$

In the update stage, the detailed samples will be restructured to the even sample. This is shown in equation (4),

$$s_i^1 = s_i^0 + \beta \times (d_{i-1}^1 + d_i^1) \quad (4)$$

### A. Basic Structure of 5/3 Filter

There are five taps in the low pass filter is and three taps in the high pass filter and hence it is (5, 3) filter. The basic structure of 5/3 filter is given in Fig 2.

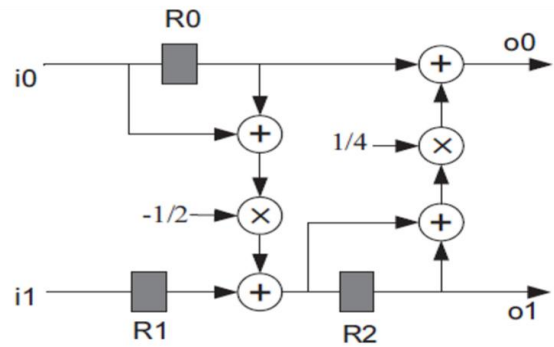


Fig 2. The Basic Structure of 5/3 Filter

### B. Basic Structure of 5/3 Filter

There are 9 taps in the low pass filter is and 7 taps in the high pass filter and hence it is (9, 7) filter. The basic construction of 9/7 filter is given in Fig 3.

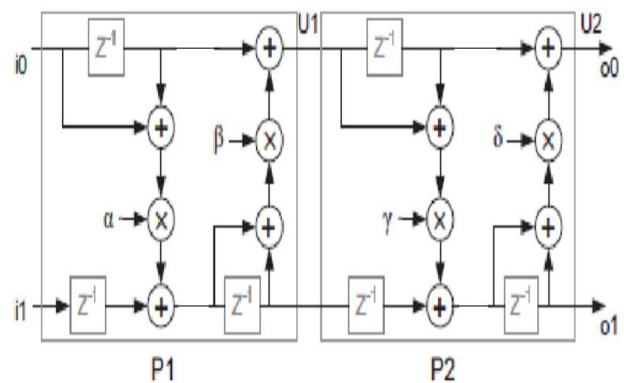


Fig 3. The Basic Construction of 9/7 Filter

## III. FINE GRAIN PIPELINING

Fine grain pipelining is a pipelining technique applied on multipliers. By placing the latches on the horizontal cutset across the multiplier, the architecture can be modified with the reduced critical path. Hence the desired speed can be achieved.

### A. Splitting methodology

Multiplier should be split such that minimum hardware should be used by each multiplier during implementation. Hence it should be power of 2. Considering the coefficient of the multiplier is 0.03125, it should be split such that  $m_1 = 0.125$  and  $m_2 = 0.25$ . By doing fine grain pipelining on the multipliers, the architecture is with the minimized critical path of  $(T_m)/2$ , where  $T_m$  is the multiplier delay.

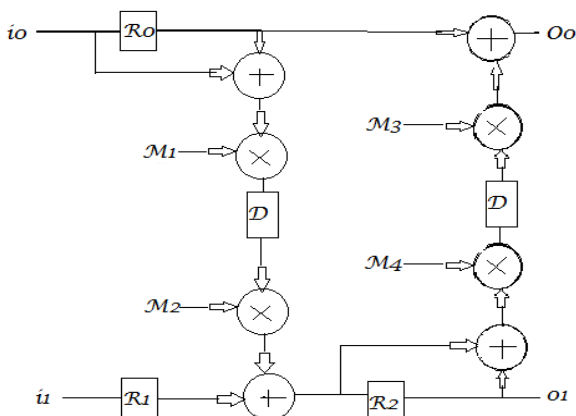
### B. Split Coefficients of 5/3 Filter

Table 1. Split coefficients of 5/3 filter.

Coefficient	In powers of 2	Split coefficients in powers of 2	Binary Representation of split coefficients
-0.5	-1	-0.5 & -0.5	10111010 10111010
0.25	-2	-1 & -1	00110010 00110010

**C. Modified 5/3 Filter**

The modified structure of 5/3 filter using fine grain pipelining is given in Fig 4. In Fig.4  $M_1, M_2, M_3$  and  $M_4$  are the split fine grain computational units of the multiplier in the conventional system.



**Fig 4. Modified structure of 5/3 filter**

**D. Split Coefficients of 9/7 Filter**

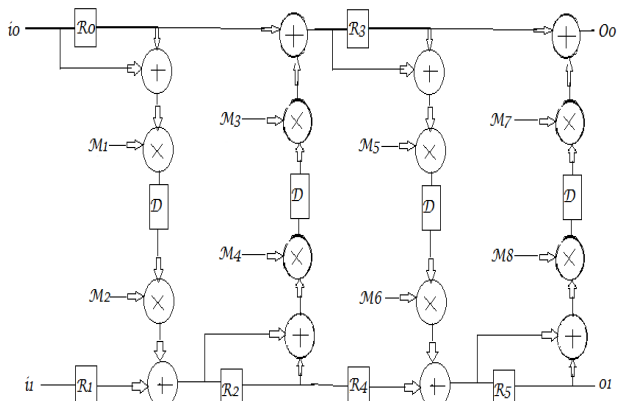
The coefficients of 9/7 filter are  $\alpha = 1.586134342$ ,  $\beta = -0.052980118$ ,  $\gamma = 0.8829110762$ , and  $\delta = 0.4435068522$ . The coefficients are split based on the power of 2. Split coefficients of 9/7 filter by fine grain pipelining is given in table 2.

**Table 2. Split coefficients of 5/3 filter**

Coefficient	In powers of 2	Split coefficients in powers of 2	Binary Representation of split coefficients
1.58	0.6599	-0.09 & -0.74 99	01011101 & 10101000
0.05	-4.321 9	-0.09 & -4.23 19	01011101 & 11111011
0.88	-0.184 4	-0.09 & -0.09	01011101 & 01011101
0.44	-1.184 4	-0.09 & -1.09	01011101 & 00101110

**E. Modified 9/7 Filter**

The modified structure of 9/7 filter using fine grain pipelining is given in Fig 5. In Fig.5  $M_1, M_2, M_3, M_4, M_5, M_6, M_7$  and  $M_8$  are the split fine grain computational units of the multiplier in the conventional system.



**Fig 5. Modified structure of 9/7 filter**

**IV. RESULT AND DISCUSSION**

**A. Comparison of Hardware Complexity**

The hardware requirement for the implementation of conventional 2D DWT design with convolution scheme and lifting scheme based 2D DWT are reviewed in terms of multipliers/ shifters and adders essential for implementation. The Table.3 shows the number of multiplication operations, addition operations and shift operations necessary for (5, 3) and (9, 7) for both convolution and lifting methods.

**Table 3. Hardware requirement for convolution and lifting 2D DWT [8]**

Filter	Multiplication/Shifts		Additions	
	Convolutio n	Liftin g	Convoluti on	Lifti ng
(5,3) Lossless	4	2	6	4
(9,7) Lossy	9	5	14	8

From the Table.3, the lifting scheme will be more appropriate for hardware implementation of DWT with lesser computational intricacy, less area and minimized power. With the intention of showing enhancement in the speed of processing, utilization of fine-grain pipelining has been planned. By using this method, the multiplier unit present in the critical path of the circuit is broken into finer pieces.

**B. Performance Comparison of 2D DWT 5/3 Filter**

The 2D DWT lifting scheme based 5/3 and 9/7 filter structures and fine grain pipelined architectures were designed using verilog HDL and implemented on Xilinx Spartan 3E FPGA. The power and delay of the conventional 2 D DWT lifting scheme and the fine grain pipelined architecture of 2D DWT architectures were given in Table 4.

**Table 4. Comparison of power and delay of the 2D DWT with 5/3 filter using conventional and fine grain pipelined techniques**

Name of the 2D DWT lifting architecture	Power ( $\mu$ W)	Delay(nS)
Using conventional technique	393.57	15.32
Using fine grain pipelined technique	276.80	13.55

The power reduction of 29.67 % and delay reduction of 11.55% is achievable with the fine grain pipelined design and the conventional design of 2D DWT architecture with 5/3 filter.

**C. Performance Comparison of 2D DWT 9/7 Filter**

**Table 4. Comparison of power and delay of the 2D DWT with 5/3 filter using conventional and fine grain pipelined techniques**

Name of the 2D DWT lifting architecture	Power ( $\mu$ W)	Delay(n S)
Using conventional technique	769.09	22.56
Using fine grain pipelined technique	507.85	16.004

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The performance comparison of fine grain pipelined design and the conventional design of 2D DWT architecture with 9/7 filter shows the power reduction of 33.97 % and delay reduction of 29.06% .

## V. CONCLUSION

High speed architecture for lifting based 2D DWT using fine grain pipelining is proposed.

In this method, the critical path is reduced to  $T_m/2$  and hence the speed of the architecture is increased. The modified lifting algorithm has a minimum critical path. Hence the fine grain pipelined architecture has a good hardware efficiency, lower complexity and increased speed.

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