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Design and Simulation of Low Power Consuming Digital Controlled Oscillator in All Digital Phase Locked Loop

SudhakiranGunda, Ernest Ravindran R. S.

Abstract:Recent IC technology innovations can achieve lowpowe r biomedical implant functionality.RF transceivers require low-power and small-sized components in biomedical implants to achieve the best results in frequency and phase control. Phase Locked Loop (PLL) is the key component for controlling these parameters in low power consumption RF transceivers. Therefore All Digital Phase Locked Loop (ADPLL) is chipping effectively into a major role in the fields of Biomedical & Communication. ADPLLs contribute better results in these areas due to their efficient blocks. This paper focuses on the design of low-power Digital Controlled Oscillator (DCO) and provides information on the various ADPLL blocks. To reduce power dissipation DCO is designed with XNOR gate using delay elements by avoiding direct contact between VDD & GND and the MOS transistors were arranged in ring topology. Tanner tools were used to design and simulation. In addition to this it also provides the detailed history of PLLs & ADPLLs and their mathematical analysis. Compared to previous design, the current DCO design gives better power consumption results.

Keywords: PLL, ADPLL, DCO, XNOR.

I. INTRODUCTION

From the past decade the usage of biomedical implantable devices is enormously increasing because of their flexibility in monitoring and caring the dear ones. This is due to the improvements achieved by the technologies in nanotechnology and wireless technologies. These made the medical diagnosis, monitoring and intervention into personal care in the form of e-care, m-health, self-care and Internet of Things (IOTS) [1]. For happening of all these cases, the Implantable Devices (IMD) has to be inserting safely & securely to stay in the body over a period of time; thus it raises a new expectation for IMDs that the implant need to communicate between body parts and external units for a real-time sensing and treatments. To achieve all these facilities IMDs need a sufficient power source. To power IMDs there are several approaches, this can be majorly divided into two types. They are independent systems like battery approach to power IMDs and another one is System with a transferring mechanism or System with a external unit like inductive coupling [1, 2].

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***** Correspondence Author
SudhakiranGunda *, Research Scholar, Assistant Professor, ECE Department, K L University Campus, Vaddeswaram Village, Andhra Pradesh, India..
Dr. Ernest Ravindran R. S., Assistant Professor, ECE Department, K L University Campus, Vaddeswaram Village, Andhra Pradesh, India.

Biomedical radio frequency (RF) transceivers require itsy-bitsy forms with a minimum battery usage and energy efficient [3]. These forms of implantable devices are more preferable for high biocompatibility applications [4]. Signal propagation frequency in the human body lies in the "Medical Implant Communication Service (MICS) band frequencies" ranging from 401 to 406 MHz (intra range is 402 to 405 MHz) and facilitates a happy medium between chip-size and power consumption. So MICS band frequencies are widely used for biomedical RF transceivers [5, 6]. Designing of RF transceivers front-end in biomedical implantable devices is a tough task because they require extremely subjacent power devouring, tiny in size, itty-bitty external components and high fidelity devices. Usage of few additional components offers higher fidelity, low cost, and small size for medical implantable devices. The front end schematic diagram of biomedical RF transceiver in medical implantable devices is shown in Fig 1.The working details of this block diagram given in the study of ADPLL in Biomedical RF transceivers [4]. The performance of Fig 1 depends on local oscillator (LO) signal, so Frequency synthesizer is one of the critical blocks in RF front-end part of medical implantable devices. Hence there is a need for best frequency synthesizing in RF front end part which can be achieved from PLL.

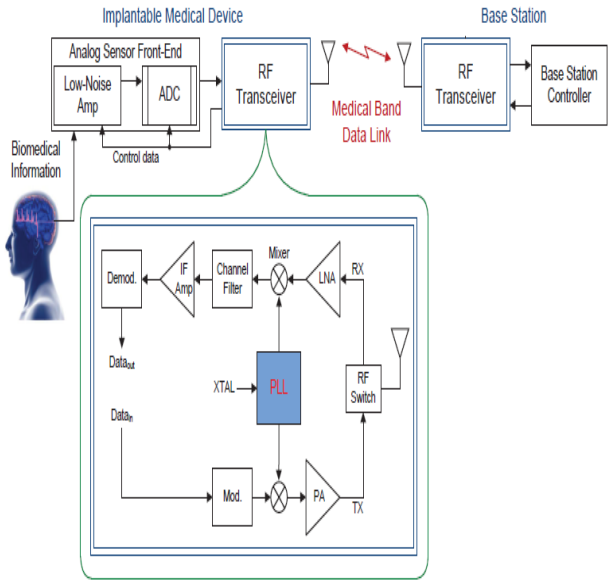

Fig 1: Schematic representation of RF front-end transceiver in medical implantable devices

II. PHASE LOCKED LOOP

A signal in Phase Locked Loop (PLL) corrects itself without the external help hence called a self-correcting control system. PLLs are of 4 types: they are 1) linear/analog PLL 2) Digital PLL (DPLL) 3) All DPLL 4) Software PLL [7]. Linear PLLs using CPs are still widely used, but ADPLLs sweep off one's feet due to their compelling benefits over their analog counterparts [3,8-10]. The analog PLL brief out is given as follows: Understanding the block diagram of PLL is very essential [8] to know its performance at various frequencies and phase values. Major blocks in PLL are phase/frequency detector, amplifier/LPF, VCO. [4].

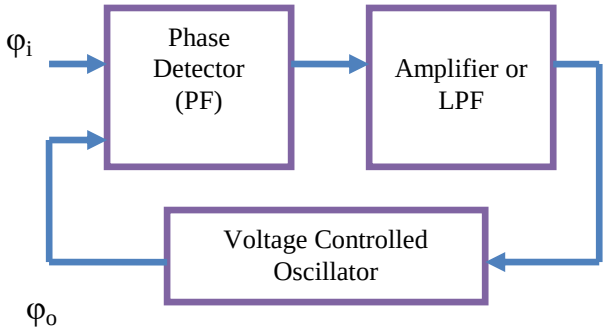

Fig 2: Block diagram of PLL

A. Mathematical analysis

The output frequency of VCO in PLL is given as

$$\varphi_o = \frac{A_o k_{pd}(\varphi_i - \varphi_o)k_{vco}}{\left(1+\frac{S}{\omega_{lp}}\right)S} \quad (1)$$

Where A_o– Sensitivity of amplifier gain
k_{pd}– Phase detector sensitivity
k_{vco}– VCO sensitivity
ω_{lp}– LPF cutoff frequency

The DC open loop gain of the system is

$$k_l = k_{vco} A_0 k_{pd} \quad (2)$$

The Laplace equation of the open loop gain is

$$\frac{K_{pd}A_0K_{VCO}}{S} \quad (3)$$

Closed loop transfer function of PLL control system is

$$\frac{\varphi_o}{\varphi_i} = \frac{1}{1+\frac{S}{k_l}+\frac{S^2}{\omega_{lp}k_l}} \quad (4)$$

If DC loop gain is high then equation 4 becomes $\varphi_o = \varphi_i$or the change in output phase follows the change in input phase thus the phase is locked. The word '$\omega_{lp}k_l$' in the equation 4 is a natural frequency of the system (ω_0) and equals to

$$\omega_0 = \sqrt{k_l \omega_{lp}} \quad (5)$$

$$\frac{\varphi_o}{\varphi_i} = \frac{1}{1+\frac{S}{\omega_{oQ}}+\frac{S^2}{\omega_o^2}} \quad (6)$$

Where $Q = \sqrt{\frac{k_l}{\omega_{lp}}}$ (7)

Linear PLLs are very bad about temperature drift, liable to be influenced to the change of voltage, high noise & high responsive towards process parameters [3, 8, 9, 11]. DPLLs are in superior positions regarding performance, speed, reliability and reduction in size and cost and also solve many problems of linear PLLs [3]. Analog phase locked loops require the initial calibrations and periodic adjustments [3] but DPLLs are not required to protect from sensitivity of the Voltage Controlled Oscillator (VCO), temperature & voltage variations. Problem of sensitivity to DC drifts does not exist in DPLLs. Fast locking speed is present in DPLLs because of the analog LPF and analog multiplier in Phase Detector (PD)[3]. All these can be achieved in DPLLs are because of advancements in CMOS technology.

DPLLs are categorized as Uniform sampling DPLLs and Non-uniform sampling DPLLs based on the process of sampling [3]. The detailed block diagram of DPLL is given in [3, 7].Based on the phase detector function again DPLLs are classified as

1) Flip-Flop DPLL, 2) Nyquist-rate DPLL, 3) Lead-lag DPLL (LL-DPLL), a.k.aBinary Quantized DPLL, 4) XOR DPLL and 5) Zero-Crossing DPLL (ZC-DPLL)[12].

ADPLL provide low-voltage operation compatibility under process and temperature variations with a curtailed system turnaround time [13]. Therefore, ADPLL provide several benefits to duty-cycled battery-operated systems, including MICS transceivers, wireless sensor nodes, and wireless telemetry devices. Realizing a low level of spurs and high-resolution is a challenge to achieve fully integrated high performance ADPLL architecture.

III. ADPLL ARCHITECTURE

The general ADPLL (a fully digital PLL) architecture consists of different blocks like Digital phase detector, digital loop filter and DCOas shown in Fig. 3 which are helpful to achieve the desiredqualities. The input signal(s) is/are digital(binary) with a single bit or a vector (combination of all digital signals).

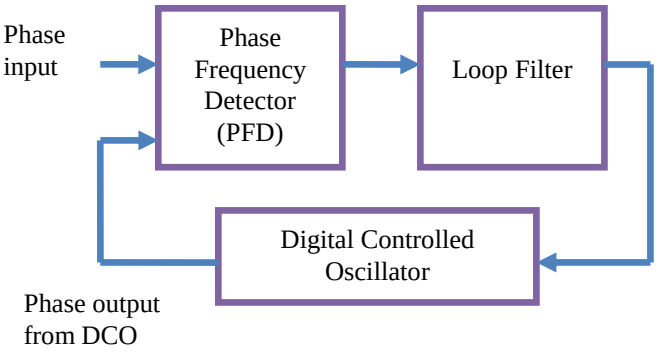

Fig 3: General ADPLL block diagram

The digital phase frequency detector (DPFD) internally has mechanism of digital phase detection (with phase accumulation and phase detector digital addition) and frequency/time to digital conversion (TDC/FDC). The output of DPFD is the comparison signal of the phases between the bit-stream representations of frequency ratio and the output from TDC which further processed by digital loop filter to provide a suitable signal for DCO.

Based on application the DCO in ADPLLs may be a combination of DAC & VCO or simply a DCO which produces a frequency output for FDC/TDC. The frequency synthesis in ADPLL is decided by the DCO output signal phase. Hence designing of DCO/TDC is the main task for the designers in ADPLL.Best architecture is possible when the designer completely knows about every block. Hence there is a need to study different blocks in ADPLL. Table 1,2 and 3 give the detailed information about PFDs, LFs & DCOs.

Table I Comparison of phase detectors

Sl.No	Phase Detector		
	Types	***Advantages***	***Disadvantages***
1	DETDFF	Low power consumption and high speed – phase locked state. [14]	Compound structure [14]
2	EXOR	Error pulse on both the edges [15]	Hard to edges. Loss of data. Phase error range is -90^o to +90^o. Less range of phase tracking[15]
3	JK Flip Flop	Hung up to edges implies little data loss. [15]	Phase error range is -180^o to +180^o. High range of phase tracking[15]
4	Phase Frequency Detector	Phase error range is -360^o to +360^o. High range of phase tracking. Possibility of locking at any instance. [15]	Labyrinthine structure [16]
5	Flip-Flop Counter	Higher bit possibility. [16]	Circuit complexity & requires triple input frequency [16]

Table II Comparison of Loop Filters (LF)

Sl.No	Loop Filter		
	Types	***Advantages***	***Disadvantages***
1	K counter	Prefect integrator [15].	Works only with XOR & JK Flip Flop PFDs [15]
2	Up/Down Counter	Easily coagulate with other PFDs [16]	Exactness of integration is less [15]

Table III Comparison of Various DCOs

Sl.No	DCO		
	Types	***Advantages***	***Disadvantages***
1	Increment – Decrement Counter	Mastery over Hold & Lock range [15]	Software implementation is not possible [15]
2	Divide by N counter	Lucid architecture [16]	No Jitter design concept [16]
3	Bootstrapped DCO	High linearity & resolution [17]	Heavy architecture [17]

With reference of the Table I, II & III it is known that the speed and power dissipation of ADPLL majorly depends on the architecture of DCOs. The present paper deals with the design of DCO with a novel three transistor XNOR gate which are connected in ring topology [9]. Switch networks were added for digital control of oscillator.

IV. RESULTS AND DISCUSSION

A. Circuit Description

Delay cell with NMOS switching network is shown in Figure 4 consists of 3-bit NMOS switching network, CMOS inverter and NMOS controlling gate between inverter and switching network; in detail M1, M2& M3 constitute a 3 transistor XNOR gate which acts as an inverter since M2 transistor input is always zero and produce the delay required for the DCO. The Transistors M4, M5, M6 & M7collectively produce switching network activities for DCO operation. These were operated with different widths and provide various resistance values according to bit pattern variations in the circuit operation. Next paragraph gives the width details of PMOS (M1) & NMOS (M2) gates in inverter and NMOS (M4, M5, M6 & M7) gates in switch network and controlling NMOS (M3).All MOS gates switching characteristics depends on the gate source voltages (V_{gs}) and drain source voltages (V_{ds}) as for N channel gates $V_{gs}>V_{th}> 0$ &$V_{ds}> 0$ and for P channel gates $V_{gs}<V_{th}< 0$ &$V_{ds}< 0$ where $V_{th}$is threshold voltage.In the previous work [5] the circuit simulated in 180nm technology and the present paper works on 150nm technology. In the switch network binary weighted NMOS & PMOS devices were used and delay of that stage is controlled by them. Device geometries are varied for technologies; in general width of PMOS & NMOS devices depends on feature/die size. The width of NMOS is 4 to 6 times of feature size while PMOS is 2 to 2.5 times of the size of NMOS widths. But based on the requirement the geometric values may changes but fall into this analysis mostly. The width sizes of transistors in the delay network areconsidered based on the formulae 2^{n-2}X1 for PMOS and 2^{n-3}X0.5 for NMOS where 'n' represents the device number. For example PMOS2 has the width 1 µm and PMOS5 has the width 8 µm similarly NMOS3 has the width 0.5 µm.But in the inverter circuit the width of PMOS is 1.0 µm and for NMOS (M1) is 2.5 µm, NMOS (M2) is 0.5 µm due to based on the requirement. The simulation circuits and results of DCO are as follows:

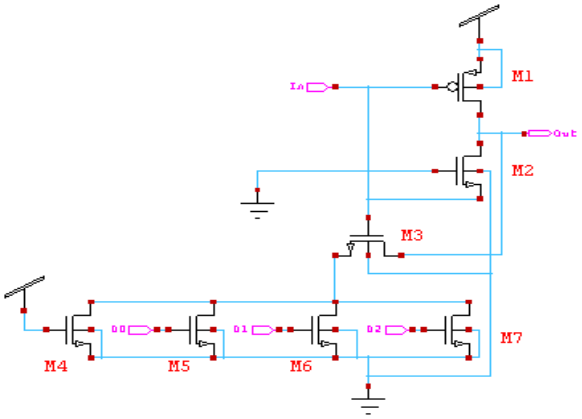

Fig 4: DCO With Single Delay NMOS Cell With Three Control Bits.

Delay cell with PMOS switching network is shown in Figure 5 consists of 3-bit PMOS switching network,

CMOS inverter; in detail M5, M6, & M7 constitute a 3 transistor XNOR gate which acts as an inverter since M6 transistor input is always zero and produce the delay required for the DCO. The Transistors M1, M2, M3 & M4collectively produce switching network activities for DCO operation. These were operated with different widths and provide various resistance values according to bit pattern variations in the circuit operation.

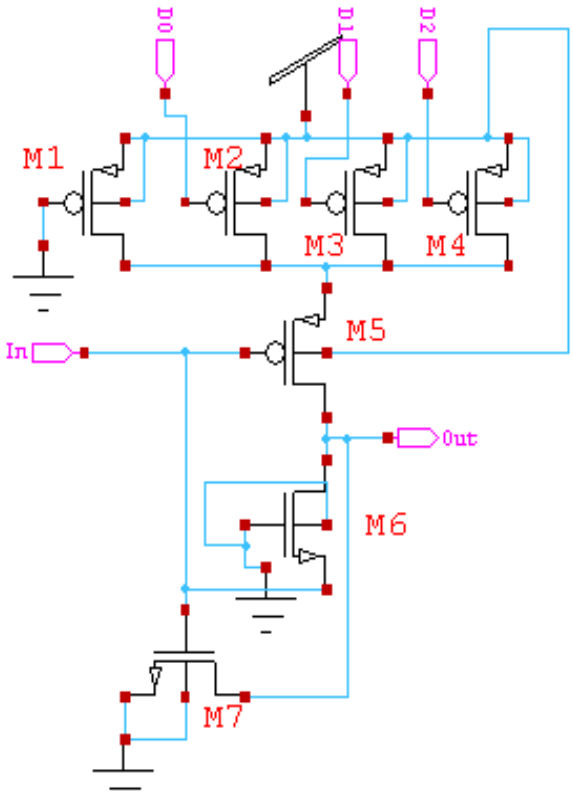

Fig 5: DCO with single delay PMOS cell with three control bits.

With this mechanism in Figure 4 & 5 the proposed delay cell, upgrades the circuit in delay modeling and frequency components. Power dissipation in the delay cell is also reduced because of the elimination of short circuit path between the power supply (V_{DD}) and ground (V_{SS}).Because of unequal widths of transistors the equivalent resistance of the circuit changes regularly which affects the speed of the circuit. Need of the bits in the DCO depends on frequency tuning [9]. The transistors M4 and M1 in the Figure 4&5 are connected to V_{DD}& GND respectively to provide a way for current conduction. The performance of the above circuits in terms of power consumption, resistance of the network and processing time will vary with control bit pattern. Power consumption and processing time of MOS cell is given in table 4 & 5. The advantage of the proposed delay cell is, extend to any number of bits in the switching network without effect of power dissipation, processing time and frequency analysis.In the NMOS switch network the resistance value of DCO is reduced with bit pattern variation (000 to 111) and the average circuit processing time for all the bit patterns is 1.87sec given in Table 4.Where as in PMOS switch network the resistance value is modulated with bit pattern variation from (000) to (111) and the average processing time is 2.02 sec given in Table IV. Power consumption comparison with the earlier report is presented in Table V.

Table IV Performance of single delay NMOS cell

Control bits $D_0D_1D_2$	Power consumption (µW)	Processing time (seconds)
000	8.228	1.97
001	8.312	1.85
010	8.299	1.74
011	8.318	1.97
100	8.287	2.14
101	8.316	1.96
110	8.309	1.42
111	8.321	2.10

Table V Performance of single delay PMOS cell.

Control bits $D_0D_1D_2$	Power consumption (µW)	Processing time (seconds)
000	77.61	1.60
001	75.10	2.37
010	76.80	2.19
011	69.53	2.12
100	77.27	1.61
101	73.37	2.40
110	76.16	1.89
111	56.47	2.00

The DCO shown in figure 6 was constructed and simulated using Tanner tools in 150nm technology and the operation of the circuit is as follows: 3 delay cells with 3 control bits consists of a switch network with 4 NMOS transistors. Binary weighted transistors were used in the design with the first NMOS gate terminal connected to VDD supply for current conduction path. Remaining 3 NMOS transistors are connected to D_0, D_1& D_2 control bits. Number of bit requirement decides by frequency tuning range. The proposed circuit can be extended to a range of 6 bits and have a limit due to circuit complexity issues [18]. In an extension; i.e. 6-bit DCO (D_0 to D_5) should connect to weighted NMOS transistors.

3-Bit DCO

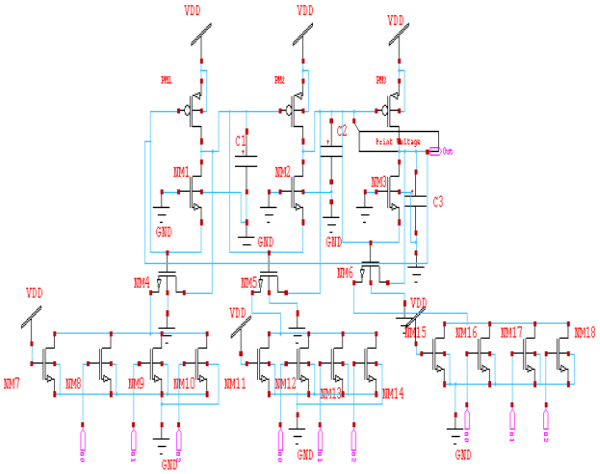

Fig 6: 3-bit DCO connected in ring topology.

B. Simulation results

The NMOS switch network simulation results for different control bit patterns is shown in Fig. 7.

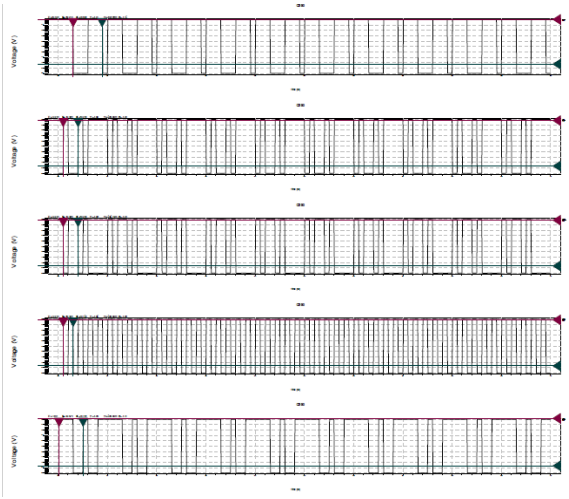

Fig. 7: Simulation results of single delay NMOS cell

Voltage (V) v/s Time (nsecs) graph obtained in three stages, the 1st part in the waveform is obtained at first stage of DCO circuit which provides less range of frequency [1.3 to 1.67 GHZ]. The 2nd part explains the output at second stage which gives the moderate frequency range [1.25 to 1.67 GHZ]. The 3rd part is at the output stage of proposed DCO which gives the best range of frequency for bio-medical applications [1 to 1.6 GHZ] shown in Fig 8. The power consumption for the proposed DCO structure, minimum power consumption is 6.813005e-003W at time 6.2e-007 Sec, the maximum power consumption is 6.817266e-003W at time 6.1e-007 Sec and the average power consumed for all combination of bits in DCO is 6.815116e-003W. Comparisons with different circuits are listed in table VI.

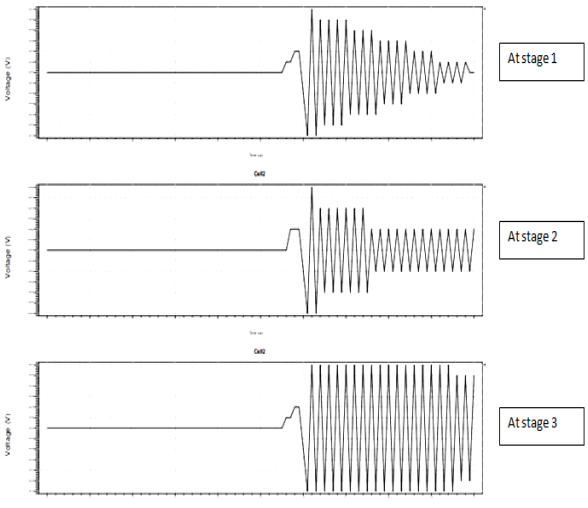

Fig. 8: Simulation results of 3-bit DCO

Table VI Comparison with the previous architectures

DCO architecture	Power dissipation in mW	O/P frequency in GHz	Technology (µm)
Ref [19]	63.4	.333-1.47	0.35
Ref [20]	-	1.35-4.55	0.18
Ref [21]	2.3	0.57-0.85	0.032
Ref [22]	5.4	0.08-0.25	0.18
Ref [23]	25	1.2	0.6
Ref [24]	2.2	0.57-0.80	0.032
Ref [25]	-	0.75-1.60	0.5
Ref [26]	-	2.4	0.13
Ref [27]	-	3.4-5.6	0.13
Ref [28]	30	4.89-5.36	0.18
Ref [29]	9	8.79-9.17	0.18
Ref [9] NMOS	0.251-0.276	1.61-1.87	0.18
Ref [9] PMOS	0.274-0.227	1.86-1.55	0.18
Present work NMOS	0.008	-	0.15
Present work PMOS	6.8	1.0 -1.6	0.15

V. CONCLUSION

Block diagram of PLL & ADPLL with mathematical analysis and types of implementations of different blocks in ADPLL has been conferred. A comparison table of different blocks in ADPLL is made known. The architecture for delay cell with bit control (NMOS & PMOS) and DCO are entrusted in this paper. It shows better reduction of 35% in power dissipation compare with the previous delay cell circuit by eliminating the direct contact between V_{DD} and GND.

FUTURE SCOPE:

The processing time is little bit more when compared with the previous architectures which can be reduced by considering the advancements in IC technologies.

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AUTHORS PROFILE

Sudha Kiran Gunda, born in Bethamcherla, Andhra Pradesh, India in 1989. He received Bachelor Degree in Electronics and Communication Engineering from JNTUA Anantapuramu, India in 2011 and M.Tech Degree in VLSI SD from JNTUA Anantapuramu, India in 2013. He is currently working towards Ph.D in VLSI domain at K L University, Guntur, A.P. India. His current research interests focus on low power, high performance CMOS digital ICs.

Dr. R. S. Ernest Ravindran received his PhD from Anna University, Chennai, India. He did his Masters in Nanoscience and Technology from Anna University, Trichy, India where he established surface coated CdS quantum dots as a luminescent probe for silver ion detection. His field of research involves Nano Composites (ceramic-polymer) for high energy storage application, green synthesis of metal nanoparticles in bio-medical applications. He is currently working as assistant professor at K L E F(Deemed to be University) Vaddeswaram, Guntur, Andhra Pradesh, India..