Effective Network Interface Architecture for Fault-Tolerant Mechanism Network-on-Chip

KodaliRadha, Kasukurthi Ramakrishna, KrishnaveniGuduru

Abstract: ***Basically, the denser integration capabilities will enable silicon technology scaling continuously. But in silicon technology higher variability and susceptibility will obtain. In this paper an effective network interfaces architecture if introduced for fault tolerant mechanism network on chip. A chip multi processor is introduced on chip components but this processor will not give effective output. Hence, the introduced system gives high throughput in modern network on chips. This system will exploit the speed of appropriate wire engineering which will transfer the long distance in single clock cycle. The data will be transferred between NOC routers by using Network interface (NI) and IP cores. Hence the proposed architecture will save the life time and overcome the issues of previous system.***

KEY WORDS: Network Interface (NI), Integrated circuits (ICs), Network on Chip (NoC), Chip multi processor (CMP).

I. INTRODUCTION

In multi core environments, network on chips establish a dominant communication. It produces the scalability for attributing communication in effective way. In modern scaled system, extra intellectual properties should be generated. Here the source to destination hop count will increase the network effectiveness. Various core realms will be provided in network on chip to get high throughput and low latency. High radix networks with long connecting links will allow the system to transverse the multiple network hops in single clock cycle. The complexity of integrated circuits will dramatically increases in CMOS technology [1]. The overall system performance will limit the wire delay. To meet the requirements of system on chip, the given requirements are not suitable. The new solutions are needed to overcome the architectural and physical issues.

The system on chip will distribute the clock signals and balance wire delays, but mainly suffers from capability, flexibility and modularity problems. Hence to overcome this network on chip will be introduced. This network on chip will distribute the clock signals and balance wire delays.

In some cases the system on chip will give physical issues this will be overcome by the NoC architecture. By using advanced techniques wide delay effects will be reduced. To get better communication for network on chip, interconnection of IP components are used [2]. Different IP interconnects are used in globally asynchronous locally synchronous paradigm. This will operate at different frequencies on the same chip.

In future GALS NOC architecture is used in mesosynchronous communication technique is used. This technique will mitigate the wire delay effects. Earlier various GALS based inter connection systems are used [3].

The GALS paradigm is used inside the Noc system using different approach. To connect the IP components asynchronously, a clock less network is used. After interconnecting IP components different clock signals are generated locally. This system is attractive and applicable to concern some type of difficulties. In the design of self timed circuits non standard cells are used which is non trival in condition. In this the timing verification is not reliable [4].

In present generation, clock less network on chips are used to evaluate the alternatives. Here IP components and clock speed is determined in the boundaries of clock domain to employ the synchronization. Some benefits are introduced in network on chip that will mitigate the physical issues. These physical issues are obtained due to wire delay effects in the network.

In this paper we introduced the design of fault tolerant mechanism for network on chip. This effectively implements the data link layer of network stack. Physical service is provided by the network interface for IP components. This system will achieve maximum throughput, low latency and full robustness against the clock skew. The proposed system will overcome the issues of chip multi processor. Basically, in standard design flow of SoC designing & verification is complex. This process will suffer from some issues. Hence proposed system is introduced, this system will control the flow and full duplex communications [5].

By using multi core chip and network, the faulty tile in system is isolated. This system will operate the system to give reduction in performance. The fault is spread in backward that will quickly congest the possible deadlocks. Here transverse faulty links will affect the transit messages in entire system. By using small resistance and capacitance values, the feature size will shrink. By understanding the electro migration and stress which is induced in on chip metal interconnect reliability process. Here there will be reduction in current densities and electro migration will increase the metal layers in effective way.

Being unique to the channel, the realized application diversions have huge modernized signaling method. Furthermore, isolation is a kind of sign system, the characteristic of channel strategy is camouflage or lacking in some part of the sign. Along these lines, in the excitement of no one stressed in the style of electronic circuit, it has the

Revised Manuscript Received on May 29, 2019.

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versatility to make the filter circuits are adapted to the social problem in a particular line of action subtleties. In the sign method, an electronic channel is a device or system that eliminates any unwanted or characteristic segment of a sign. Propulsion channels are used for 2 general purposes; plot of sign that unites, and recovery of sign that has been ruined in some philosophy. Routine, it is proposed to eliminate a pair of frequencies and not others to cover the sign of the level of the intrusion signal and the configuration.

This parallel allocation is abused to adapt to internal disappointment. In all honesty, reliability can be a vital test for the electronic structure. in particular, sensitive slips are a critical problem and many strategies are organized over time to mitigate them Send feedback History Saved Community.

Some of these systems change the low level style and the execution of the planned circuits to avoid the appearance of sensitive sprays. The different procedures address the level of thought that accompanies it by including the redundancy that you will observe and the real problems. The protection of mechanized channels has been widely analyzed. for example, fault-tolerant executions have maintained the use of development grouping systems or design codes have been devised. the use of a reduced precision replica or a word level confirmation has been further criticized for another option to execute the fault amendment consisting of using 2 executions of absolutely exceptional deviations in parallel. Each of these images focuses on the security of a channel. The bumble encoding is used for non-tolerant management in the PC memory, the captivating and optical information accumulated by the media, satellites and commercial parties, organizes coincidences, remote frameworks, and for all intents and purposes some other kind of automated correspondence.

Writing Fault uses bits of scientific data to code the origin into longer words for the transmission equations. "Keyword" is decoded at that point in order to recover the data. Additional bits within the offer code word excess, depending on the composition of the object used, allow the objective of using the decoding technique to decide whether errors are corrected by the correspondence and sometimes corrected together, the information must not be retransmitted. writing systems completely different errors depending on the types of errors expected, the expected error rate of the media is selected and whether or not information is transmitted or not. faster processors and technologies higher communications create a lot of complex coding schemes, with increased police and error correction capabilities that can be achieved with smaller integrated systems, allowing for a lot of solid communications.

In any case, the trade-offs between measurement data and the overload composition, the complexity of the composition and the acceptable delay composition between transmissions should be considered for each application

II. CHIP MULTI PROCESSOR

The chip multi processor is mostly applicable to identically sized logic blocks. This identically sized logic blocks are also known as tiles which is organized by regular 2D layout. By using different processor generations the size of CMP is decided. This will increase the number of on chip tiles and reduce the size of tiles. This CMP will translate the inter link distances which depends on the scaling functions. From below figure (1) we can observe the effect of CMP processor. Here the CMP cores will decrease the length of network chips from

An IP core is a functional component that has its own role inside the chip. These IP cores can be general-purpose processors, DSP, embedded memories or I/O blocks, each having its own function and capacity. The ability to integrate a number of IP cores in NoC helps in improving the electronic system's performance and decrease the complexity in the chip. However, an increase in the number of IP cores results in greater communication complexity between these IP cores. The issue of communication complexity in NoCs has become the most important and considerable challenge in NoC design. Therefore, several approaches and methods have been proposed to overcome this issue in NoCs.

The first approach for resolving the communication complexity in NoC is called point-to-point connection; it provides direct point-to-point communication between the IP cores in NoC. In this approach, the IP cores can directly communicate with each other without any priority or arbitration unit. Therefore, a larger wiring area is needed to implement a complete system in Noc [2]. Another solution to the problem of communication inside NoCs is bus-based communication systems. There are several existing NoCs that are bus-based. In bus-based communication, a shared communication bus is provided that connects multiple IP cores.

Generally, in NOC there are two limiting factors they are Increasing complexity and interconnection delay. The system will become unbalanced when the network traffic increases. The delay is increased because of switching and channels congestion. There are three phase’s in path congestion as shown in fig (1)

1) Switch contention: Dispute will happen, if a few packets go after a similar output channel.

2) Switch Congestion: So when a packet is transmitted through the north output post, some packet get a fizzled yield which are blocked and holding up at the input buffers.

3) Channel Congestion: The change comes up short on buffer space, due to the constrained input buffer size. Recently arrived packets are not suited by input buffers.

The network interface is the part of NoC that provides the connection between the routers and IP cores. This interface coordinates the data moving between routers and IP cores in NoC via a full-duplex communication link.

When the IP core transmits the data to the network, the data will be first received in the network interface, which packetizes the data and adds destination information to the packets. After that, the routers will read the packet information to route it to the right direction based on the routing algorithm policy in the router

From figure (1) we can observe the effect of CMP processor. The most attainable clock frequencies are achieved by wire transversal. Fast speed operation is available in this system. Here the power consumption will be under controlled modestly.

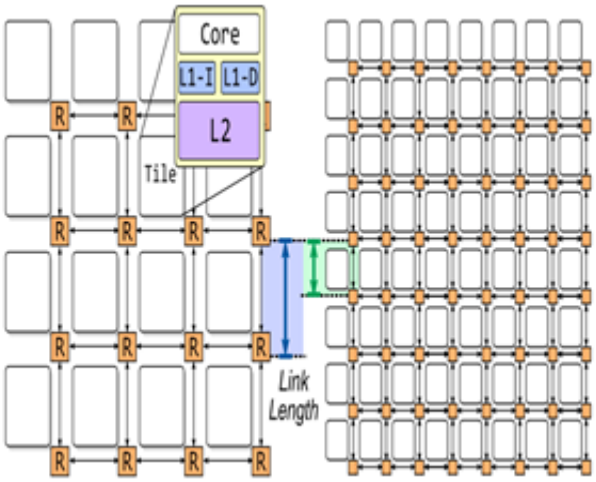

Fig. 1:16-CORE CMP (LEFT) TO A 64-CORE CMP (RIGHT).

From figure (1) we can observe that the number of tiles will be increased and inter tile length will be decreased. This CMP processor will have equal die size. The design procedure of single cycle link transversal (LT) is difficult. This design is mainly used in the general purpose and heterogeneous multi processor system on chip. The physical layout has irregular structure and has longer links. To increase the performance of scaled down link lengths and longer links.

In NoC the original clock frequency is unaffected. The routers will not run the clock frequency faster. The rapid link will produce the normal operating frequency. The link traversal delay will not exceed the router from one half of the router. Small medium wire lengths are appropriate for wire engineering and this is previously mentioned. Here multiple segments are linked by using rapid links and this is introduced by the dual stream elastic buffers. The pipeline registers will act as elastic buffers which will control the DDR. In NoC design the rapid link will provide benefits. Here the long wires will increase the delay in rapid link.

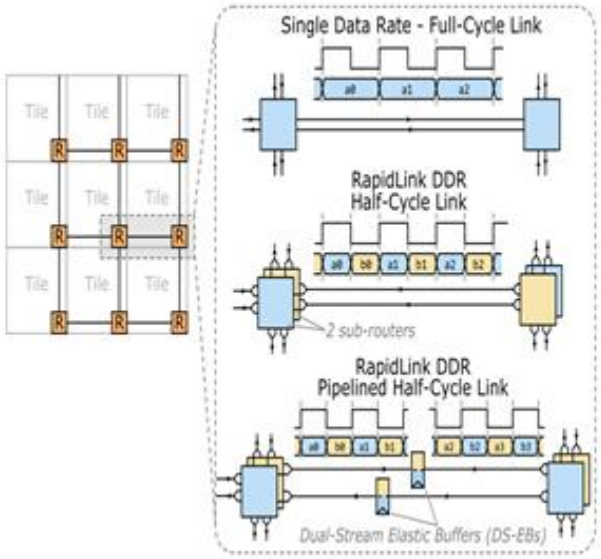

Fig. 2: ROUTER OF ONE FULL CYCLE

Basically, the design of single router will operate in single clock cycle. Along with single clock cycles, multiple clock cycles also used. This process will be continued at each node of network. Here one full cycle is performed in the system to transfer the flits across routers. The entire process is shown from figure (2). The transversal will remain at one full cycle by using the longer links. By using pipelining register multiple numbers of cycles are used for better performance. Double rate transmission in NoC links will constraint the delay router with full cycle operation. In DDR mode, the NoC link will operate the sender and receiver in effective way. Here the negative and positive edges will flits the clock in effective way. Here two routers are used for sending and receiving paths. The inter router link will be used for each path by using separate streams for flow of data.

The two streams will be separated by using data flow and this can be transferred using time multiplexed manner. In the multiplexed manner, the inter router link will ride in DDR mode. The positive phase clock will stream ride in the inter router link and in the same way the positive phase clock will stream ride in same inter router link. From figure (2) we can observe the router organization of one full cycle. Here in DDR link the all sub routers will drive per node. In timing closure the all data will reach to next node with in full time.

The original clock frequency in network on chip will be affected by using rapid link. This link will be un affected and the routers will not run faster than the normal operating frequency. The link transversal delay will not exceed the router depends on constraints. This system is feasible for small and medium wire lengths using appropriate wire engineering. The half of clock cycle will not fit the delay depend on rapid link. Multiple DDR half cycle segments will be introduced depend on fragments used. The dual stream elastic buffers will control the flow of pipeline registers. The NoC design uses DDR transversal link for better performance.

III. NI ARCHITECTURE FOR FAULT TOLERANT MECHANISM

The below figure (3) shows the network interface architecture of fault tolerant mechanism. Inter and intra router delays are exploited in the NoC design and this will be in the format of asymmetry. In one single clock cycle, the system transverse long distances which will fit the components. High radix routers are used to allow the designation of small hops. This constitutes longer links and as well as fairly complex routers. Here acceptable operating frequencies are obtained to increase the port of switching logics. Custom design effort are obtained to complicate the layouts in high radix networks. High latencies are obtained in high radix networks which will incur the local traffic from neighbor. This will transfer the unnecessary data over longer distances

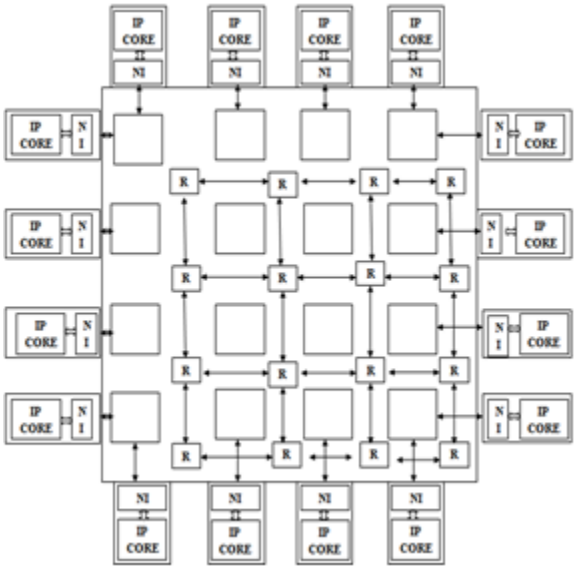

Fig. 3: NI ARCHITECTURE FOR FAULT TOLERANT MECHANISM

The physical architecture of fault tolerant mechanism in Noc is shown in above figure (3). In this we use mainly four network interface (NI), IP core, router and link. The mesosynchronous links are interconnected to each other by using routers. There should be communication between network interface and router. A conjunction synchronizer is used to perform the better communication in meso synchronous links. Various clock regions are used to enable the clock domains. Here all routers will reaches the interconnect pins through network interface. The design of this proposed architecture is simple compared to others and there is no need to meet the constraints of clock skew inside the network interface. By using low effort the clock design is distributed. In end to end communication the network interface is responsible to implement the transport layer of ISO/OSI stack. Data link layer is implemented depend on the routers in network layer. From below figure (4) shows the design of network interface for fault tolerant mechanism.

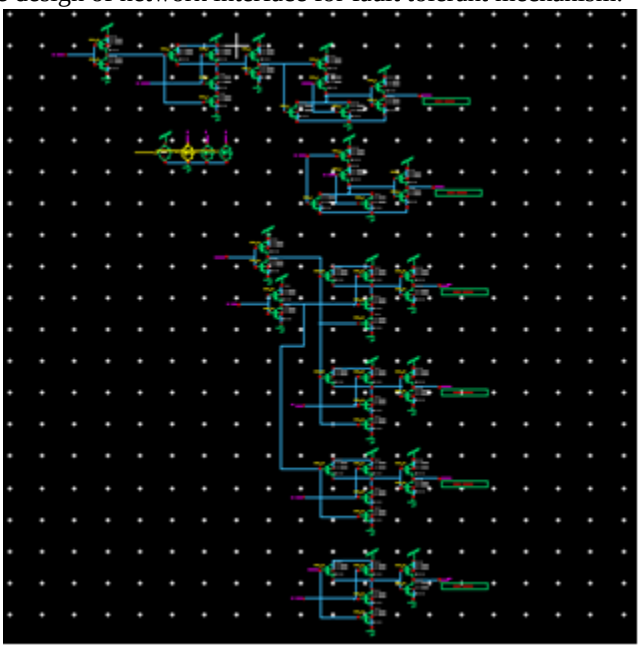

Fig. 4: PROPOSED NI DESIGN

It is mainly implemented on the layered approach on the top of lower one. At last the both network interface and router will exploit the service in effective way. This plays import role in point to point communication mechanism. The proposed synchronous approach will determine the data link layer. This will mainly enable the capability of system. in the same way, data flow control will embed the network interface unit and router interface unit. The signal propagation is done in physical layer by using set of wires. This system will manage the vertical interactions between data link and physical layer.

IV. RESULTS

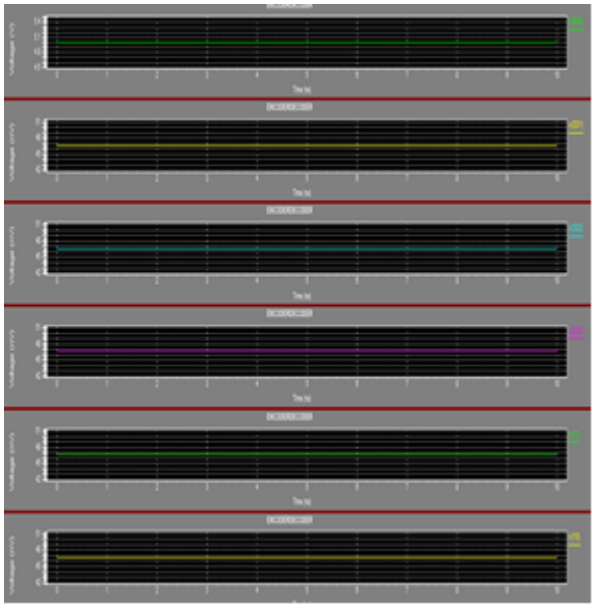

Fig. 5: OUTPUT WAVEFORM OF PROPOSED DESIGN

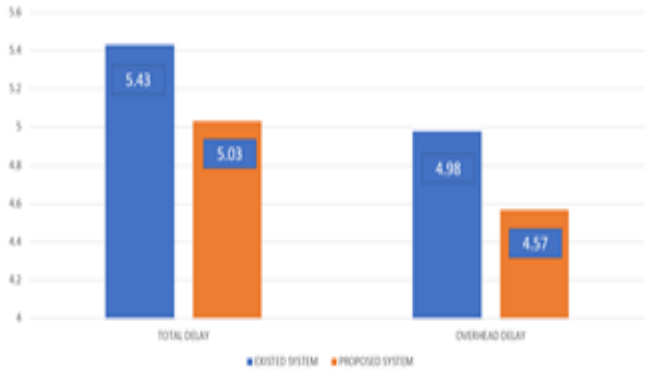

Fig. 6: COMPARISON GRAPH

The above figure (6) shows the graph of total delay and overhead delay. Here the value of total delay for proposed system is less than existed system and this can be observed from graph.

Table. 1: COMPARISON TABLE

S.NO	TOTAL DELAY	OVERHEAD DELAY
EXISTED SYSTEM	5.43	4.98
PROPOSED SYSTEM	5.03	4.57

V. CONCLUSION

In this paper, an effective network interface design using fault tolerant mechanism is implemented. This system will manage the control flow in effective way. In the same way, the physical issues of system on chip will be reduced by using the network interface. Here the bout network interface and router are interconnected to each other. The IP connections will play major role in entire system. This system gives maximum throughput and low latency performance compared to others. Similarly, the proposed network interface architecture will not produce bandwidth limitations. Because of this effective results are obtained in the proposed network interface system.

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