

High Performance Bulk Driven Operational Transconductance Amplifier and Applications

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Abstract: In this paper a bulk driven Fully cascoded operational transconductance amplifier(FCOTA) is designed. OTA applications are designed for voltage controlled current amplifier, filters and analog subtractor. With the current sizing method, all transistors in FCOTA work under weak inversion field. The total current in the proposed amplifier in terms of nano amperes only. As part of low power the circuit operated with the power supply of 0.8V. The main important features of the design are good linearity and accuracy. Full input and output voltage swings. This circuit has been constructed using CMOS technology with UMC90 nm. The circuit's total power consumption is 620nW.

Keywords: OTA, bulk driven, active filters, trans conductance, power consumption.

I. INTRODUCTION

CMOS arithmetic circuits plays important role in the signal processing applications[4-6]. Because most of the future processor designs required high speed, low power and medium resolution[1]. Addition, subtraction and multiplication functions are easy to design in digital CMOS techniques, but in analog design these functions are difficult. Because most of the analog arithmetic circuits are designed with operational amplifier based circuits with resistor and switched capacitor networks. CMOS analog arithmetic circuits, highly works on the principle of linearity. So the operational amplifier is best at linearity that's the reason amplifier best suitable for analog arithmetic circuits. Such type of circuits is struggling with rise time and fall time problems and propagation delays. Another important application of OTA is in the design of active filters. Amplifier used as an active device in many filter applications [7-9]. In digital design, power consumption is mainly because of static and dynamic power consumption. In analog design power consumption is mainly because of load capacitance and frequency of operation. Operating all the transistors in the sub threshold conditions means operating weak inversion region, there is a chance to effect with leakage currents. With a Current steering approach leakage current problems can be avoided [9].

II PROPOSED OPERATIONAL TRANS CONDUCTANCE AMPLIFIER (OTA) WITH BULK

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DRIVEN INPUT FOR CMOS ARITHMETIC CIRCUITS

The output circuit for the bulk is identical to the input operated by the gate, the input signal is applied to the transistor's bulk terminal and The gate provides a connection between the source and the drain [1-3]. The traditional OTA inaccurate to obey Square Law for sub-micron devices. So the proposed OTA works in weak inversion region with gm/ID base design. It is also good at accuracy and high output voltage range. Gm depends on the bulk trans conductivity of the input pair for a bulk-driven input level. Relative to gate-driven transconductance, a bulk-driven opamp has a lower gain and higher bandwidth because the bulk trans conductance (). Substrate terminal transconductance of an input transistor is much smaller than its gate trans conductance (). Substrate or bulk trans conductance can be expressed as

$$g_{mb} = g_m \frac{V}{\sqrt{2\phi_F - V_{SB}}} \quad (1)$$

The input signal is given to the bulk input pairs T1 and T2 in the input phase of Figure 1, and the gates are attached to the ground then the T1 and T2 in the weak inversion region. The drain to source current (2) depends on the leakage current in the sub-threshold region , T is the temperature in Kelvins, n is the tangential change in weak inversion, K is the constant of Boltzmann, q the electron or hole charge.

$$I_{DS} = I_S \left(\frac{W}{L}\right) \exp\left(q \frac{V_{GS} - V_{th}}{nKT}\right) \left[1 - \exp\left(-q \frac{V_{DS}}{KT}\right)\right] \quad (2)$$

The transistors T5 – T8 implement the proposed current scaling method. For voltage to current conversion, transistors Tb1, Tb2, Tb3 form a current mirror to supply differential currents to the output phase. Transistors T1-T12 operated with an suitable W / L ratio in a sub-threshold region

Table 1: Operating points for transistors in the OTA

Transistors	W(um)/L(nm)	I _D	Region of operation
T1:T2	18/180	393nA	Region 3
T3:T4	45/180	393nA	Region 3
T5:T6	13.02/200	505nA	Region 3
T7:T8	2/180	112nA	Region 3
T9:T10	2/180	112nA	Region 3
T11:T12	2/180	112nA	Region 3

** Region 3 - Sub threshold region

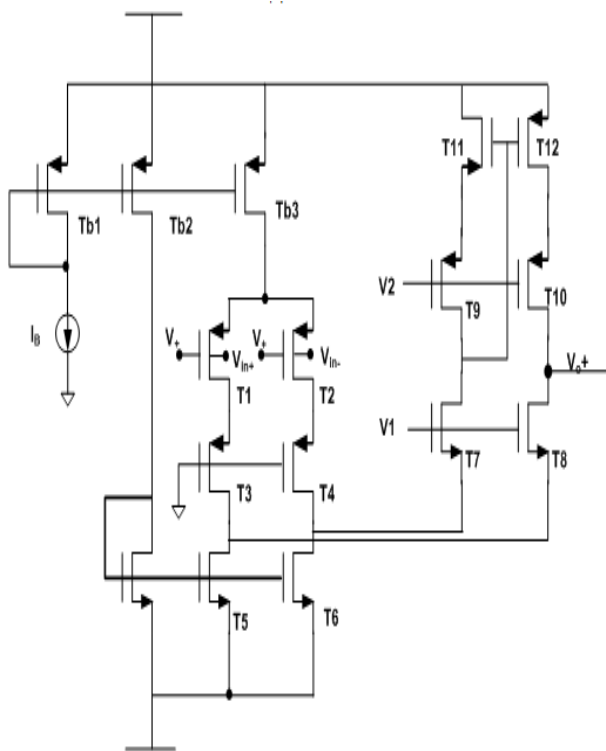


Figure 1: Schematic of Standard Folded-Cascode OTA with Gate Input

Current Sizing:

Current sizing is reached by reducing impedances in output. The T5 and T6 transistors form the source degenerated current mirrors. These two transistors set the current in T7-T8, which is the T3-T4 and T5-T6 difference. That is a small part of the T1 and T2 currents.

The current sizing ratio between Tb1 and Tb2 is 7:1(2I_B/14) maintained to save the power in the bias circuit as shown in Figure 1. This is part of the differential input pair current.

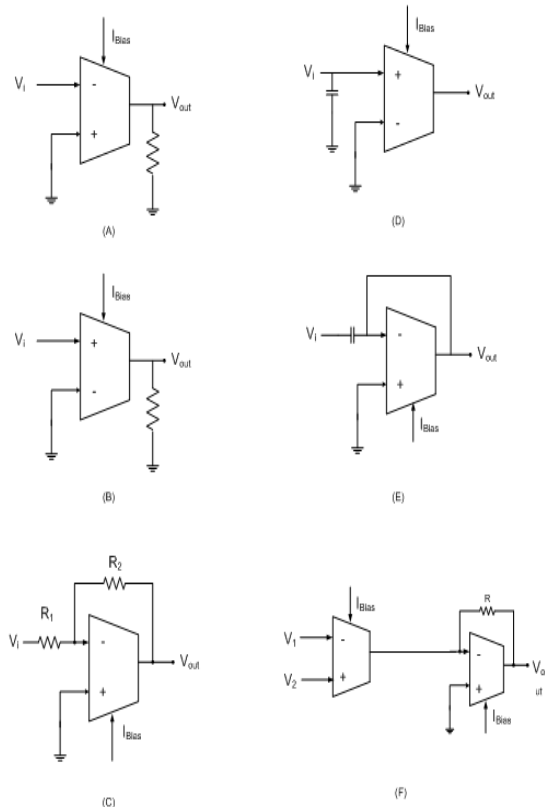


Figure 2 A) Inverting Amplifier B) Non Inverting Amplifier C) Buffer D) Low Pass Filter E) High Pass Filter F) Analog Subtractor

III. APPLICATIONS OF OTA AND SIMULATION RESULTS

Figure 2 displays the basic inverting and non-inverting amplifier and its transient analysis is shown in the Figure 3 and 4 while providing input at the OTA inverting terminal circuit which inverts the input signal at the output. While giving input at the non inverting terminal output of the OTA is in phase with the input

Active filters can be easily designed using OTAs. The filter characteristics easily controlled by using the structure of OTA's. Low pass and High pass filters are shown in Fig. 2.D and 2.E and their AC analysis with gain plots are shown in Fig. 6 and 7.

The signal bandwidth of the low pass filter is

$$f = \frac{1}{2\pi RC}$$

$$A_{VL} = \frac{A_{Vm}}{\sqrt{1 + (\frac{f_i}{f})^2}}$$

The low pass structure is a fixed pole and fixed DC gain with fixed tones conductance GM and variable output impedance. The capacitance and reactance at the input is larger at low frequencies and large at low frequencies

The 3dB cutoff frequency of the high pass filter is

$$A_{Vh} = \frac{A_{Vm}}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}}$$

The response of the both filters can be adjusted with trans conductance of the OTA.

CMOS analog sub tractor is designed with proposed folded cascode OTA. The structure was simple connection of back back to OTA. The difference signals are connected to primary inputs of the first block and its output is driven by a buffer structure. The common mode noise is almost negligible in the proposed analog subtractor. Because the folded cascode amplifier designed with current scaling method. Throughout the circuit total current is scale-able and maintaining constant current. The transient analysis results are shown in the Figure 8. Gain and bandwidth are shown in the Fig 9.

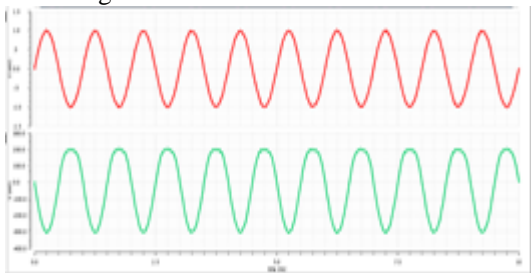


Figure 3 Transient Analysis of Inverting Amplifier

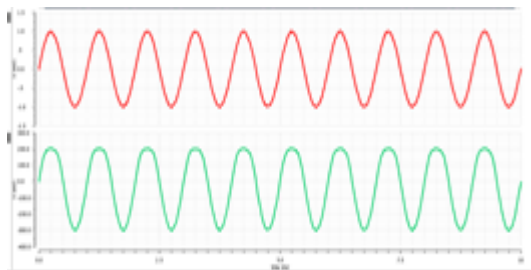


Figure 4 Transient Analysis of Non Inverting Amplifier

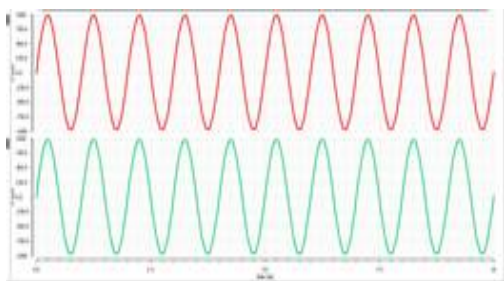


Figure 5 Transient Analysis of Buffer

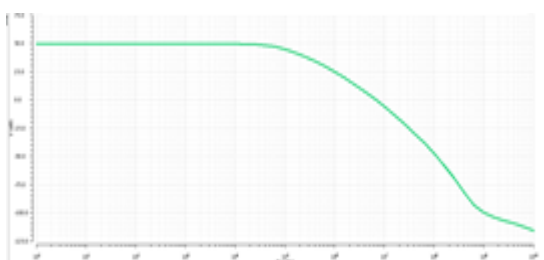


Figure 6 AC Analysis of 1st LPF

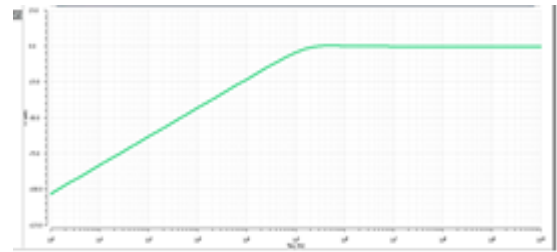


Figure 7 AC Analysis of 1st HPF

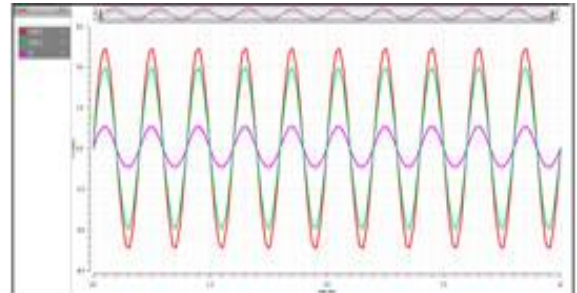


Figure 8 Transient Analysis of Analog Subtractor

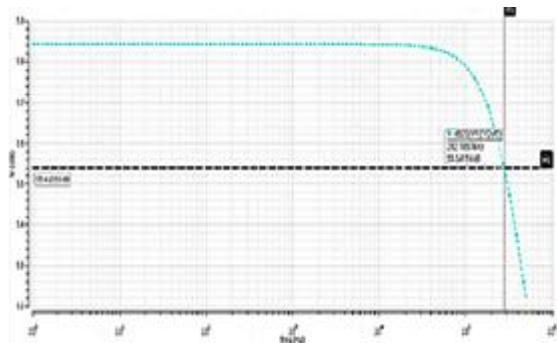


Figure 9 Gain 58 dB and BW=282 KHz

Table 2: Measured Characteristics of BULK DRIVEN OTA

Characteristics	Values
V_{DD}	0.8V
P_D	620nW
I_{Bias}	100nA
A_{DC}	58 dB
3dB BW	282KHz
Unity Gain BW	18MHz
CMRR	87.7
PSRR	94
C_L	1pF

IV. CONCLUSION

Using proposed high performance bulk driven OTA a group of active filters and as part of arithmetic circuits analog subtractor is presented. All the applications in the proposed paper designed with less number of transistors. Applications include inverting and non inverting amplifiers and low pass, high pass filters with transfer characteristics are obtained. The major annoyance performance of OTA based filters is less bandwidth compared to the commercially available differential amplifiers

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