

# Calibration Techniques of Analog to Digital Converters(ADCs)

Chakradhar Adupa, Rajesh Kumar Srivastava, Sreenivasa Rao Ijjada

**Abstract**— Data converters play a vital role in converting analog signal information to its equivalent digital information. In general purpose computing devices, industrial electronic equipment, and biomedical equipment especially in display device modules, they make use of these converters for displaying accurate results very effectively with high precision. these data Converters establish a key rolein between the analog transducers sensors, actuators to digital signal processing and helps for easy data processing in systems, like wireless communication systems and also in multi-channel biomedical devices etc.,There are variety of converters are available for different applications at different levels considering their parameters such as speed of conversion resolution, gain accuracy, etc., and In this paper, a comprehensive overview of the errors and the different calibration are discussed. The research work will give the different concepts and techniques for error calibration of ADC for an effective output with low INL and DNL obtaining high ENOB.

**Keywords**- ADC, Calibration, Errors, INL, DNL, ENOB.

## I. INTRODUCTION

Data converters are present in every electronic application majorly the analog to digital converters are becoming platform for humans to give commands to the electronic devices. There are lot of applications related to data converters but their accuracy is the concern for their usage in most critical applications such as medical, space, defense etc.,. The basic requirement of designing ADC is to have more accuracy in terms of INL, DNL and ENOB. There are several error sources in ADC which degrades the critical factors and to subdue the errors we look into calibration.

Digital calibration techniques [1]–[10],found in literature states that there are lot of advancements are done in designing of pipelined ADC but even though also found so many drawbacks are facing due to the analog signal paths during the calibration which will be performed in foreground or background[1]–[4].

The forefront calibration method stands from the absence of capability of tracking, and these methods are subtle to temperature and voltage variations and the aging of the device. In Analog paths, the interference cannot be escaped. In traditional methods, Calibration from LSB to MSB is done by accurate boot strapping algorithm, lower stages calibrated accommodated in the circuit and continued till the end stage finished. During the calibration process, the

implementation of sequential operations are very much complex in practice, since they need analog switch circuits in pipeline structures. This entire mechanism makes complicate the digital control logic and adds analog circuitry overhead. This will results more power and delays the conversion process as in the literature in [1]–[8].

## II. SOURCES OF ERRORS

The ADC's specifications has been deviated and limited mainly due to both linear and non linear errors presented in the data converters. The sources of these errors are the zero and full scale voltage offsets, Differential and Integral nonlinearities, Signal noise ratios, error in quantization process, Effective number of bits and spurious free dynamic range.

*Significance of these errors:*

Offset is the fluctuation seen in the ADC's characteristics between the actual and exact characteristics. this offset is observed in the converters because of the offset which is caused by the comparators which usually used in converters.

1. Offset errors creates a limitation in the ADC functionality. The substantial positive offset error causes the output value to steep at maximum before the input voltage reaches topmost level.and a substantial negative offset error gives a zero output value to the compact input voltages

2. Gain error is a change in the slope of the stair case in ideal to actual characteristics. It primarily gathers the error to considerable for higher output codes. in general the un calibrated voltage reference gives rise to gain error and the output code will scale with the voltage reference, hence the different voltage references will gives us different output codes.

3. INL error is the fluctuation seen in the LSB of a real transfer function from a straight line. and DNL is the fluctuation seen in the real step width to its absolute of 1 LSB. these are the two kinds of ways in which the errors can be found in ADC's functionality.

4.The error which occurs in analog to digital conversion process where it out-turn from its impotence to responds to small changes of less than a magnitude.

These errors can be reduced by calibration. Several calibrations schemes are discussed below.

## III. LITERATURE ADDRESSING THE ISSUES

Myung Jun Choe and Bang Sup Song and Kantilal Bacrania [11] have implemented a pipelined and background offset trimming method to 13 bit data converter

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circuit which converts from analog to digital information at a rate of 40 mega samples per second. the mentioned cmos converter background offset trimming is planned with highly Over sampling DS modulator which intensifies the resolution of "Folders" after 12 bits. Here The framework offset trim circuit constantly computes and fine tunes offset of turn up amplifier without butt into the usual operation of the circuit. in the process of framework offset trimming a part of pipelined ADC with additional circuitry is considered for misconception computation. The folding amplifiers are denoted as TA(Turn up amplifier) so TU2,TU3,and TU4 means three amplifiers are seen in the figure and each of these amplifiers are composed of three differential current controllers.

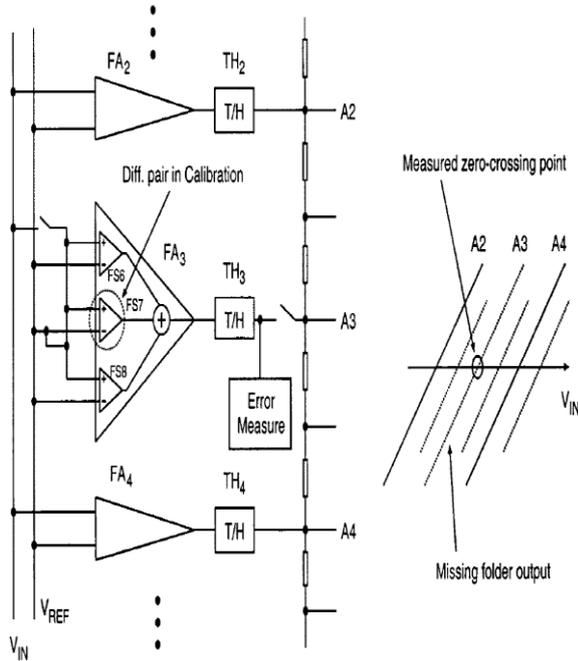


Fig.1 Backdrop offset Measurement

In figure 2 the detailed discussion regarding the offset computing and calibration is made. where both the things can be done independently. here highly over sampled converters are used to measure the output of the FA and at the same time the measured deviations are stored in memory. After every new measurement the up down blocks updates them selves. the arrangement is done for each current switch such that there will be a proper adjustment will be done by using a dissimilar voltage on a twin capacitors which needs a regular recharge.

The results shows that a SFDR of 82 decibels at 40 mega samples per second and the measured INL as 5 LSB and DNL is around +/-2LSB separately. and this work is done at 0.5um cmos technology which shows that it consumes 800W of power at 5v dc. and this method of implementation also proves that the feasibility of availing interpolation turn up ADC for elevated resolution at gaint speed is seen by joining the planning of two intensification and framework trimming idea.

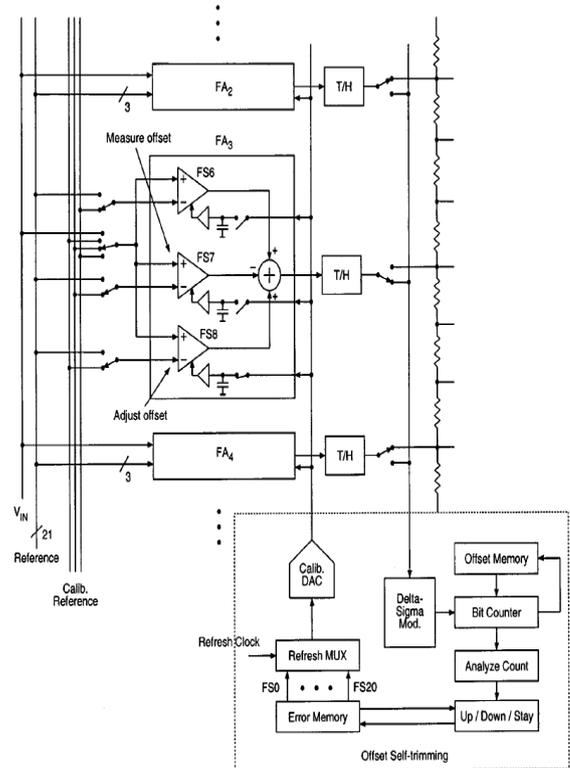


Fig.2 Backdrop offset trimming

Yun Chiu, Cheongyuen W. Tsang, BorivojeNikolicand Paul R. Gray [12] presents an adaptive digital technique which is closely to pipeline ADCs for calibration. in conventional approach the linearity is achieved by adjusting the analog component values but in this scheme it concludes component misconception from altering outcome and appeals digital post processing to precise those results. the method which is suggested at this point is making a immediate analogy to the channel equalization problem generally found in electronic Communications.

In the new architecture which is proposed in pipelined ADC where the component errors collected from entire stages of the pipeline are pull out at the same time using an Flexible FIR digital Filters it is similar to the twisting in communication channel. here the analog signal is path is thoroughly intact so the greatest conversion speed is allowed by fixed device technology. This way most of the Governing of the memory less errors can be corrected which are occurred due to capacitor mismatch, limited op-amp gain and switch-induced offset errors. the suggested correction techniques feasible to improve the conversion Precesion,conversion speed and lower the power Utilization in an effective wayby relaxing the analog parts when we consider precision matching and high open loop gain.

There is a need of a prototype of a pipelined ADC Errors in preparing and enlarging the digital correction techniques. by an assessment. assuming few errors in a pipelined ADC and these errors can be modelled as a twist in code domain. this depiction is very similar to that distortion in the channels of digital communication system. here we introduce a adaptive linear equalization (LE) for removing

the unwanted things from signal which shows to be the solution to attain well planned computation. with the help of Linear equalization we can also validate the channel postulation.and the block diagram representation for this error correction is shown in below figure3.

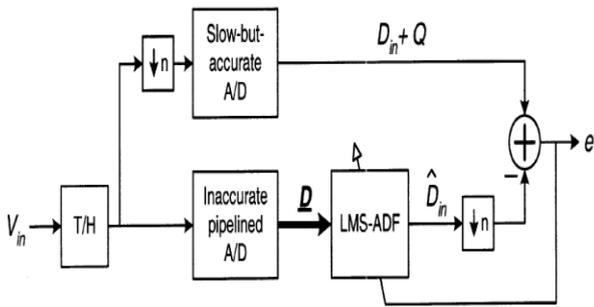


Fig.3 Error correction of pipelined ADC by Yun Chiu et.al.

so here the consequences of a particular point errors like capacitor discrepancy, restricted op-amp gain, opamp offset, and sampling key induced offset if these all are not signal dependent then these can be addressed by proposed code domain adaptive FIR filter.here the total procedure is all digital and data driven and fully adjustable and can be operated in background.in this process astrong tradeoff is seen between the accuracy and speed of a pipelined ADCswit the aid of digital correction techniques. So by this way we can translate the analog accuracy issues into the difficult of digital signal processing circuits this proceed towards satisfying the CMOS device scaling when compared to most traditional correction techniques.

Masanori Furuta, Shoji Kawahito, and Daisuke Miyazaki [13]says that the offset errors caused due to charge booser, and gain in accuracies caused by capacitor mismatch,in redundant radix-4 pipelined ADCs will be addressed by digital calibration Technique.

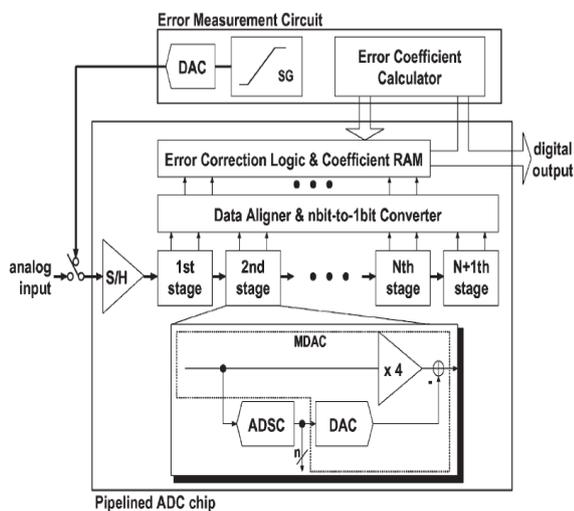


Fig.4 Proposed digitally calibrated ADC by Masanori Furuta et.al.

In fig.4 resolution of each stage is considered to be same for reducing the analysis. the analysis consists of as sample and hold circuit connecting to radix 4 ADC which utilizes

the ADSC and DAC with multiplying i.e. MDAC with a residue. The residue is generated from converting and sample and hold circuit with gain 4. The above discussed analysis proposes a digitally error corrections.

The suggested method makes more comprehensible error-quantifying and eliminate on board circuitry in the ADC. The work station simulation consequences shows that the maximum of 15 LSB of INL in case of a an un calibrated 15-bit ADC is abridged to 0.3 LSB.

A. Tahmasebi, A. Kamali, Z.D. KoozehKanani and J. Sobh [14] proposed analog-to-digital converter with pipelined architecture, deviations from operational amplifier gain and capacitor variations subdue the performance of general pipelined converters. In this paper, internal stage deviations due to gain are addressed with a novel technique. Correction of the error generated in every stage is done in analog domain. The suggested adjustment of plan of action use a distortion free ADC to decide acquired error of the calibration stage. The principle aim of the paper is to make use of profitable, moderate, stunted power, giant resolution ADC to make gain error free.

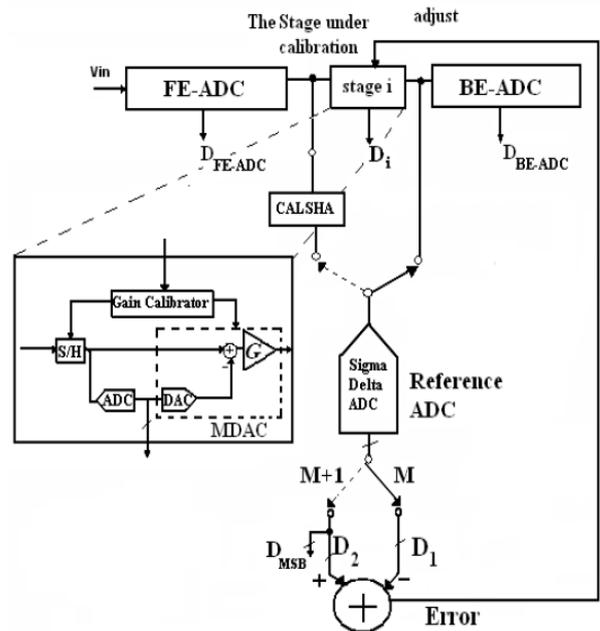


Fig.5 Basic idea of calibration algorithm by A. Tahmasebi et.al.

In figure 5 the primary aim beyond the computing scheme mentioned is precise for the inaccuracy in gain of non optimal pipelined stages applied a slow and giant resolution. In a 12 bit pipelined ADC shows that the benefit is calibration accuracy doesn't depend on other stages, as it shows that its SNDR is improved from 39db to 72db.

Qing Leil, ZhaoHui Wu, Bin Lil and Hailun Wu [15]discusses a digital backdrop error-computation Method for a 16 bit successive approximation pipeline data converter based on LMSA is presented with a 16 bit resolution and ENOB is improved from 10.31 bits to 15.66 bits in this a combination of LMS Algorithm combines with

a reference ADC which is a slow but accurate one for calibrating gain error, capacitor discrepancy etc.. the computing algorithm scheme is shown where a LMS algorithm is used with an output vector D of an imprecise pipelined SAR ADC is connected with a LMS adjustable digital FIR Filter.

Andres Amaya, Hector Gomez and ElkimRoa [16] present a method where a fully digital implemental by maintaining the offset accuracy phase calculation approach for offset voltage rectification capability is on slicer output phase by circumvent the input connection to a CM voltage is developed for high speed correction technique apart from traditional methods.

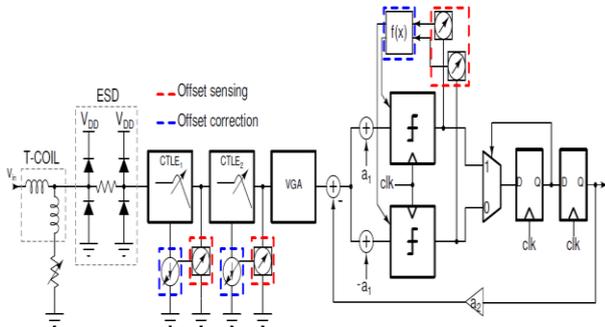


Fig.6 Conventional offset correction by SHS interface by Andres Amaya et.al.

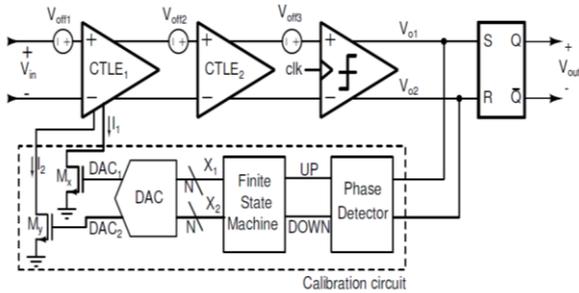


Fig.7Proposed offset compensation by Andres Amaya et.al.

Offset correction is by auto zero offset in every block of front end design using continuous time equalizer (CTE) and Variable gain amplifier (VGA) in addition with finite state machine (FSM). Resulting in low area and minimum offset.

IV. COMPARISON AND ANALYSIS & RESULTS

There are two different types of calibrations are available Analog field calibration and digital field calibration in Analog field calibration type the inaccuracy will be calibrated by calculation of residue, and then by quantizing gain error is reduced. Whereas the digital expedited method reveals enhanced power efficiency when we go for high speed implementations. In Correlation based methods mathematical algorithms are used for error correcting. In statistical based methods of calibrations they will detect the gain coefficient. These kind of digital calibrations require less modifications of ADC.

In this section the discussed ADC in this paper are compared and analysed to tabulate the results. Table. 1 shows the comparison of the different ADC and calibration of errors with the end result. This comparison summarises the total work done in this paper on ADC calibration.

Table1. Comparison of Literature of ADC and Calibration Techniques

	[11]	[12]	[13]	[14]	[15]	[16]
Type of ADC	Pipelined Folded ADC	Pipelined ADC	Radix-4 pipelined ADC	Pipelined ADC	SAR ADC	High-speed digital interfaces
Technique Used for Calibration	Pipelining and Background Offset Trimming	Adaptive digital technique using LMS Algorithm	Digital-computation ability	Digital-computation ability	LMSA for Digital backdrop error-computation method in SAR ADC	Offset voltage correction
Errors Calibrated	Offset of Folding Amplifier	module errors as well as capacitor inequality	Gain errors and offset errors	Gain of operational amplifier and mismatch in capacitors	Capacitor disparity, gain error and reference voltage offset error	Offset Error

Technology	0.5 $\mu$ m	-	-	-	-	130 nm
INL	$\pm 2.0$ LSB	-	$\pm 0.3$ LSB	-	-	-
DNL	$\pm 0.5$ LSB	-	-	-	-	-
ENOB	13 Bits	-	15 Bits	12 Bits	15.66	-
SNDR	82 dB	-	-	72 dB	-	-
Result	Background offset trimming implemented -  Resolution improved for 12 bits	Proposed technique benefit scaling CMOS circuit	Digital calibration  INL 15 to 0.3 LSB	SNDR - 72 dB 12-bit ADC.	ENOB improved to 15.66 bits.	Offset decrease

### V. CONCLUSION

This paper focuses on the importance of calibration in ADC and possible sources of errors for improving INL, DNL and ENOB. A detailed study of different state of art is given for reduction in error sources and calibrations for gain and offset errors.

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