Design and Analysis of Low Power SRAM using CMOS Technology

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Abstract*: The power consumption in commercial processors and application specific integrated circuits increases with decreasing technology nodes. Power saving techniques have become a first class design point for current and future VLSI systems. These systems employ large on-chip SRAM memories. Reducing memory leakage power while maintaining data integrity is a key criterion for modern day systems. Unfortunately, state of the art techniques like power-gating can only be applied to logic as these would destroy the contents of the memory if applied to a SRAM system. Fortunately, previous works have noted large temporal and spatial locality for data patterns in commerical processors as well as application specific ICs that work on images, audio and video data. This paper presents a novel column based Energy Compression technique that saves SRAM power by selectively turning off cells based on a data pattern. This technique is applied to study the power savings in application specific inegrated circuit SRAM memories and can also be applied for commercial processors. The paper also evaluates the effects of processing images before storage and data cluster patterns for optimizing power savings..

***Index Terms*: *Low Power SRAM*, SRAM, CMOS, Power Saving.**

I. INTRODUCTION

SRAM (Static Random Access Memories) is used in processing image frame buffers[1, 2, 3]. Videos have multiple frames that need to be stored. SRAM provide a low latency solution for comparing master video frames with subsequent frames. SRAM have low access time and can service a request for data elements quicker than DRAM (Dynamic Random Access Memories). They are fabricated on-chip, thus allowing them to use the same technology process in their manufacture as that of the core and other on-chip logic. SRAM is a volatile memory element, but does not require refreshing like that of DRAM. As there is high amount of temporal locality between subsequent video frames, usually the differential between the master frame and adjecent frames is stored on disk. The master frame is stored in a SRAM system that predominently only reads this frame[1, 2].SRAM memory system for image and video processing in application specific integrated circuits (ASICs) consume upto 81% of the power as standby/leakage power[4].

The power dissipation of the chip is dictated by the amount of power consumed by unit area. The total power in the system is comprised of two components, active power and idle power. Active power is consumed when the processor chip is busy. This power is used while processing data. Since the usage patterns of commercial electronic appliances imply that a device need not be busy all the time, there are gaps of idle periods. Transistors consume idle power (leakage power) during all times. At sub-nanometer nodes, the leakage power of transistors increases and their threshold voltage (Vth) is found to reduce. A lower Vth results in more leaky transistors as the pressure differential of Drain-Source voltages induces a small sub-threshold current even when the device is not active. This results in increased idle power, thus increasing the overall system power even when the processor or application specific IC is not active.

SRAM consumes significant area of the on-chip real estate. For video processing, this number has increased as the number of processing engines has increased. Since each processing engine can operate on independent portion of memory, an increase in number of processor engines require an increase in SRAM size for better throughput [2]. The size of SRAM impact system performance and most processing engines are allocated significant on chip area for SRAM system. Leakage power is determined by the number of SRAM cells. As the size of SRAM system in commercial appliances increases leakage power for SRAM is found to dominate the total power consumption.

Commercial processors and ASICs reduce operating power using techniques like power gating and frequency scaling for cores or processing engines and other on-chip logic circuits during idle modes [5]. Power gating drives the supply nodes (VDD/GND) into high impedence by using power gating transistors. This results in reduced power into the logic circuitry but also results in tri-stating these logic circuitry. Memory elements store data and validity of data cannot be compromised. Most large memory elements like L3 (Level Three) caches have additional error correcting circuits to ensure data fidelity. Since for memories, one cannot afford to have a loss in data reliability as it results in incorrect execution or crashing of applications that are run by the cores or incorrect processing of video frames and images by the processing engines. Thus we cannot use techniques like power gating for SRAM system, as tri-stating these elements result in data loss.

Studies show that processors and image, audio or video processing engines operate on data that is biased towards a particular data value zero or one [6, 7, 8].

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This results in SRAM memories having larger number of data cells that these biased values. Thus architecting memories that have biased properties for storing biased values has been suggested in some previous literature. Some techniques that are used to mitigate this problem include lowering the supply voltage across the SRAM cells. As leakage exponentially reduces with decrease in supply voltage, this results in reduced idle power. Data retention voltage (DRV) of an SRAM cell defines the minimum voltage that must be applied across the SRAM cell before it will flip. This voltage places a limit on supply voltage reduction. Due to process variations, across the chip, huge variations in DRV are observed[9]. This thesis analyzes traditional 6T SRAM designs for image storage, specifically for long idle periods of time and also suggests a novel implementation of 7T SRAM cell. Oriented for low nanometer nodes (sub 22nm), the proposal targets system power and suggests an alternate design called 'Energy Compressed SRAM system' that exhibits 15% lower power consumption. These proposals are targeted to be designed for large area and low activity memories consuming large amount of idle power. The thesis will consider ASIC's which operate on images. The goal of this research paper is to suggest a novel SRAM system targetted for image/video processing applications for saving leakage power.

II. Background and Motivation

A SRAM cell employs a cross coupled inverter structure to store data. Figure 1 shows the cross coupled inverter structure and its equivalent 6T (6 transistor) circuit. This structure is prevalent in processor caches and ASIC memory due to its simple design [10].

A. *Memory System using SRAM: Organization*

A memory system with SRAM consists of banks and each bank consists of multiple subarrays. Subarrays are internally organized into rows and columns. Columns consist of SRAM cells connected to a pair or bitlines. The columns are grouped and multiplexed to a sense amplifier. Rows consist of SRAM cells that share a common word Line. Figure 2 shows the full system that using SRAM. To read data, the pair of bit lines need to be precharged. To access an SRAM cell, the address is decoded upto the subarray level, asserting the appropriate word line and selecting one column from the group. The column address helps select one pair of column bit lines to the sense amplifier. Depending on the value of the data stored, on activating the cell, one of these bitlines will start to discharge. Data is detected using the sense amplifier which amplifies the voltage differential. The output of the sense amplifier is the stored bit value (having voltage levels VDD [logic 1] or Zero [logic 0]).

B. *Leakage Power in SRAM*

Power consumption of a large memory system with SRAM is dominated by leakage power at nanometer nodes. In ASICs used in cameras and in commercial processors (specifically last level caches), memories store data for long time and have low activity.

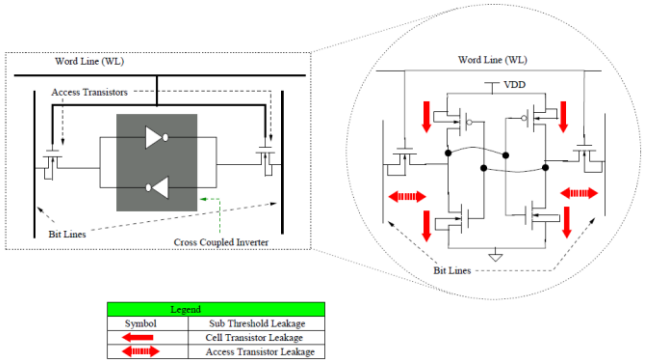

Figure 1: A 6T SRAM Cell

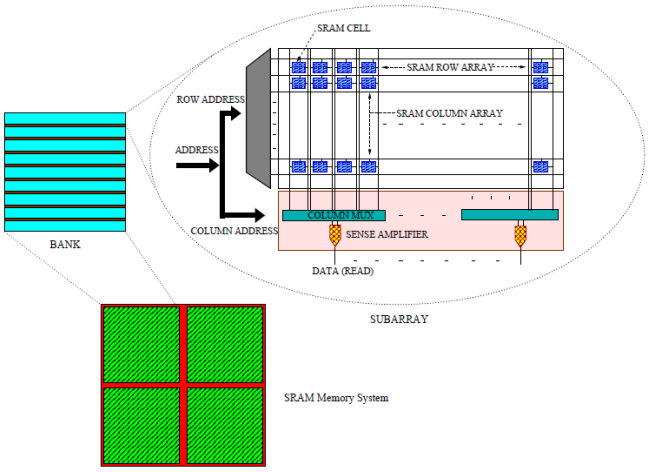

Figure 2: SRAM Memory System

Their power consumption is due to idle power which is dissipated due to leakage currents. At nanometer nodes, subthreshold, gate and reversed-biased junction leakage currents exist. As the technology node get reduced, the threshold voltage (Vth) of transistors reduces. This increases sub-threshold leakage at nanometer nodes and it dominates the total leakage[11]. There are two components of subthreshold leakage in SRAM, cell leakage and bit line leakage. Figure 1 describes the direction of cell leakage and bit line leakage. Bit line leak- age can occur in any direction and it depends on the data stored within the cell. Cell leakage occurs from VDD towards GND [12]. Cell leakage is caused due to the supply voltage differential accross these SRAM cells. Bit line leakage is due to voltage differential between the storage nodes and the bit lines and is found to be much lesser than cell leakage [13]. Techniques such as body biasing of access transistors ensure that bit line leakage can be reduced [14]. Low power SRAM schemes focus on reducing the supply voltage or increasing the Vth of individual transistors in the SRAM cell.

Initial SRAM low power techniques proposed employing dual Vt for reducing the leak- age power and some innovations in decoding [15]. Most of the modern SRAM cells employ these techniques already and still have high leakage currents. This is because in nanometer nodes, most of these techniques for controlling leakage become ineffective.

Leakage power in 6T SRAM cells can be reduced by using reducing gate voltage and body biasing the access transistors.

Dual biasing and PMOS transistors can also be used to reduce leakage [14].

SRAM can be power gated towards a nominal supply voltage at sub-array granularity to reduce the idle power consumption [16]. This proposal leverages on data retention characteristics of these SRAM cells, such that the supply voltage is maintained above the data retention voltage (DRV) of a majority of these SRAM cells. Data retention voltage is the voltage above which data integrity for a SRAM cell is assured with a high probability. However the DRV value tends to vary within a large cluster of cells. As technology node decrease DRV increases causing bit flips in SRAM cells leading to retention failures. Thus current last level caches employ ECC to provide some protection in case of errors [17, 18]. At a system level, many manufacturers use DRV characteristics to employ fault tolerant SRAM systems [19].

C. Image Storage for Application Specific Integrated Circuits

For the purpose of initial design, image benchmarks (using unprocessed raw images) are analyzed. These benchmarks are publically available and is used for research on image and video processing [20, 21, 22, 23]. The size of the SRAM system that will be required to store a single image is shown in figure 3. On an average, the image sizes in the benchmark tend to be nearly 1MB for raw bitmaps.

Figure 4 shows the total number of cells that store logic '0' is almost 50% on an average. Since images have high amount of correlation between between adjacent pixels, adjacent data sets can be grouped and grouped elements can be analyzed. In this thesis, data is inverted and stored, so that this work is compatible other systems such as commercial processors. This thesis considers data sets containing zeros in the same position between adjacent pixels. Figure 5 shows groups having 2,4,8 and 16 data bytes and shows the proportion of groups that will have only zeros scanning bit positions one by one for all bytes in the group, called a compress-group. For instance, if a group is constructed by using two adjacent pixels, where each pixel is a byte long and has zeros exactly at MSB and LSB positions. Other positions all have ones. The proportion of compress-groups to total groups for the image will be 0.25, as 2 (LSB and MSB only) in 8 bits are a zero on an average. It is interesting to see that this number will remain the same even if the group is constructed by using 4,8 or 16 adjacent pixels, if all pixel elements have MSB and LSB positions have a zero.

However, Figure 5 shows that as the size of group increases the proportion of compress- groups decreases. Since the benefits saturate around a size of 8, in this thesis, compress group with a size of 8 is analyzed. Use data patterns to compress the energy in SRAM (En-Com System) by selectively turning OFF groups of cells SRAM to save leakage power.

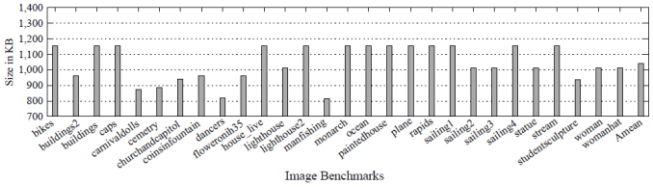

Figure 3: The size of memory occupied by the raw-image

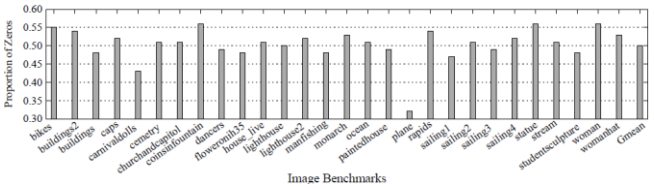

Figure 4: The proportion of SRAM cells that store a value of '0' to total number of SRAM cells

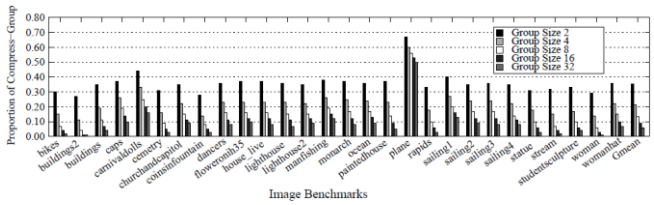

Figure 5: The size of the group is varied and the proportion of compress-groups is compared to total groups. The proportion of compress group is found to exponentially decrease with increasing group size

The En-Com System proposed should be used at low nanometer designs (below 22nm) as the leakage power becomes dominant at these nodes and DRV technique with SECDED does not help due to large DRV values and variance. In this paper, we evaluate the design at 130nm IBM process.

III. System Design Consideration and Implementation

There is high amount of spatial and temporal locality in video/image data. The data in these structures can be compressed by grouping together adjecent pixels. At the system level, these pixels may be stored in adjecent columns in an SRAM. Every row in SRAM can represent a line of pixels. There can be one bit assigned for every 8 bits of image pixels. A frequent pattern like 00000000 can be compressed using this one bit to represent the data for the entire 8 bits. These 8 bits can then be turned off saving leakage power. These can be done in 2 ways; the frequent pattern can be identified on a row basis or column basis. Each of these techniques have trade-offs in layout and implementation.

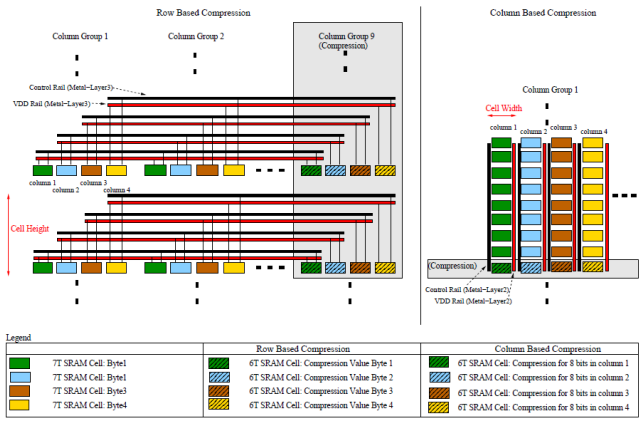

Figure 6: Row Based Compression increases the per cell height by four 'Layer 3' metal lanes per cell. Column Based Compression increases the per cell width by two Layer 2 metal layers only

The En-Com system employs a novel column based data based compression instead of row based techniques that have already been proposed. The row based techniques involve the use of large number of metal wires that require to be connected to each SRAM cell. This involves an area overhead in the design of the SRAM cells as shown in the Figure 6. The column based technique involves using parallel column based metal lines. The row based compression technique increases the cell height by four 'Layer 3' metal lanes. Compared to this, the column based technique will only increase the cell width by two 'Layer 2' metal lanes, saving layout area, an important design point in this paper.

The En-Com system stores the compresses value on an additional cell, called the Zero- Switch Cell. The compression pattern for this system is 00000000. When the Zero-Switch Cell stores the compressed value (data value 0), it switches OFF the compress-group. The compress-group consists of 7T SRAM cells that hold their values (data value 0), even though they are switched OFF. These switched off cells can be read without turning them ON and does not require any modifications in the read circuitry. This allows En-Com to be used as a perfect framework for video/image processing applications that usually compare master frames/images with subsequent ones. This comparision involves reads from the SRAM. By selectively switching OFF, En-Com can save leakage power in these applications. On any other pattern, the Zero-Switch Cell should not switch off the compress- group. To implement this, the Zero-Switch Cells are initialized to '0' at start. This ensures that almost all of the SRAM is switched OFF in the beginning. On a write of a '1', it is written to the Zero-Switch Cell along with the original cell.

En-Com uses one cell per compress-group, the area overhead will increase as the group size reduces. The additional overhead is because every compress-group will require an additional SRAM cell to store its information. Table 1 gives the area overhead as the group size is varied.

Table 1: Compress-Group Area Overhead

Compress-Group Size	Area Overhead
2	50%
4	25%
8	**12.5%**
16	6.25%
32	3.125%

Table 2: Parameters of the Energy Compressed System

Feature	Specification
Supply Voltage	1.2V
Row Decoder	4:16 working at 500MHz (Dynamic)
Column Decoder	2:4 working at 500 MHz (Dynamic)
Sense Amplifer	voltage based
Data Granularity	1 Byte access/cycle

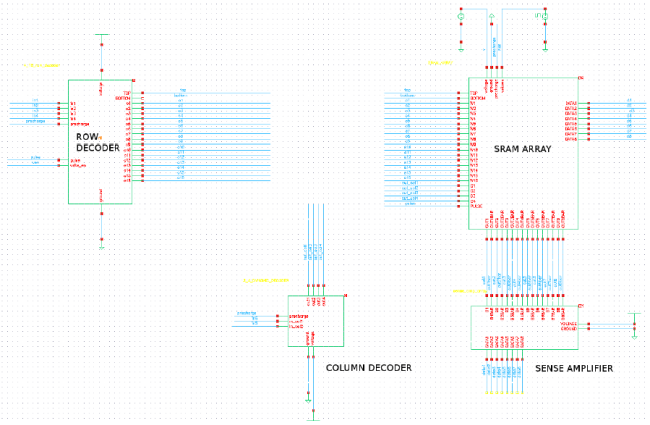

Figure 7: 'En-Com' implementation (Schematic). The top and bottom pins in the decoder and the SRAM array represent the lines to the Zero-Switch Cells

The En-Com SRAM System requires minor modifications in the decoders, SRAM column array and write circuitry. En-Com requires an architectural change that includes having a double write signal in case of a writing binary value '1' into the array. A write of binary value '1' requires one extra cycle. Since the decoder tree of a large SRAM memory system has a delay of many clock cycles, an additional cycle is a reasonable trade-off for the energy savings. Figure 7 shows the schematic of En-Com system.

The SRAM based memory system is designed at the 130nm node using the IBM process. A 16x32 SRAM subarray consists of dynamic NAND based decoders for operating the array at 500MHz. Table 2 shows the specifications of the system.

A. Design Consideration and Working

The En-Com System relies on energy compression using a frequently appearing data pattern. We choose a data pattern of 0000000 (eight zeros) to enable the compression. This number is selected based on figure 5 and table 1. A group of cells storing this pattern of eight zeros form the compress-group for the design. Each cell in the compress-group is a 7 transistor SRAM (7T SRAM). The design also requires a pivot cell to turn off the compress-group and store its value called the Zero-Switch Cell. Even though images contain more compress groups having only '1's, the En-Com system stores inverted values of data for images. This is to make the design consistent even for commercial processors, that have higher number of '0's over '1's in the caches. Commercial processors can ignore the inversion of data. Other major design considerations are:

- The Zero-Switch Cell will require a small driver for operating on the compress-group and a power-gate transistor
- The power gate transistor sizing determines the turn on/off time of 8 cells
- The compress group must hold the data-value (0 for each cell) and requires a 7T SRAM structure.

- This ensures that reads to the compress group will work without any modifications to the read circuitry at the SRAM.
- At the system level, the implementation of write logic and the read logic for the SRAM Array requires a few changes. Reads require that the pulse generator is not activated by the system and writes require it to be active in case of writing data value '1', the pulse generator must be active for an additional cycle to enable dual write.

The 16 rows in the 16x32 array are divided into 2 sections (vertically) of 8 rows each. Every column in a section has a Zero-Switch Cell. All Zero-Switch Cells are reset to a '0' at the beginning. Every write of a 1 to the SRAM section is also written to its Zero-Switch Cell. Only when all 8 cells in the column have '0's i.e the compress-group has the data pattern 00000000, the Zero-Switch Cell switches off the compress-group.

B. 7T SRAM Cell Design

The compress-group consists of cells with 7 transistor SRAM. This enhancement over traditional 6T SRAM is to store the compressed data value, instead of putting the SRAM in a high impedance state. The 7T SRAM cell holds logic zero 'strongly' when the compress- group gets activated. The activation of the highlighted transistor (Figure 8) ensures that the cell can be switched off without SRAM going into the high impedance state. Without this transistor if the cell is switched off, the sense amplifier may produce an erroneous output on a read. Due to positive feedback, there is unpredictability of the final state once the cell is turned on. By storing a strong '0', 7T SRAM ensures that these problems do not occur. Figure 8 shows the 7T SRAM cell in its logical view.

C. Compress Group

A Zero-Switch Cell is connected on each column for a group of 8 cells called the com- press group. Writing a '0' to the Zero-Switch Cell power gates the compress group. All cells in the compress group will be held to data value '0' even after power gating. The implementation of the Zero-Switch Cell and the compress group shown in figure 9.

D. Zero-Switch Cell

The 6T SRAM cell along with an inverter driver forms the Zero-Switch Cell. Its job is to store the information for the compress group. If the compress group contains data that is all '0', the Zero-Switch Cell is activated. A '0' in the Zero-Switch Cell implies a pattern of all '0's in the compress group. For any other pattern, the Zero-Switch Cell stores a '1'.

E. Dual Write Pulse Generator

The pulse generator, enabled when dual write must take place, produces a clocked signal that selects the Zero-Switch Cell from the section called the Dual Write Pulse Generator. After a write into the original cell, if the data value is '1', the Dual Write Pulse will also write into the Zero-Switch Cell.

F. Modification in Row Decoder

The row decoder is modified to accomodate additional 1 cell per group. This requires a select signals that are derived by taking the Most Significant Bit of the 4:16 row decoder.

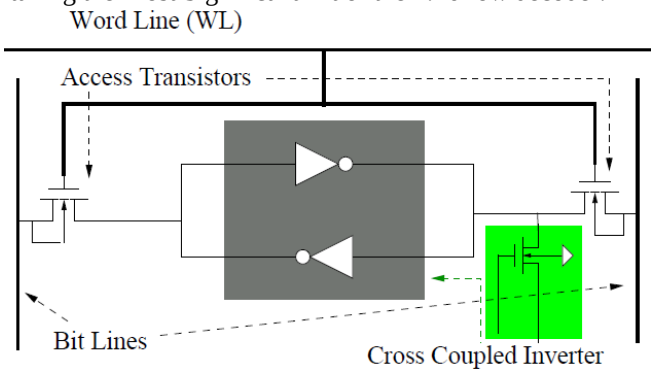

Figure 8: 7T SRAM cell (Logical View)

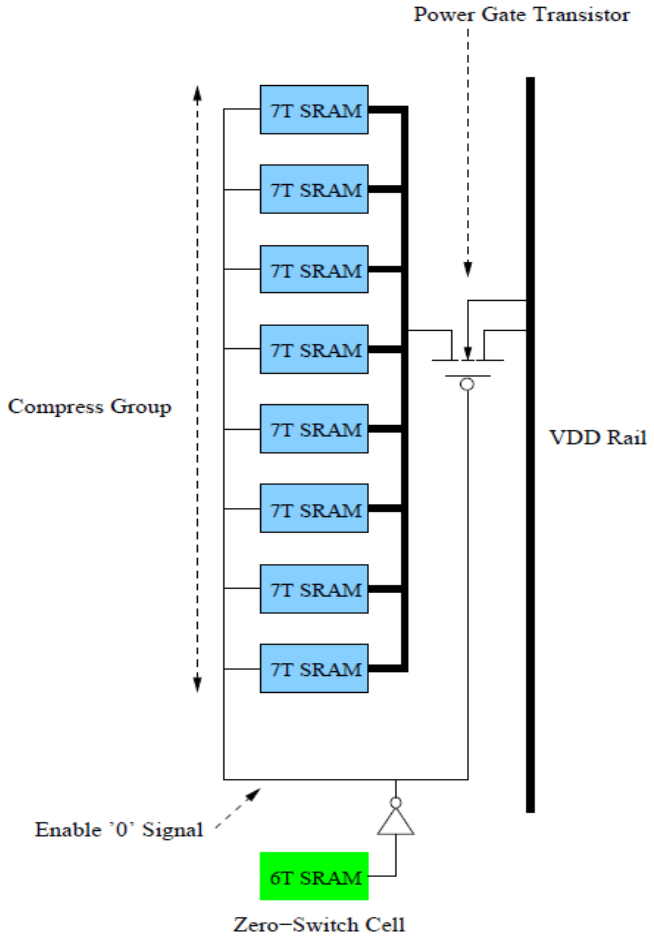

Figure 9: An 8 Cell Compress Group

The cells are selected on the assertion of the Dual Write Pulse Generator. Figure 10 shows the implementation of the 2 select signals.

G. Modification in the Write Circuitry

The write circuitry is modified to perform 2 writes in case of writing a '1'. Since writing is done by isolating the sense amplifier circuity, a dual write will involve maintaining this isolation for 2 cycles.

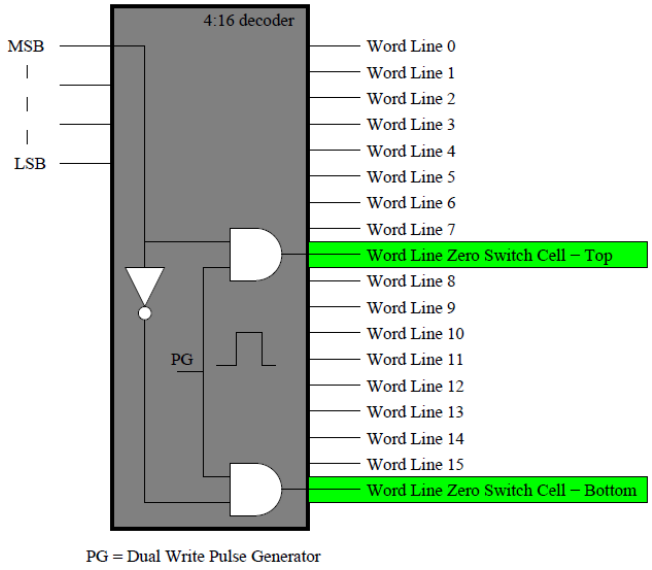

Figure 10: En-Com requires one NOT gate and two AND gates to select between the top or bottom Zero-Switch Cell in case of a write

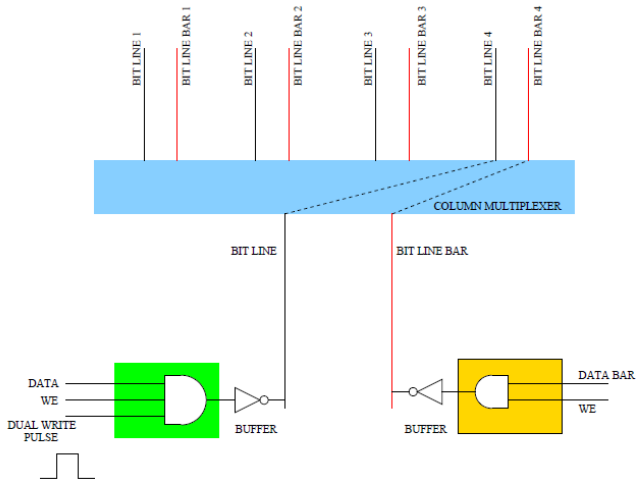

Figure 11: The write circuit is modified to support dual write in case of data value '1'. The pulse generator enables the dual write

The logic to implement dual writing is shown in figure 11. The 3 input AND gate for writing into the 'BIT' position ensures that dual write is activated only when Dual Write Pulse is generated.

IV. Conclusion and Future Scope

SRAM systems have leakage which is dominated by cell leakage. When these systems are used to store data they tend to have high power dissipation to leakage currents. They are usually used to store images or video frames in ASICs or to store application data in commercial processors. ASICs have processing engines that operate on this data. As the complexity of these processing engines have increased, they operate on larger data to improve performance. To supply this large amount of data, the size of the SRAM have increased in these ASICs along with increasing its leakage power. As these SRAM systems store images/video frames for long periods of time, leakage power mitigation is an important design point.

The paper implements a pattern based Energy Compression System (En-Com) that switches OFF cells to save leakage power. Contrary to row based compression scheme, En-Com is implemented as a column based scheme. En-Com allows reads to the SRAM to take place without any modifications and does not require turning ON the switched OFF cells. Traditional 6T SRAM is modified to a 7T structure to allow such reads to happen. En- Com requires an additional Zero-Switch Cell that is activated on compression and switches of a group of cells.

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