Design of Energy Efficient Control Unit and Implementation on High Performance FPGA

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Abstract—With the crisis of power across the globe, green communication and power-efficient devices are getting more and more attention. This work emphasis about the implementation of Control Unit (CU) circuit on FPGA kit. In this project, power consumption of CU circuit is analyzed by changing the different Input/Output (I/O) standards of FPGA. This project is implemented on Xilinx 14.1 tool and the power consumption on CU is calculated with X Power Analyzer tool on 28-Nano-Meter (nm) Artix-7 Field Programmable Gate Array (FPGA). Out of different I/O standards, CU circuit is most power efficient with LVCMOS I/O standard on Artix-7 FPGA.

Keywords: Control Unit, I/O standard, Low Power, LVCMOS, FPGA.

I. INTRODUCTION

With the increase in population and industrialization across the entire world, the world is facing a huge problem of energy and power crisis [1]. Green communication and power efficient devices are the most suitable technique for overcoming from the problem of energy and power crisis [2]. Keeping all these aspect in knowledge, this research work gives an idea about designing a power-efficient CU circuit with FPGA. The control unit is the basic and one of the initial components of Central Processing Unit (CPU) [3]. The function of CU is to respond on the set of instructions, which is to be sent to the processor of CPU. In this research work, various LVCMOS I/O standard [4] of Artix-7 FPGA which is shown in figure 1 is changed, to calculate the power utilization on CU.

Figure 1.Different LVCMOS I/O standards.

LVCMOS I/O Standards.

The LVCMOS is low voltage digital integrated circuit of CMOS technology [5]. I/O standards are Input/Output standards, which works to match the impedance of device with input line, input port, output line and output port, in order to avoid the reflection of transmission line. With 28nm Artix-7 FPGA, LVCMOS I/O standards is operated at maximum voltage of 3.3 V. The different LVCMOS I/O standards are following:

- LVCMOS12
- LVCMOS15
- LVCMOS18
- LVCMOS25
- LVCMOS33

In this work, power analysis is done only for LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33. LVCMOS12 is not compatible with 28nm Artix-7 FPGA.

II.METHODOLOGY

High-performance Random-Access Memory (RAM) design is implemented on 28 nm FPGA [6]. In this work power calculated for different LVCMOS I/O standards. Using LVCMOS I/O standards, authors have designed a low power D Flip-Flop [7]. Green data flip-flop design is implemented on FPGA using different LVCMOS I/O standards [8]. LVCMOS I/O standards based 4-bit register [9] is designed by authors on FPGA. Researcher also design Energy efficient digital clock with the help of LVCMOS I/O standards is implemented on Spartan-6 FPGA [10]. Clock gating-based energy efficient Arithmetic Logic Unit (ALU) design is implemented on FPGA by scaling operating frequency [11]. Therefore, a lot of work has been done on LVCMOS I/O standard-based FPGA devices for promoting green communication and power efficient devices. But no work is done on LVCMOS based CU circuit. So, in this work, a power efficient LVCMOS based Control Unit circuit is designed on 28-nm FPGA

III. EXPERIMENTAL SECTION

In this research work, the interfacing of CU with Artix-7 FPGA is done at an ambient temperature of 25°C with the airflow of 250 Linear Feet per Meter (LFM). The power is calculated at the frequency of 1GHz. The power calculated for different LVCMOS I/O standard is analyzed by X Power Analyzer tool. The CU takes 8-bit data instruction, clock signal, reset signal and zero as input for the operation. The output of CU has 13 wire line. The Register-Transfer Level (RTL) schematic of the CU is presented in figure 2.

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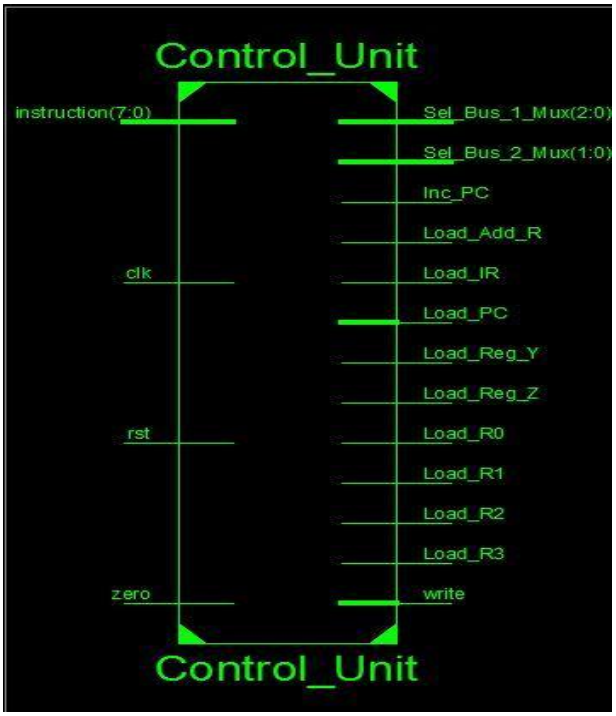

Figure 2.Schematic of Control Unit.

IV. POWER ANALYSIS.

The total on-chip power dissipation is calculated for LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33. The total consumption of on-chip power is sum up of static power and dynamic power. Static power is also called as leakage power of FPGA. Dynamic power is the sum of Clock power usage, Logic power dissipation, Signal power utilization and I/O power consumption of FPGA.

A. Power Analysis of LVCMOS15.

The total power of LVCMOS15 is 0.084 W which constitutes clock power utilization of 0.005 W, logic power usage of 0.001W, signal power dissipation of 0.001W, I/O power consumption of 0.036 W and leakage power dissipation of 0.042 W. The power analysis is represented in figure 3.

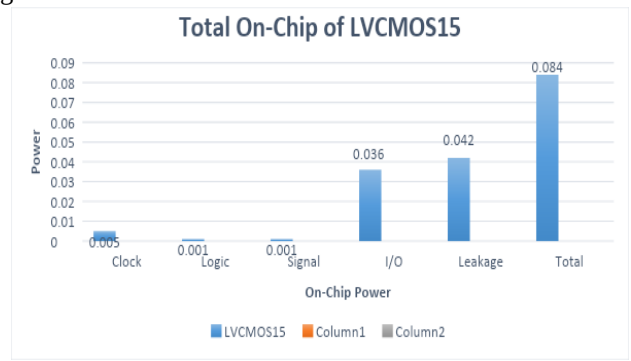

Figure 3.Power Analysis of LVCMOS15.

B. Power Analysis OF LVCMOS18.

For LVCMOS18 I/O standard, clock power dissipation is 0.005 W, logic power utilization is 0.001 W, signal power usage is 0.001 W, I/O power consumption is 0.048 W, leakage power dissipation is 0.043 W and total power used by device is 0.097 W, which is shown in Figure 4.

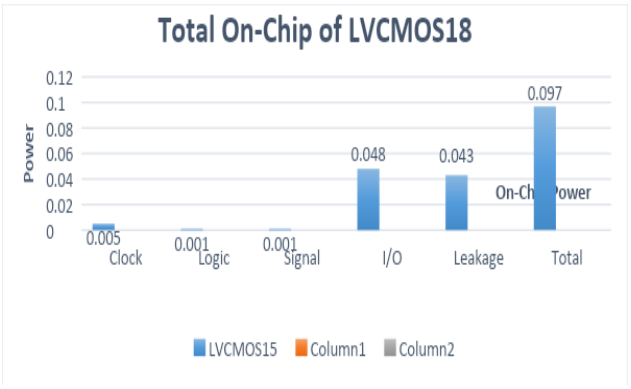

Figure 4.Power Analysis of LVCMOS18.

C. Power Analysis OF LVCMOS25.

The total on-chip power of LVCMOS25 is described in Figure 5. The total power usage of the device is 0.135 W, which is sum up of, clock power utilization of 0.005 W, logic power usage of 0.001 W, signal power utilization of 0.001 W, I/O power usage of 0.086 W and leakage power utilization of 0.043 W.

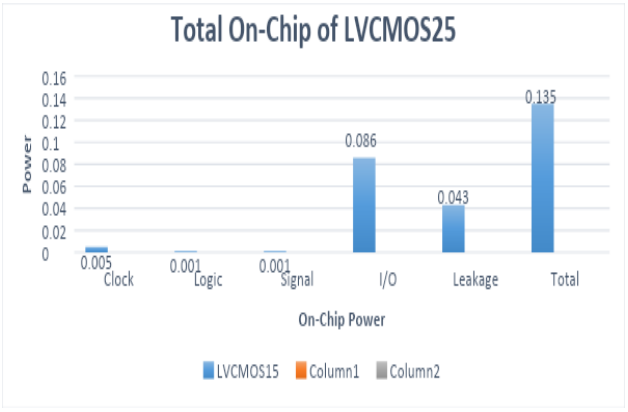

Figure 5.Power Analysis of LVCMOS25.

D. Power Analysis OF LVCMOS33.

In Figure 6, total on-chip power for LVCMOS33 is shown. For LVCMOS33 I/O standard clock power, logic power and signal power of device is same as for LVCMOS15, LVCMOS18 and LVCMOS25. For LVCMOS33, I/O power utilization is 0.146 W, leakage power dissipation is 0.044 W and total power is 0.197 W.

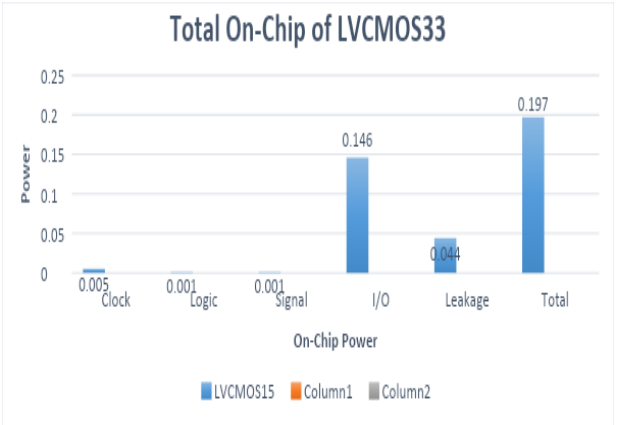

Figure 6.Power Analysis of LVCMOS33.

V. RESULT ANALYSIS

From the power analysis of all above mentioned LVCMOS I/O standard, it is observed that total power dissipation of device increases when LVCMOS I/O standard is changed. LVCMOS15 I/O standard utilizes least amount of power and LVCMOS33 consumes the highest amount of power for device operation. The total power consumption of all the LVCMOS I/O standard is shown in Figure 7. LVCMOS18 utilizes 15.4762% more power, when compared with LVCMOS15 I/O standard. LVCMOS25 consumes 60.7143% more power than LVCMOS15 I/O standard. LVCMOS33 uses 134.524% more power, when compared with LVCMOS15 I/O standard.

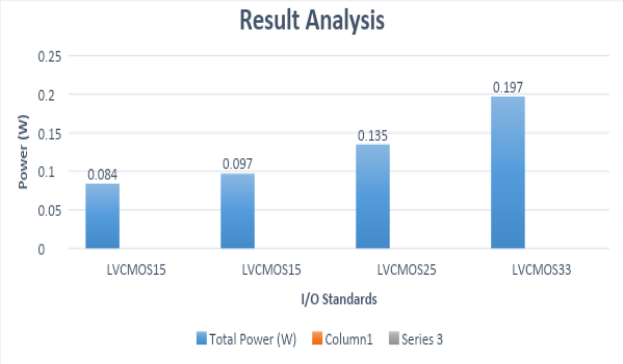

Figure 7.Total Power of LVCMOS I/O standards.

VI. CONCLUSION

In this research work, the CU circuit is interfaced with 28-nm Artix-7 FPGA. For power calculation of the device, the I/O standard of FPGA is changed. It is observed that at 1GHz of frequency device is most power efficient with LVCMOS15 I/O standard. LVCMOS33 I/O standard uses highest amount of power, so this will not be beneficial for promoting green communication.

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