Design of Low Power Transceiver on Spartan-3 and Spartan-6 FPGA

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Abstract—In this research work, a low power transceiver is designed using Spartan-3 and Spartan-6 Field-Programmable Gate Array (FPGA). In this work, a Universal Asynchronous Receiver Transmitter (UART) device is used as a transceiver. The implementation of UART is possible with EDA tools called Xilinx 14.1 and the results of the power analysis are targeted on Spartan-3 and Spartan-6 FPGA. The variation of different power of chips that are fabricated on FPGA for e.g., Input/Output (I/O) power consumption, Leakage power dissipation, Signal power utilization, Logic power usage, and the use of Total power, is observed by changing the voltage supply. This research work shows how the change in voltage influence the power consumption of UART on Spartan-3 and Spartan-6 FPGA devices. It is observed that Spartan-6 is found to be more power-efficient as voltage supply increases.

Keywords— Spartan-3, Spartan-6, Power, Voltage, Field-Programmable Gate Array (FPGA), Universal Asynchronous Receiver Transmitter (UART)

I. INTRODUCTION

In the current scenario of the world, energy crisis across the globe accounts a very major significant problem. And the energy crisis and the shortage of natural resources like crude oil, coal, etc. in India affects the economy of the country [1]. Population growth and industrial development have led the global demand for a huge amount of energy. So in order to reduce the energy consumption, we are making a UART using FPGAs which consumes less amount of power. UART stands for Universal Asynchronous Receiver Transmitter which is used for serial communication of data. In UART only two wires are required for data transmission. Not only that no clock signals are required to drive UART. When the value of voltage is at the extreme, the UART produces less noise and interference and signal can travel a longer distance [2-3]. The voltage applied to UART plays a vital role in determining the chip's power that is fabricated on FPGA. From the universal power voltage equation$P \propto V$ and $P = VI$, it is observed that power is based on voltage. Hence, in case of UART also, if the voltage supply is changed, then the input voltage (vccint) and thermal properties will change but the effective thermal resistance to

air also known as (ΘJA (°C/W)) and Voltage supply for auxiliary logic (vccaux) and Voltage supply for I/O banks 25 (vcco25) remains same. Similarly, when the supply voltage is increased, then the maximum ambient temperature increases but the junction temperature decreases.

II. RELATED RESEARCH DONE BY OTHER RESEARCHERS & METHODOLOGY

In [4], there is a UART based on asynchronous technology which consumes low power. In [5] authors by varying the frequency of FPGA designed an energy-efficient Arithmetic Logic Unit (ALU) which reduces clock and dynamic power consumption. In [6] authors using 45nm and 28nm FPGA designed an electron inducing single event upset at a nominal voltage value. In [7] authors have designed a method for analyzing the high-level utilization of FPGA power dissipation. In [8] an energy-efficient counter was designed by scaling voltage value on different FPGAs technology. In [9] authors have designed a modular feedback PID controllers system using FPGA technology. PID controllers help in saving power consumption. In [10] researchers designed an energy-efficient instruction register for green communication on FPGA. In [11] a low power frequency scaled and thermal-aware control unit design is implemented on FPGA. But in this project, we are making a UART which usage low power using Spartan-3 and 45nm Spartan-6 FPGA family.

III. EXPERIMENTAL SECTION

The UART design was implemented on Xilinx14.1 ISE design Suite using Spartan-3 and Spartan-6 FPGA. The UART module is coded in Verilog HDL (Hardware Description Language). The voltage varies from $1.1V$ to $1.5 V$ in both FPGA and power variation is analyzed using X Power Analyzer tool. This implementation is done at a frequency of 1GHz. The ambient temperature of both FPGA is $25(^0C)$ having the airflow of zero Linear Feet per Minute (LFM). Spartan-3 and 45nm Spartan-6 FPGA runs on speed grade of -5 and -3 respectively.

IV. THERMAL BEHAVIOR OF SPARTAN-3 AND SPARTAN-6 FPGA.

Effective Thermal Resistance to air (ΘJA (°C/W)) remains constant for both Spartan-3 and Spartan-6 FPGA as voltage rises from 1.1V to 1.5V. For Spartan-3 FPGA

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effective thermal resistance to air is 37.0 (ΘJA (°C/W)) and for Spartan-6 FPGA effective thermal resistance to air is 38.4 (ΘJA (°C/W)). Maximum ambient temperature (MAT) decreases and junction temperature increases for both FPGA when the voltage gets raised from 1.1V to 1.5V. Table 1 and Table 2 represents the change in thermal properties of FPGA due to the change in voltage supply.

Table 1. Thermal properties of Spartan-3 FPGA as voltage raises from 1.1V to 1.5V.

| Voltage Source (vccint) (V)	Effective Thermal Resistance (ΘJA (°C/W))	MAT (°C)	Junction Temperature. (°C)
1.1	37.0	82.8	27.2
1.2	37.0	82.7	27.3
1.3	37.0	82.5	27.5
1.4	37.0	82.3	27.5
1.5	37.0	82.0	28.0

Table 2. Thermal properties of Spartan-6 FPGA as voltage raises from 1.1V to 1.5V.

Voltage Source (vccint) (V)	Effective Thermal Resistance (ΘJA (°C/W))	MAT (°C)	Junction Temperature. (°C)
1.1	38.4	83.0	27.0
1.2	38.4	82.9	27.1
1.3	38.4	82.7	27.3
1.4	38.4	82.5	27.5
1.5	38.4	82.3	27.7

V. POWER ANALYSIS

### A. Power Dissipation at Spartan-3 FPGA.

For voltage 1.1V and 1.2V, I/O power dissipation is 0.017W and for 1.3V, 1.4V and 1.5V I/O power consumption is 0.018W. Leakage power increases as 0.026W, 0.027W, 0.029W, 0.031W and 0.034W respectively as voltage is raised from 1.1V to 1.5V. Therefore, the total power consumption also gets increased as 0.058W, 0.063W, 0.068W, 0.074W and 0.080W respectively for increment in voltage from 1.1 V with a step size of 0.1 V to 1.5 V. The voltage and power variation are shown in figure 1.
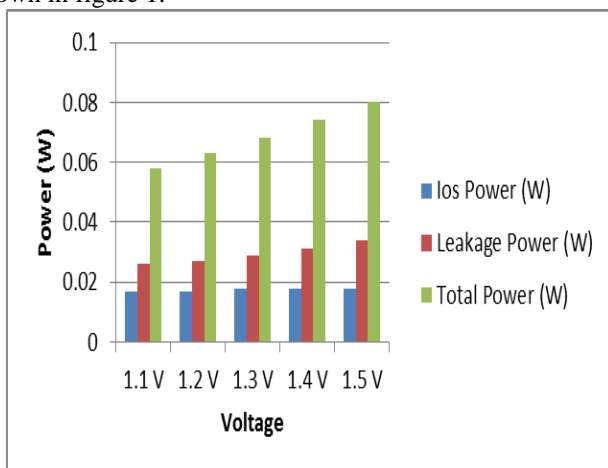
Figure 1. Power Consumption at Spartan-3 FPGA.

B. Power Utilization at Spartan-6 FPGA.

For voltage 1.1V and 1.2V, I/O power utilization is 0.025W and for 1.3V, 1.4V and 1.5V I/O power usage is 0.026W. Leakage power increases as 0.012W, 0.014W, 0.017W, 0.020W and 0.025W respectively as voltage is increased from 1.1V to 1.5V. Therefore, the total power consumption also gets increased as 0.051W, 0.055W, 0.059W, 0.064W and 0.072W respectively for increment in voltage from 1.1V with a step size of 0.1 V to 1.5V. The voltage and power variation are shown in figure 2.
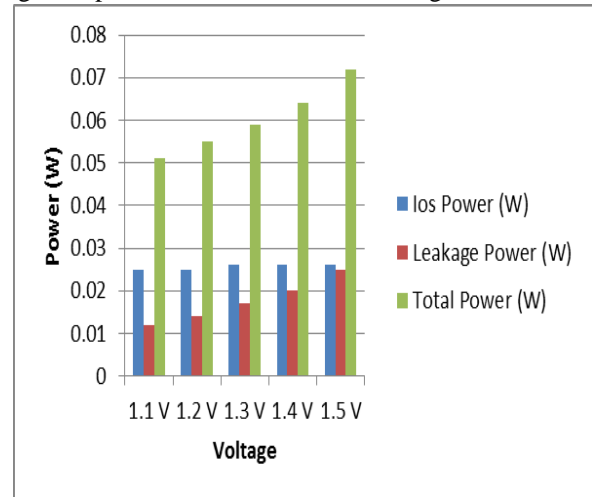
Figure 2. Power Usage at Spartan-6 FPGA.

VI. RESULTS

As compared to Spartan-6 FPGA, there is a rise of 116.667% of the total power usage for Spartan-3 FPGA when the voltage supply is at 1.1V. The increment in total power consumption for Spartan-3 FPGA at voltage 1.2V, 1.3V and 1.4V is 14.545%, 15.254%, and 15.625% respectively. For 1.5V voltage the increment in the total power consumption of Spartan-3 FPGA is 11.111% as compared to 45nm Spartan-6 FPGA. Figure 3 shows the total power comparison of the older Spartan-3 and the newer Spartan-6 FPGA.
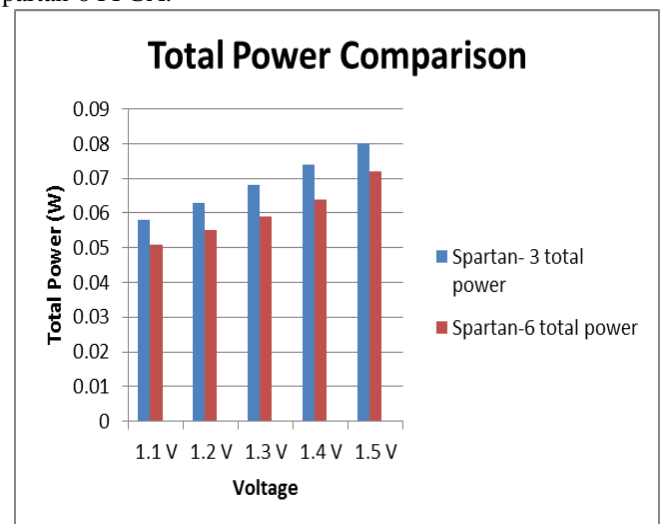
Figure 3. Total power comparison of Spartan-3 and Spartan-6 FPGA.

VII. CONCLUSION

The implementation of UART is done on Xilinx 14.1 ISE EDA tool and the results are targeted on Spartan-3 and Spartan-6 FPGA devices. The UART module is coded in Verilog HDL. In this work power consumption of the device is analyzed at a different value of voltage ranging from 1.1V to 1.5V. It is observed that as voltage increases the total power consumption of both FPGA also increases. The device consumes low power if the supply voltage is low, therefore it is concluded that Spartan-6 FPGA is most power-efficient device for UART as compared to Spartan-3 FPGA.

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