Impact of Mole Fraction Variation on Nanoscale SiGe Hybrid FinFET on Insulator

Vidhya Sagar G, VijayaKumar D

Abstract*: *This work investigates the performance of SiGe Hybrid JunctionLess FinFET (HJLFinFET) on insulator with different mole fraction x. The band gap difference for different mole fractions are explored. Impact of electrical characteristics and SCE of HJLFinFET are analyzed with fin width 10nm and varying gate length from 5nm-40nm for different mole fraction. Synopsys Sentaurus TCAD tool(sprocess and sdevice) are used in Device modelling and device simulation. Simulation results shows improvement in On current, DIBL and SS. For high performance application SiGe with mole fraction less than 0.3 at channel length less than 10nm are suitable because of the bandgap value is similar to silicon.

Keywords : SiGe, HJLFinFET, Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL), Short channel effects (SCE).

I. INTRODUCTION

Performance limitations due to scaling has become more challenging in nanoscale regime. Due to which carrier velocity saturation, high field effects, short channel effects (SCE) of electrostatic origin such as DIBL, threshold voltage shift, subthreshold degradations are given more importance. Promising devices like FinFETs, Junction less transistors, HEMT devic shows better gate control which overcomes the effect of short channel effects compared to conventional MOSFETs[1]. Moreover various materials with strained silicon, compound materials and high k dielectric for gate stack are used on few pictorializations like gate all around and Silicon on Insulator for high carrier mobility and reduced SCE. Using high-K materials reduction in leakage current across junction is achieved due to large bandgap [2,3]. Materials like strained silicon increases mobility with increase in strain and also limits mobility enhancement due to lattice dislocation. Compound materials are defined with Mole fraction x which defines the amount of composition present in mixture of compound materials with a dimensionless quantity [4]. SiGe is a material used as an alternative to Si because of its compatibility with standard Si technology. The band structure of SiGe is strongly impacted by strain, dependency of Ge mole fraction on SiGe for high mobility due to high stress is studied [6].Hetero-structure models and super lattice buried channel investigation are studied [7-9]. SOI technology is employed to reduce SCE as oxide layer isolates the channel from the bulk. The device is grown on oxide layer for better electrostatics. Moreover the advantage of SiGe as device material, it equals the bandgap value with Si due to bandgap variation caused by the mole fraction x [4]. The lattice constant of Si is x=5.431^{0}A, Ge is x=5.658^{0}A and SiGe has 4.2% of lattice mismatch respectively [19, 20]. The mole fraction x value includes lattice match and lattice constant.

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II. MATERIAL AND METHOD & METHODOLOGY

Fig. 1 depicts the 3D-schematic of n-type SiGe HJLfinFET on insulator with high-K spacer. Silicon material is used as substrate with boron doping and buried oxide material with SiO2 is deposited. SiGe is grown as an epitaxial layer on top of the oxide forming source and drain regions [10]. Uniform doping with zero doping gradient over the device represents junctionless transistor [5]. Junctionless transistors conducts with high φm that denotes the difference between the gate metal and channel material fully depletes the channel region [11-15]. To enhance better gate control over the channel and mobility, high-K spacer HfO2 is deposited. The device parameters of HJLFinFET are listed in table 1.

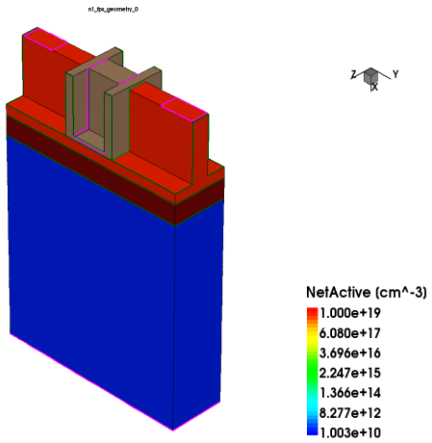


Fig. 1 SiGe Hybrid Junctionless FinFET with gate length 20nm and width 10nm.

Three dimensional (3D) device simulation are performed using Sentaurus device. For device simulation old-slotboom bandgap narrowing models are used due to high doping of the channel. Mobility degradation models such as doping dependency, high field saturation to account velocity saturation of charge carriers are included.[16-19]

Table 1. Device parameters and doping profiles

Parameter	HJLFinFET
Gate length(L_g)	20nm
Fin height(H_{fin})	30nm
Fin width(W_{fin})	10nm
Equivalent oxide thickness	0.9nm(HfO_2)
Ultra-thin body thickness	6nm
Spacer length	10nm(HfO_2)
BOX thickness	10nm
Fin dopants(Arsenic)	1 X 10^{19} cm^{-3}
Substrate dopants(Boron)	1 X 10^{15} cm^{-3}
Gate metal work function	4.6eV-4.7eV

III. RESULT AND DISCUSSION

A. Comparison of Transfer Characteristics

In this section, the DC performance of SiGe HJLFinFET is analyzed with varying channel length and temperature. Fig.2 represents the calibrated simulation of SOI junctionless FinFET and Hybrid FinFET at V_{TH}≈325mV and the result are matched [5] Fig.3 exhibits the energy band gap over the device with mole fraction x=0, 0.1, 0.3, 0.5, 0.7 and 0.9 at threshold voltage of 300mV and channel length of 20nm. It is observed that band gap value decreases with increase in mole fraction. The energy band gap varies from 1.1eV to 0.6eV due to the germanium mole fraction in SiGe material. The difference between the conduction band and valence band of Si is EG=1.1eV. EG=1eV with mole fraction of x=0.1 and EG=0.6eV for mole fraction x=0.9, which indicates the composition of germanium in SiGe at 10% and 90%. The fermi energy is zero due to high doping concentration which is close to the conduction band an added advantage for the SiGe junctionless transistor.

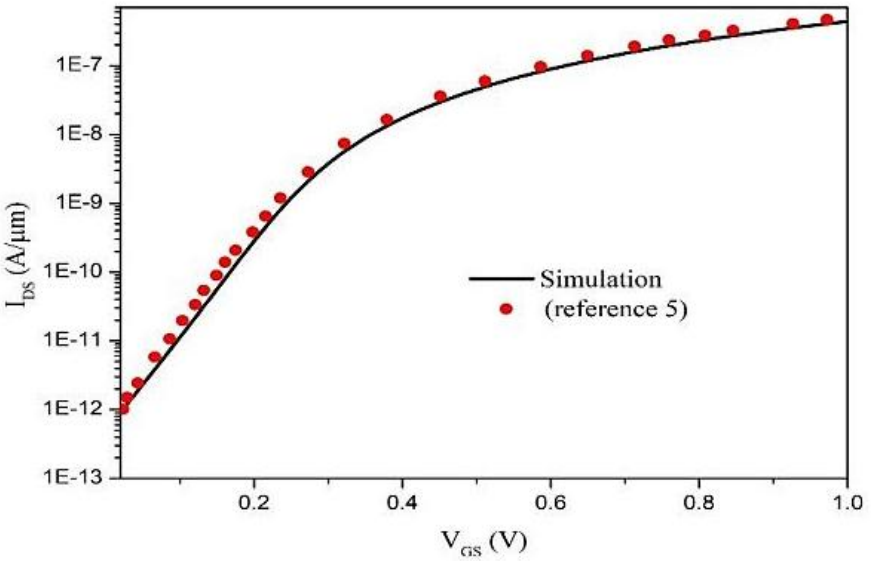


Fig.2. IDS-VGS of Junctionless transistor calibrated at VDS=1V and Lg=1μm.

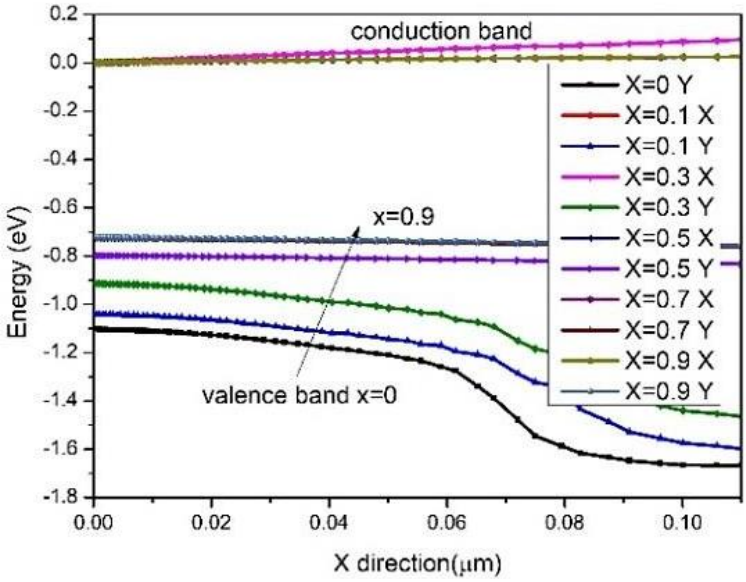


Fig.3 Energy band gap over the device for variation mole fraction.

Fig.4 shows the influence of mole fraction variations on I_{ON} and I_{OFF} with gate voltage at channel length L_g = 20nm. The on current increases with increase in mole fraction at low gate voltage when gate voltage greater than 0.7, current decreases with mole fraction 0.7 and 0.9. When gate voltage increases electric field tends to decrease. Off current decrease reduces the I_{ON}/I_{OFF} ratio.

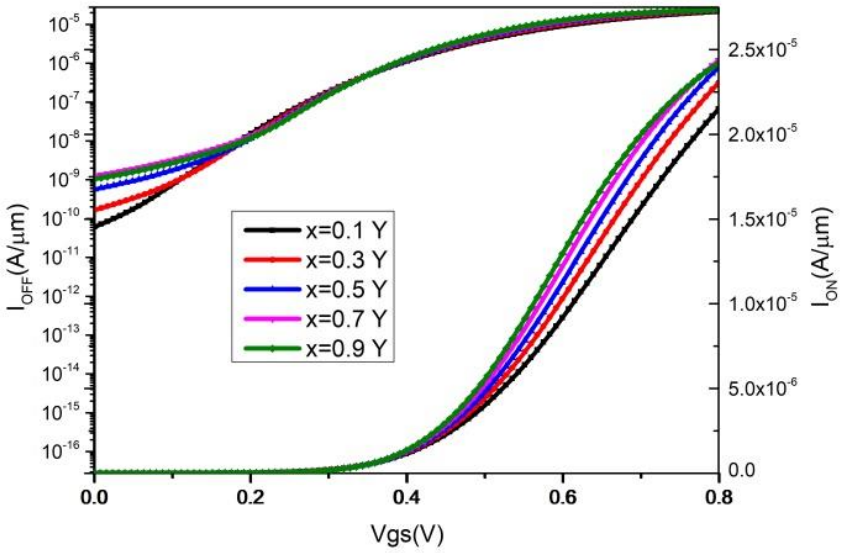


Fig.4 On-current and Off current variation over SiGe mole fraction variations at L_g=20nm and V_{TH}=300mV.

B. Transconductance and gate capacitance variation

Fig. 6 shows the impact of transconductance over different mole fraction with channel length of 20nm. Transconductance which is considered as the figure of merit for analog applications decreases as the mole fraction increases. Maximum g_m of 70μ(S) is achieved with mole fraction x=0.9 with less gate voltage. As the gate voltage increases gm decreases. Fig. 7 shows the gate capacitance impact over the mole fraction. Gate capacitance increases at low gate voltage and decreases at higher gate voltage as it directly proportional to dielectric constant. Gate capacitance decreases with increase in mole fraction. $7x10^{-17}$F is achieved with mole fraction 0.9 at low gate voltage.

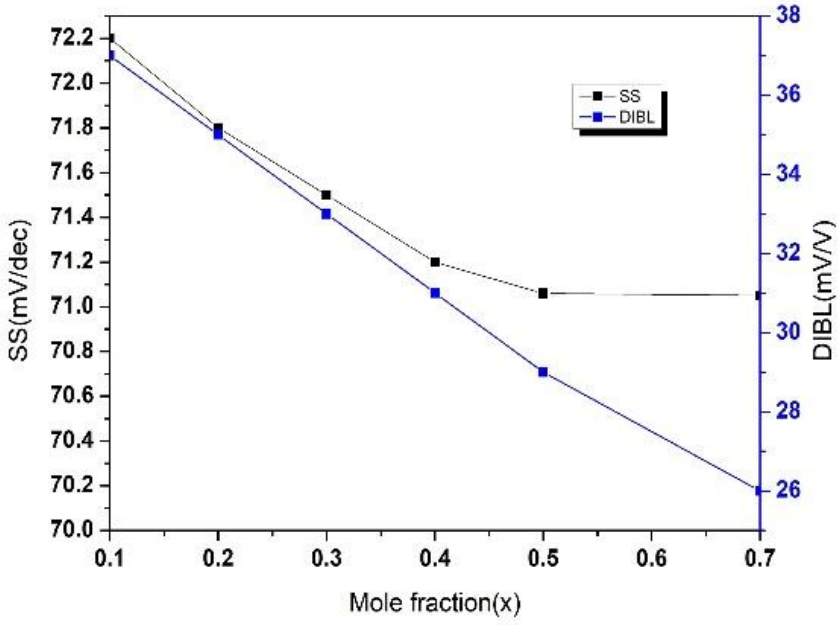


Fig.5 DIBL and SS over SiGe mole fraction variation at L_g=20nm and V_{TH}=300mV

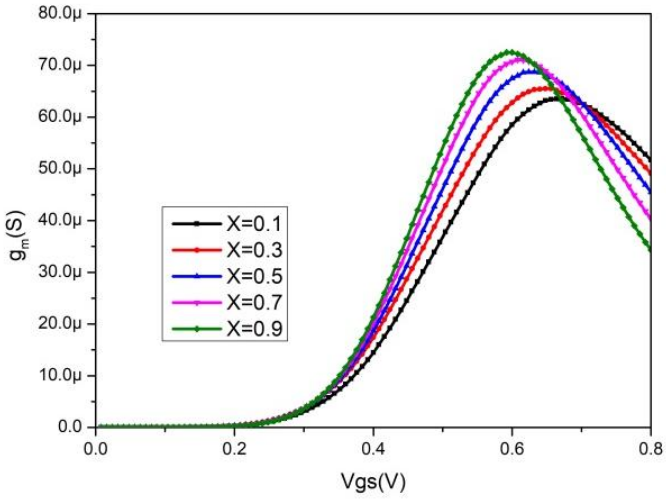


Fig. 6 Transconductance with gate voltage for different mole fraction.

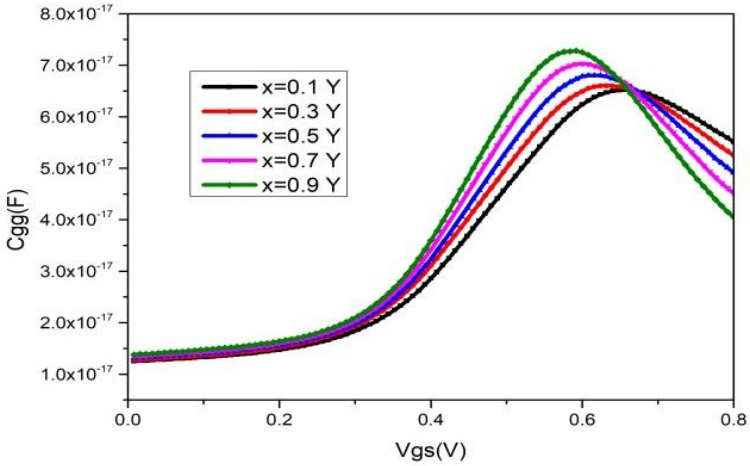


Fig.7 Gate capacitance with change in gate voltage for different mole fraction.

C. Channel length variation

Fig. 8 shows the off current variations to different channel length with mole fraction x=0.1, 0.3, 0.7 and 0.9. It is evident that when channel length increases better off current is achieved. Better I_{OFF} is obtained with mole fraction 0.1 when the channel length is less than 10nm. With germanium concentration of less than 30% in SiGe material better I_{ON}/I_{OFF} ratio is achieved.

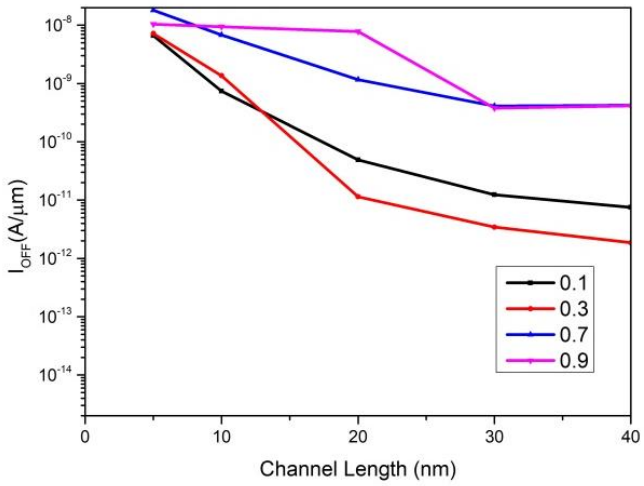


Fig.8 I_{OFF} variation to channel length with mole fractions x=01, 0.3, 0.7 and 0.9.

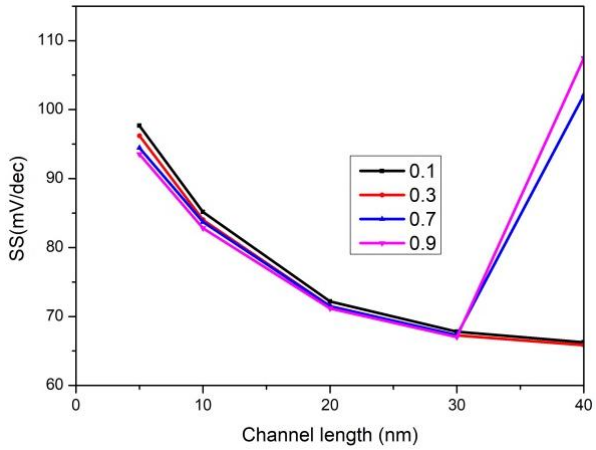


Fig.9 SS variation to channel length with varying mole fraction

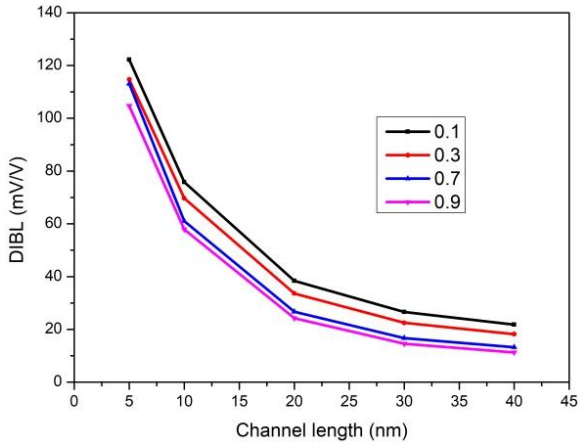


Fig. 10 DIBL variation over channel length with different mole fraction

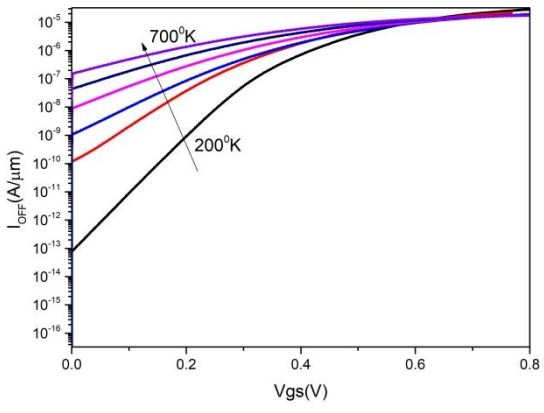
Fig.9 and 10 shows the impact of SS and DIBL of different mole fractions. SS decreases with increase in mole fraction for channel length less than 30nm. 65mV/dec is achieved at channel length of 40nm with mole fraction less than 0.3 DIBL decreases with increase in mole fraction, very less DIBL of 15mV/V is achieved at channel length 40nm with mole fraction 0.9.

Table- II: Computed parameters of $Si_{1-X}Ge_X$ HJLFinFET for different mole fraction X at $V_{D,Lin}$ =0.05 V and $V_{D,Sat}$ = 0.8V

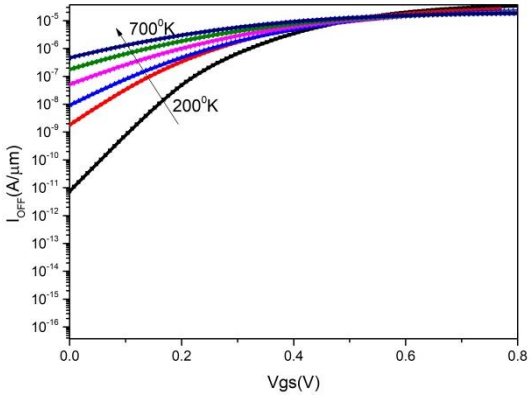
Device	X=0.1	X=0.3	X=0.5	X=0.7	X=0.9	X=0(Silicon)
V_{TH} (mV)	300	300	300	300	300	300
DIBL(mV/V)	37.7	33.04	29.27	26.24	23.7	41.8
SS(mV/dec)	72.19	71.53	71.054	71.5	71.224	72.7
I_{ON}(A/µm)	2.15 x 10-5	2.3 x 10-5	2.39 x 10-5	2.43 x 10-5	2.42 x 10-5	20.3 x 10-5
I_{OFF}(Aµ/m)	6.13 x 10-11	1.67 x 10-10	5.69 x 10-10	1.243 x 10-9	1.04 x 10-9	5.15 x 10-11

D. Temperature Variation

Fig.11 indicates the temperature variation upto 700^0K on transfer characteristics of SiGe HJLFET for mole fraction 0.1 and 0.9. Temperature variations causes different scattering phenomenon which reflects in mobility variation [20]. Better off current is achieved with decrease in temperature eventually increasing I_{ON}/ I_{OFF} ratio. It is observed that current improves over 10^3 times over temperature decrease from 300^0K to 200^0K for the mole fraction x= 0.1 and 10^2 for x=0.9. This is due to carrier concentration at high temperature. Better off current is achieved at mole fraction 0.1 around 10^{-13}.



(a)



(b)

Fig, 11 Temperature variation over I_{DS} -V_{GS} for mole fraction (a) x=0.1 and (b) x=0.9.

CONCLUSION

In this article we presented the DC characteristics of SiGe Hybrid Junction-less n-FinFET with different mole fractions. The impact of mole fraction for different channel length and temperature are investigated and concludes that mole fraction less than 0.3 witnesses better on current off current results when channel length is less than 20nm.

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