

VLSI Design of An Area & Time Efficient Design of Overloaded CDMA Architecture Using Han Carlson Adder

Arulananth TS, Praveen Sagar S, Anusha B

Abstract: On-chip interconnects are the performance bottleneck in modern system-on-chips. Code-division multiple accesses (CDMA) have been proposed to implement on-chip crossbars due to its fixed latency, reduced arbitration overhead, and higher bandwidth. In this paper, we advance overloaded CDMA interconnect (OCI) to enhance the capacity of CDMA network-on-chip (NoC) crossbars by increasing the number of usable spreading codes. Serial-OCI and P-OCI architecture variants are presented to adhere to different area, delay, and power requirements. Compared with the conventional CDMA crossbar, on a Xilinx Spartan-3E FPGA kit, the serial OCI crossbar achieves 100% higher bandwidth, 31% less resource utilization, and 45% power saving, while the parallel OCI crossbar achieves N times higher bandwidth compared with the serial OCI crossbar at the expense of increased area and power consumption. Further to increase the speed of OCI crossbar we are implementing Han Carlson adder in place of parallel adder architecture. The use of Han-Carlson adder gives better performance than the existing system by 38% area reduced and 49% speed increased.

Index Choice: Code-division multiple access (CDMA) interconnect, CDMA router, network-on-chip (NoC), NoC physical layer, overloaded CDMA crossbar, Carry Select Adder, Han Carlson adder.

I. INTRODUCTION

On-chip affect the general zone interchanges outstandingly, execution, and power employment of present day framework on-chips (SoCs). Expanding the correspondence overhead debases accelerate skilled by parallel processing as designate by Amdahl's law. In related to that, creating effective superior on-chip concatenation has remained of fundamental implication for the equidistant and elite figuring advancements. Systems on-chips are the nearly all versatile interrelationship worldview particularly fit for tending to divergent application be in need and meet distinctive execution necessities of substantial assignment including inactivity as a result of versatile steering, throughput by means of enhanced way decent variety, control dispersal by improving the web of piece to focused assignment and versatility by run-time arrangement. In web of piece information exits dealt with as bundles, this period on-chip

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Arulananth TS, Department of Electronics and Communication Engineering, MLR Institute of Technology, Hyderabad, Telangana, India

Praveen Sagar S, PG Student, Department of Electronics and Communication Engineering, MLR Institute of Technology, Hyderabad -43, Telangana, India

Anusha B, PG Student, Department of Electronics and Communication Engineering, MLR Institute of Technology, Hyderabad -43, Telangana, India

handling components Manage Components are contemplated to system hubs between associated by means of switches and switches. NoCs give an adaptable reaction for substantial SoCs, however they display expanded power utilization and huge asset overheads. The web of piece over layer lookalike parts the exchange which laid as: 1) appeal; 2) transit; 3) process; and 4) manual surfaces.

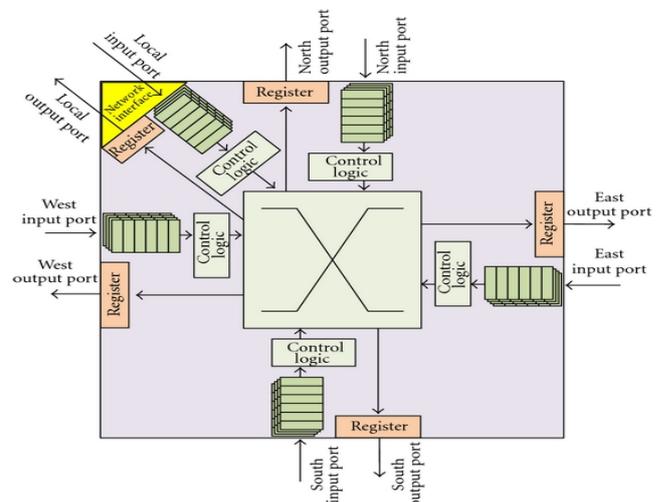


Fig.1: Representative NoC router architecture

Crosspiece is the paramount construction square of the NoCs manual surface. Crosspiece transformation has been mutual correspondence ordinary receiving numeral entrance system to empower manual bundle trade. Individually dominant asset sharing systems be awarded for extant NoCs crosspiece are's point-division numerous entrance (TDMAs), that to spot the manual connection is point to time dispensed in the middle of the interconnected PEs, and volume-analysis different access (SDMAs), to spot a committed interdependence develop linking each combine of interlinking manage components. The manual surfaces of a NoCs controller additionally accommodate diminishing with capacity gadgets.

Key-analysis numerous approach is an additional channel distribute strategy that's use the key volume to empower concurrent channel entry. In CDMA's passages, each communicate- get (TXs-RXs) match is relegated one of a kind bipolar expanding key and information open out by all connections are aggregated in an added substance correspondence medium.



The expanding set of symbols in traditional CDMA frameworks do perpendicular—curse relationship in the middle of perpendicular keys is 0 which empowers the CDMA recipient to appropriately interpret the got whole by means of a correspond decoder. Traditional CDMA frameworks hang on Wash– Hadamard right-angled keys to empower channel allocating. On-key interlinks sharing strategy for both transport and NoCs interlinked structures has been developed by CDMA. Numerous focal points of exploit CDMA for on-chip interrelated incorporate diminished power employment, settled correspondence idleness, and decreased framework many-sided quality. A CDMA switch has not so much wiring multifaceted nature than a SDMA's crosspiece and little intervention elevated than TDMA's button, in this manner it gives a decent bargain of the pair. Notwithstanding, just essential high spot of the CDMA innovation had been investigated in the on-key interlink writing.

Over-burden CDMA is a notable channel access method sent in remote interchanges from the quantity of clients allocating the correspondence medium is helped by expanding the aggregate of usable spreading codes to the detriment of expanding diverse access obstruction MAI. Over-burden CDMA's idea could connect to on-key interlinks to erect the interlinked limit.

In our past efforts, we couple the over-burden CDMA's idea for CDMA-in view of key transports, displayed couple of methodologies, to be specific, MAI-form and contrast build over-burden CDMA's interlinks, to expand this transport boundary for 25pct. and half, separately. Here, we appeal the over-burden CDMA's idea to NoC's and propel a book over-burden CDMA interconnect (OCI) crossbar sketch to expand the CDMA switch limit by 100% at negligible price. Crosspiece over-burdening depends on abusing exceptional properties of the utilized perpendicular distributing key set, to be specific, Wash– Hadamard transforms, to include an arrangement of non orthogonal spreading keys that could be peculiarly distinguished by the recipient part.

The commitments of this approach are as per the following.

- 1) Launch two novel methodologies that could be conveyed in CDMA's NoC's crosspieces to expand the switch limit, subsequently, data transfer capacity by 100% at negligible cost.
- 2) Available the OCI scientific establishments, spreading code age methodology, and OCI-based switch representations.
- 3) Enlarge and assess the OCI-construct switches worked in light of a Modelsim Artix-7 AC701 assessment pack and utilizing a 65-nm ASIC innovation for a few fabricated activity samples and look at their inertness, data transfer volume, and power application with the fundamental CDMA's and SDMA's exchanging topologies.

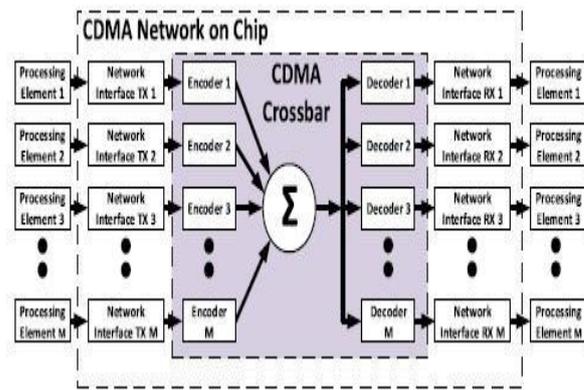


Fig.2: CDMA's basic Router Framework

II. OVERBURDEN CDMA INTERCONNECT

The CDMA switch has M transmit/get ports. The primary contrast between the over-burden and traditional CDMA switches implies M is greater than N -1 to the previous because of passage over-burdening. Every PE's is associated with couple of system combinations (NI's), transfer and get NI's segments. Amid bundle transference through a PE, the parcel is partitioned into bounces into put away in the communicate NI's 1st-load 1st yield (FIFO). The switch judge at that point chooses M appealing flutters almost by the highest point of the NIs 1st-load 1st yield to be transference amid the present exchange. They chose dances should all have a restrictive goal deliver to forestall clashes, and a champ from two clashing dances is chosen by the switches need conspire. The utilized need plot is the settled victor that takes all need plans; just a single of the transferences is given to a distributing key and is recognized to begin cryptography. When completed, the switch appoints CDMA's keys each and each transfer and gets NIs. Each of the null CDMA's keys to such an extent that their don't subscribe MAI to the CDMA's passage total NIs with exhaust FIFOs or clashing goals are relegated. Thereafter, flutters from every NIs are widened by the CDMA's keys in the cryptography block.

OCIs Crosspiece Top-plane framework:

The primary goal of this doc is expanding the quantity of doc allocating the customary CDMA's crosspiece exhibited in while charging the framework intricacy unaltered utilizing basic encoding hardware and hangs on the aggregator decoder with insignificant converts. To accomplish this objective, a few adjustments to the traditional CDMA crossbar are progressed. A similar design is reproduced for a multi bit CDMA switch. All TXs-RXs ports allocating the CDMA's switch, and distribute information from the sender ports are included exploiting a math double snake having M paired sources of info and a m-bit yield, where m = log2M. The snake is executed in both the reference and pipelined designs.

Dissimilar to perpendicular distributing keys, those are XOR with the coupled information piece& AND door is used to distribute information utilizing non perpendicular



distributing keys. An AND entryway cryptography fills in as takes after: if the communicated material piece is "0," it posts a flood of 0's amid the utter distributing cycle, which is not source MAIs into the passage; if the communicated material piece was "one," the cryptographer passes a non perpendicular distributing key. Consequently, the extra MAIs distributing key shall further subscribe a MAIs estimation of 1 or 0 to every cycle in the clock in light of the fact that the cryptography is an AND entryway. The XOR concealed of the normal CDMA's crosspiece can't be utilized to conceal the OCIs keys since it just supplements the distributing key chips, then a XOR door will make MAIs the crosspiece whether the particulars data is "zero" or "one." Both perpendicular and non perpendicular allocating with a XOR entryway, an AND entryway is growed by a mixture encoder, and a heterogeneous unit, as appeared in Fig. 2. Couple of polyglot originates are actualized for perpendicular and non perpendicular message.

OCIs Key Outline

The Walsh– Hadamard distributing key group has included belongings that empower CDMA's interrelate over-burdening. Contrast in middle of any back to back passage totals of information distribute by the perpendicular distributing keys for an non even numeral of TXs-RX sets M is constantly not odd, paying little heed to the spread information. This property implies that for the N – 1 TX-RX sets utilizing the Walsh perpendicular codes, one can modify extra N – 1 material bits in continuous contrasts in middle of the N chips creating the perpendicular key. Along these lines, abusing this property empowers including 100pct non perpendicular distributing keys which can twofold the limit of the common CDMA's cross piece. Given the key plan procedure, scientific establishments, and the deciphering subtle elements of the OCI codes in this region.

Notation	Description
N	Orthogonal spreading code extent
M	Number of attached ports Number of crossbar rattle wires
S	Sum of CDMA chips carried by the channel
d_c	Data bit encoded by an orthogonal CDMA code
d_T	Data bit encoded by an non orthogonal TDMA code
$C_o(j)$ T(j)	The j th chip of quadratical CDMA code The j th chip of non quadratical TDMA code
C_n	TDMA MAI code (non-orthogonal spread data)

Table I: Table of Notations

OCIs Crosspiece Constructing Modules

There are couple of variations are acknowledged to each and every OCIs crosspiece, authority and channeled designs. The channeled engineering is actualized to expand the crosspiece working recurrence, and thusly, data transmission by rattled nonworking channeling memories to diminish the crosspiece basic way. The OCIs crosspiece made out of mainly these below probity building pieces: a) the entangler covers; b) the disentangle covers; and c) the crosspiece snake squares, those are portrayed to accompanying.

Crosspiece monitor

By the start of every crosspiece exchange, the monitor allots distributing keys to various entangles. The task of perpendicular disseminating keys to get ports is settled, that means does not modify among the stake exchanges. Appropriately, by a switch port to start the correspondence with the get dock it locations, its entangler have got be doled out a distributing key that equivalent the foreordained disentangler.

Cross Entangler

The entangler is half and half, it can modify both perpendicular and non orthogonal information. A transferred information data is XOR ed/AND ed with the distributing key to create the perpendicular/non orthogonal distribute information, separately. A multiplexer picks between the orthogonal and non orthogonal contributions as indicated by the code compose appointed to the entangler. The entangler is duplicated N times for the P-OCI crossbar.

Execution Evolution

In this area, OCIs Crosspiece Extension an examination amongst the customary CDMA's, T-OCIs, and the P-OCIs crosspieces was drawn. A crosspiece comprising various TXs-RXs docks crosspiece. Entire CDMA crosspiece structures in both the referral and channeled variations are actualized and approved on an Artiix-7 AC-701 assessment pack. The created crosspieces are assessed for various distributing key durations N = {8, 16, 32, 64}.

The crosspiece recurrence diminishes with expanding N for two over-burdens and conventional CDMA's crosspiece for that reason that of the expanding computational multifaceted nature of the rattled. Thus clock recurrence of the P-OCIs crosspiece is greater than that of the T-OCIs crosspiece because of the nonappearance of the exceedingly stacked proportion counter and little narrowing storages displayed in the T-OCIs crosspiece. For a settled N, the upgrade of the CDMA's crosspiece transfer quickness for the P-OCIs and T-OCIs crosspieces over the established CDMA's crossbars is notable. The CDMA's crosspiece data transfer capacity BW's is gives the accompanying condition for most of the part:

$$BW = W f_c \frac{M}{T} \tag{4}$$

Here W is the width in digits, f_c is the crosspiece clock recurrence, and M is the quantity of crosspiece docks, and is the amount of clock cycle to encode single bit of information from entire docks.

OCI for NoCs

To think about the adequacy of the OCIs crosspiece in a almost working NoC's, a 65-hub orb geology is fabricated utilizing 5 OCIs switches, every singleton of the 13 PE's is associated by the OCI's switch to N = 8, and the 5 OCI's switches are interlinked by a SDMA's focal switch. To T-OCIs-and P-OCIs-based NoC's are contrasted and 64-hub, 16 bit bounce, and 8 ary 2-3D square torus SDMA's-formed NoC's created by the (CONNECT) device .



A 65-hub OCIs-formed orb NoC's were acknowledged & contrasted and a SDMA's-formed torus NoCs produced by CONNECT. The assessment comes about show the predominance of the OCIs-formed NoC's as far as region and throughput.

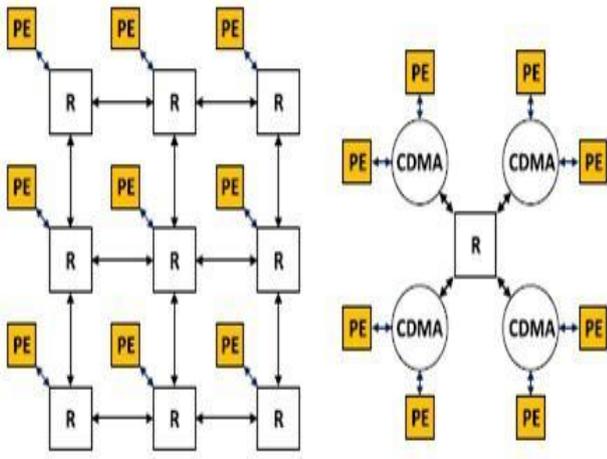


Fig.3: (a) CONNECT torus geology (b) vs the OCIs orb geology.

Fig.3 representing the torus geology utilized to the CONNECT NoC's vs the orb geology embraced for the OCIs NoC's. The orb geology is decided for these OCIs since the change of the OC Interlinked many-sided quality again the SDMA's switch increments as per the quantity of docks increments because of the straight increment in the OCIs crosspiece region contrasted with the drastic increment in the SDMA's crosspiece region.

Augmentation Method

In Overloaded-CDMA crossbar we have snake hardware to build on the encoded messages cooperatively to create total flag. We are accomplishing the increases with ordinary snake which takes vast postponement for parallel augmentations.

In the augmentation technique to enhance the execution of the OCI crossbar Han-Carlson snake is utilized as a part of the place of parallel viper design which brought about increment in the speed of the OCI crossbar.

Han-Carlson Topology.

A. Prefix Addition

The parallel expansion issue can be all-inclusive as takes after: given n-bit augends $A = a_{n-1}, a_{n-2}, \dots, a_0$ and an n-bit rattled $B = b_{n-1}, b_{n-2}, b_0$. Produces n-bit sum $S = s_{n-1}, s_{n-2}, \dots, s_0$. Allow us to visible as C_i the do of the i^{th} bit the entire piece S_i and the convey C_i can be registered as takes after.

$$s_i = a_i b_i c_{i-1} \quad (5)$$

$$c_i = a_i b_i + a_i c_{i-1} + b_i c_{i-1} \quad (6)$$

In prefix expansion we utilize three phases to enroll the total pre-handling, prefix-preparing and post-planning. In the pre-dealing with organize the create g_i and spread p_i flag are figured as:

$$g_i = a_i \cdot b_i \quad (7)$$

$$p_i = a_i b_i \quad (8)$$

The statement $g_i = 1$ implies that convey is created at bit i . While this condition $p_i = 1$ implies that a help is proliferated

through piece i . The idea of create and spread can be stretched out to a square of adjoining words, from bit k to bit i (with $k < i$) as takes after:

$$g[i:k] = \{g[i:i] = kg[i:j] + p[i:j]g[l:k] \text{ else} \quad (9)$$

$$p[i:k] = \{p[i:i] = kp[i:j]p[l:k] \text{ else} \quad (10)$$

Where: $i \geq l \geq j \geq k$

This statement $g[i:k]$ implies that a convey is created in the square $k-1$, while the infirmity $p[i:k]$ implies that a help is engendered through the piece. Along these lines, for any piece i the convey C_i can be interfaced as:

$$C_i = g[i:0] + p[i:0]c_{i-1} \quad (11)$$

Where C_{-1} is the particulars convey of the n-bit snake. In the accompanying, for straight forwardness, we accept that $C_{-1} = 0$, so that above equation follows as: $C_i = g[i:0]$

The square create and proliferate terms are enlisted in the prefix-planning period of the viper. To that reason, the $(g[i:k], p[i:k])$ couples are spoken with the help of the prefix administrator portrayed as takes after $(g[i:k], p[i:k]) = (g[i:j], p[i:j]) \bullet (g[l:k], p[l:k]) = (g[i:j] + p[i:j]g[l:k], p[i:j]p[l:k]) \quad (12)$

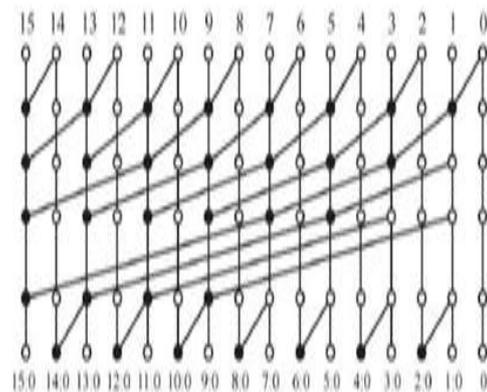


Fig.4: Han-Carlson parallel-prefix physiographic. n=16

III. SYNTHESIS AND IMPLEMENTATION OF THE DESIGN

The outline must be orchestrated and actualized before it can be checked for accuracy, by running practical reenactment or downloaded onto the prototyping board. With the best level Verilog record opened (should be possible by double tapping that document) in the HDL manager window in the correct portion of the Project Navigator, and the perspective of the task being in the Module see, the execute plan choice can be found in the process see. Outline passage utilities and Generate Programming File alternatives can likewise be found in the process see. The previous can be utilized to incorporate client requirements. To incorporate the plan, tapping 2 times on the Synthesize Design alternative in the Processes window.



To execute the outline, double tap the Implement plan alternative in the Processes window. It will experience steps like Translate, Map and Place and Route. On the off chance that any of these means wasn't possible or finished with mistakes, it will put a X stamp before that, generally a tick check will be put after every one of them to demonstrate the fruitful culmination. On the off chance that everything is done effectively, a tick stamp will be put before the Implement Design alternative. On the off chances that there are notices, I can see stamp before the alternative showing that there are a little notices. One can take a gander at the notices or blunders in the Console window exhibit at the base of the Navigator window. Each timing the outline record is spared; every one of these imprints vanishes requesting a new aggregation.

IV. SIMULATION RESULTS

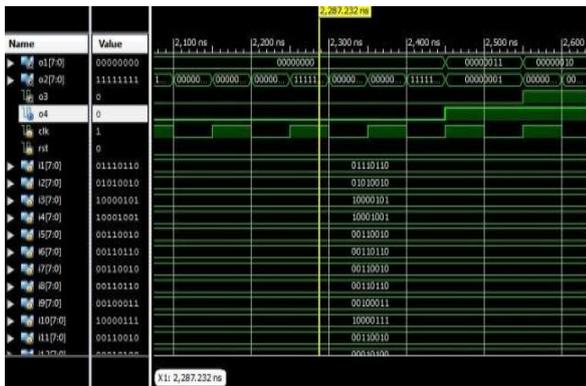


Fig.5-a: Simulation

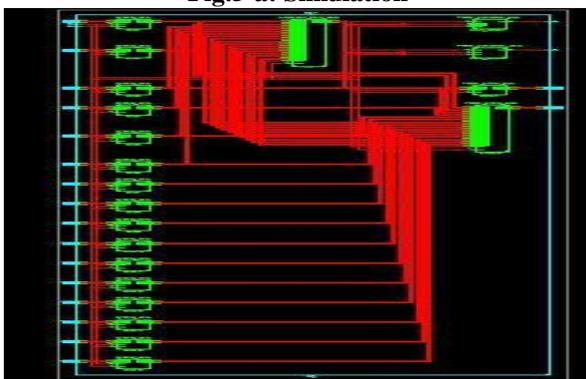


Fig.5-b:Technology Schematic

The above figure 5.a shows the simulation result of the proposed CDMA Architecture and Technology Schematic in figure 5.b. These are obtained in the tool Xilinx.

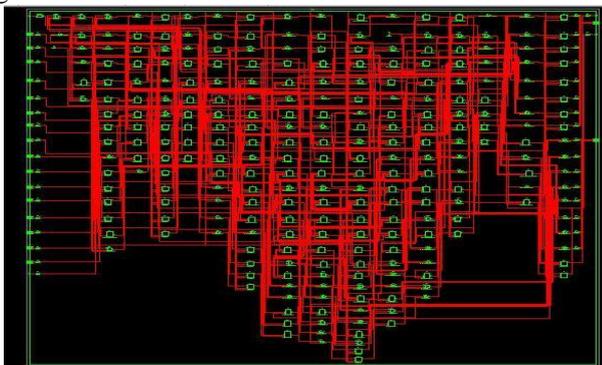


Fig.5-c: RTL schematic

This is the RTL schematic of the proposed Overloaded CDMA Architecture which will give detailed view of each and every module connection.

Device utilization summary (estimated values)			
Logic utilization	Used	Available	Utilization
Number of slices	42	960	4%
Number of slice flip flops	46	1920	2%
Number 4 input LUTs	73	1920	3%
Number of bonded IOBs	27	66	4%
Number of GCLKS	1	24	4%

Table II: Design and summary

The above table shows the FPGA Device Utilization detailed summary by comparing the used devices with the available devices. Based on this we can estimate the Area efficiency.

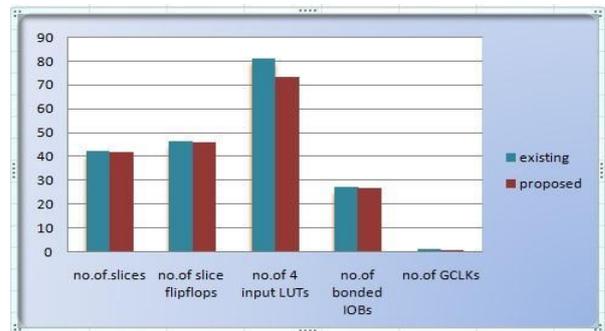


Fig.6: Comparison of prevailed and augmented project

Device	On-Chip	Power (W)	Used	Available	Utilization (%)	Supply Summary	Total	Dynamic	Quiescent
Family	Spartan6e		Logic	43	1920				
Part	xc6s100e		Signals	75		Source	Voltage	Current (A)	Current (A)
Package	vq100		I/Os	50	66	Vccint	1.200	0.008	0.000
Grade	Commercial		Leakage	0.024		Vccaux	2.500	0.008	0.000
Process	Typical		Total	0.034		Vcc0v25	2.500	0.002	0.000
Speed Grade	-5								
Environment			Effective TjA	Max Ambient	Junction Temp				
Ambient Temp (C)	25.0		(C/W)	(C)	(C)	Supply Power (W)	Total	Dynamic	Quiescent
Use custom TjA?	No			49.0	83.4		0.034	0.000	0.034
Custom TjA (C/W)	N/A								
Airflow (LFM)	0								

Fig.7: Power Consumption

Above figure shows the total power consumed by the proposed Overloaded CDMA Architecture. The total power will come from the Dynamic power and the quiescent power.

V. CONCLUSION

From this novel, we presented that the idea of over-burden CDMA's crosspieces for the manual surface empowering agent of the NoC's switches. In over-burden CDMA's, the correspondence passage is over-burden along to non orthogonal keys to expand the channel limit. Here couple of crosspiece structures that utilize the over-burden CDMA's idea, specifically,



T-OCIs and P-OCIs, are progressed for expand the CDMA's crosspiece limit by 100pct. and $2N \times 100$ pct, separately; here N is the distributing key duration. We abused highlighted belongings of this Walsh's distributing key kindred bring into effective action in the established CDMA's crosspiece to enlarge the quantity of transformation docks distribute the crosspiece lack adjusting the straightforward gatherer decrypt err engineering of the regular CDMA's crosspiece. Age techniques of non orthogonal distributing keys are exhibited alongside the referral and channeled structures for every crosspiece variation. The T-P-OCI crosspieces were accomplished & approved on a Modelsim Artix7 AC-701 FPGA assessment pack.

Then execution of the OCIs crosspieces is contrasted and that of the customary CDMA's crosspiece. The forceful potential is lessened by 45pct. for the T-OCIs crosspiece yet expanded by 133percentum for the P-OCIs crosspiece. The T-OCIs crosspiece uses 31pct. less assets, along the P-OCIs crosspiece utilizes 400percentum more assets contrasted and the systematic CDMA's crosspiece. The T-P-OCIs crosspieces with Han-Carlson rattle is contraption and confirmed on a modelsim ISE design Suite. The usage of Han-Carlson rattle gives superior performance apart from the breathe system by 38 proportion and area diminished and 49% velocity enlarged.

REFERENCES

1. K. Asanovic et al., "The landscape of parallel computing research: A view from Berkeley," Dept. EECS, Univ. California, Berkeley, CA, USA, Tech. Rep. UCB/EECS-2006-183, 2006.
2. P. Bogdan, "Mathematical modeling and control of multifractal workloads for data-center-on-a-chip optimization," in Proc. 9th Int. Symp. Netw.-Chip, New York, NY, USA, 2015, pp. 21:1-21:8.
3. Z. Qian, P. Bogdan, G. Wei, C.-Y. Tsui, and R. Marculescu, "A traffic-aware adaptive routing algorithm on a highly reconfigurable network-on-chip architecture," in Proc. 8th IEEE/ACM/IFIP Int. Conf. Hardw./Softw. Codesign, Syst. Synth., New York, NY, USA, Oct. 2012, pp. 161-170.
4. Y. Xue and P. Bogdan, "User cooperation network coding approach for NoC performance improvement," in Proc. 9th Int. Symp. Netw.-Chip, New York, NY, USA, Sep. 2015, pp. 17:1-17:8.
5. T. Majumder, X. Li, P. Bogdan, and P. Pande, "NoC-enabled multicore architectures for stochastic analysis of biomolecular reactions," in Proc. Design, Autom. Test Eur. Conf. Exhibit. (DATE), San Jose, CA, USA, Mar. 2015, pp. 1102-1107.
6. S. J. Hollis, C. Jackson, P. Bogdan, and R. Marculescu, "Exploiting emergence in on-chip interconnects," *IEEE Trans. Comput.*, vol. 63, no. 3, pp. 570-582, Mar. 2014.
7. S. Kumar et al., "A network on chip architecture and design methodology," in Proc. IEEE Comput. Soc. Annu. Symp. (VLSI), Apr. 2002, pp. 105-112.
8. T. Bjerregaard and S. Mahadevan, "A survey of research and practices of network-on-chip," *ACM Comput. Surv.*, vol. 38, no. 1, 2006, Art. no. 1.
9. Y. Xue, Z. Qian, G. Wei, P. Bogdan, C. Y. Tsui, and R. Marculescu, "An efficient network-on-chip (NoC) based multicore platform for hierarchical parallel genetic algorithms," in Proc. 8th IEEE/ACM Int. Symp. Netw.-Chip (NoCS), Sep. 2014, pp. 17-24.
10. D. Kim, K. Lee, S.-J. Lee, and H.-J. Yoo, "A reconfigurable crossbar switch with adaptive bandwidth control for networks-on-chip," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2005, pp. 2369-2372.
11. R. H. Bell, C. Y. Kang, L. John, and E. E. Swartzlander, "CDMA as a multiprocessor interconnect strategy," in Proc. Conf. Rec. 35th Asilomar Conf. Signals, Syst. Comput., vol. 2. Nov. 2001, pp. 1246-1250.
12. C. C. Lai, P. Schaumont, and I. Verbauwhede, "CT-bus: A heterogeneous CDMA/TDMA bus for future SOC," in Proc. Conf. Rec. 35th Asilomar Conf. Signals, Syst. Comput., vol. 2. Nov. 2004, pp. 1868-1872.
13. S. A. Hosseini, O. Javidbakht, P. Pad, and F. Marvasti, "A review on synchronous CDMA systems: Optimum overloaded codes, channel capacity, and power control," *EURASIP J. Wireless Commun. Netw.*, vol. 1, pp. 1-22, Dec. 2011.
14. K. E. Ahmed and M. M. Farag, "Overloaded CDMA bus topology for MPSoC interconnect," in Proc. Int. Conf. ReConfigurableComput. FPGAs (ReConFig), Dec. 2014, pp. 1-7.
15. K. E. Ahmed and M. M. Farag, "Enhanced overloaded CDMA interconnect (OCI) bus architecture for on-chip communication," in Proc. IEEE 23rd Annu. Symp. High-Perform. Interconnects (HOTI), Aug. 2015, pp. 78-87.
16. T. Nikolic, G. Djordjevic, and M. Stojcev, "Simultaneous data transfers over peripheral bus using CDMA technique," in Proc. 26th Int. Conf. Microelectron. (MIEL), May 2008, pp. 437-440.
17. T. Nikolic, M. Stojcev, and G. Djordjevic, "CDMA bus-based onchip interconnect infrastructure," *Microelectron. Rel.*, vol. 49, no. 4, pp. 448-459, Apr. 2009.
18. T. Nikolić, M. Stojčev, and Z. Stamenković, "Wrapper design for a CDMA bus in SOC," in Proc. IEEE 13th Int. Symp. Design Diagnostics Electron. Circuits Syst. (DDECS), Apr. 2010, pp. 243-248.
19. J. Kim, I. Verbauwhede, and M.-C. F. Chang, "Design of an interconnect architecture and signaling technology for parallelism in communication," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 8, pp. 881-894, Aug. 2007.
20. X. Wang, T. Ahonen, and J. Nurmi, "Applying CDMA technique to network-on-chip," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 10, pp. 1091-1100, Oct. 2007.
21. W. Lee and G. E. Sobelman, "Mesh-star hybrid NoC architecture with CDMA switch," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2009, pp. 1349-1352.
22. Halak, T. Ma, and X. Wei, "A dynamic CDMA network for multicore systems," *Microelectron. J.*, vol. 45, no. 4, pp. 424-434, Apr. 2014.

