Design and Implementaion of Energy Efficient Muliplier Architecture in Low POWER Vlsi

Rajendra Prasad

Abstract: The Low power multipliers having high clock frequencies assume a significant role in the present advanced technology. Multiplier is such a vital component which subsidises the aggregate power utilization in a systematic environment. Low Power VLSI optimization is carried out from basic subsystem level to architecture level. Power reduction is addressed at every stage of design thus the overall power reduction is minimized. Various innovative design techniques namely, clock gating, power gating and low power libraries are adopted to minimize power dissipation. The techniques proposed in this publication can be generalized and adopted for design complex signal processing and communication blocks required for various applications. To estimate 2's complement of multiplicand for final Partial Product Row (PPRG) we used MBE technique in proposed system. The proposed multiplier consumes power up to 60% and reduce the logic delay up to 7.2% and route delay up to 92%. So compared to all existed multipliers, the proposed multiplier produces effective results.

KEY WORDS: Low power multipliers, Digital Signal Processing, Power Reduction Techniques, High Clock Frequencies, Modified Booth Encoding (MBE), Partial Product Row Generation (PPRG).

I. INTRODUCTION

As we know that in the areas of system on chip and VLSI designs, the low power circuit designs is an important issue. As the dimensions of transistors are shrunk into the deep sub-micron region, the effect of static leakage currents becomes more significant. This aspect of power consumption can be controlled to some extent by novel design, but is predominantly handled by process engineering. As the dimensions of transistors are shrunk into the deep sub-micron region, the effect of static leakage currents becomes more significant. Two areas that have been the focus of active research are asynchronous logic and adiabatic logic. If the power reducing properties of these techniques could be combined, then it should be possible to produce a logic design methodology that is only active when it is performing useful computations, and recycles a large proportion of the energy used to perform those computations. Working in asynchronous fashion to get the advantages of both the techniques.

Scaling of transistor geometries have led to integration of millions of devices in a very small space, thus driving realization of complex applications on hardware and supporting high speed applications. While the basic principles are largely the same, the design practices have changed enormously because of the increases in and transistor budgets and clock speeds, the growing challenges of power consumption, and the improvements in productivity and design tools. Device scaling has increased the operating frequency of many applications, but has led to high power consumption.

This synergy has revolutionized not only electronics, but also industry at large. In order to reduce power, many researchers, designers and engineers have come up with many innovative techniques and have patented their ideas. Nevertheless, designers will need to budget and plan for power dissipation as a factor nearly as important as performance and perhaps more important than area. Low power techniques have been successfully adopted and implemented in designing complex VLSI circuits. As the demand for faster, low cost and reliable products that operate on remote power source performing high end applications keep increasing, there is always a need for new low power design techniques for VLSI circuits. Multiplication is an expensive and time consuming operation. The execution of numerous computational issues is commanded by the speed at which an augmentation activity can be executed. This perception has for example incited coordination of finish augmentation unit in condition of state of art of digital signal processors and microprocessor. Multipliers are as a result complex adder Arrays. In this work, the examination of multiplier is completed to optimize the execution of complex circuit topological. The least difficult and most well-known duplication technique is included and shift algorithm. In parallel multipliers quantities of incomplete items to be included is the fundamental parameter that decides the execution of multiplier. Hence in this work, the basic way that decides the most extreme delay in parallel multiplier is distinguished and advanced utilizing power. Likewise the aggregate power utilization of the distinctive multipliers is resolved and low power methods are consolidated to limit the power. With the end goal to accomplish rapid of activity in increase, the pattern is resort parallel multipliers. Be that as it may, the execution of the multiplier is dictated by number of parallel items to be included. In this paper we recognize and streamline the basic way that decides the extreme interruption in parallel multipliers.

II. LITERATURE SURVEY

In DSP systems multiplier plays an important role. But in DSP system mostly they perform filtering and convolution operations. Instead of that the multiplier operation plays very crucial role in DSP systems. Day by day innovative technology is being developed vigourously. Fundamental technology is used in public key cryptography for the

process of addressing. Various technologies are proposed but each technology has its own way of representation. But there are no such type of techniques which doesn't provides key agreement and public encryption. The most fundamental type of augmentation comprises of framing the result of two unsigned numbers. A wide range of sorts of multipliers have been proposed with altogether different equipment necessities, throughput and power scattering. These include: sequential multipliers, serial multipliers, array multipliers and tree multipliers.

Array multipliers and tree multipliers are quick however costly as far as equipment and power utilization. Iterative structures permit an exchange off among execution and equipment prerequisite. Pipe lining is typically utilized in iterative frameworks to enhance their execution. In the mid 1950's, multiplier execution was essentially enhanced with the presentation of booth multiplier and the advancement of quicker adders and memory segments. Corner's strategy and the altered stall's technique don't require a remedy of the item when either (or both) of the operands is negative for two's supplement numbers. Amid the 1950's, snake's structures moved far from the moderate

Successive arrangement of conveyed executed by swell convey adders convey look forward, convey select, and restrictive a few adders yielded rapid aggregates through the quicker synchronous or parallel age of bearers.

In the 1960's two classes of parallel multipliers were characterized.The five star of parallel multipliers utilizes a rectangular exhibit of indistinguishable combination cells to create and total the incomplete item bits. Multipliers of this compose are called Array multipliers. Because of the consistency of their structures, exhibit multipliers are conveying to format and have been executed as often as possible. The below average of parallel multipliers lessens a lattice of fractional item bits to two words through the key use of counters or blowers.

In Array multiplier, the two fundamental elements of halfway item age and summation are consolidated. For unsigned N by N augmentation, N2+N-1 cells, where N2 contain an AND entryway for fractional item age and a full snake for summing and N-1 cells containing a full viper, are associated with create a multiplier. The exhibit creates N bring down item bits straightforwardly and utilizes a Carry-spread viper, for this situation a swell convey snake, to frame the upper N bits of the item. With the end goal to plan a cluster multiplier for two's supplement operands, Booth calculation can be utilized. The execution of a stall's calculation cluster multiplier registers the halfway items by inspecting two multiplicand bits at once. With the exception of empowering utilization of two's supplement operands, this present stall's calculation cluster multiplier offers no execution or territory advantage in contrast with the fundamental exhibit multiplier. Better postponements, however can be accomplished by executing a higher radix adjusted stall calculation. Another strategy for building a cluster multiplier that handles two's supplement operands was displayed by Baugh. This strategy builds the most extreme segment stature by two. This may prompt an extra phase of fractional item decrease, along these lines expanding by and large deferrals.

As indicated by Thomas Callaway and Earl E. Swartz lander. Jr, segment pressure multipliers are highly power effective than any other source. In 1964, Wallace presented a proposal for quick augmentation dependent on the halfway item bits on parallel utilizing a tree of convey spare adders which turned out to be by and large known as the Wallace tree. Dada later refined Wallace's technique by characterizing a counter position methodology that required less counters in the fractional item decrease organize at the expense of a bigger convey proliferate snake. For the two strategies, the aggregate deferral is relative to the logarithm of the operand word-length

III. SOURCES OF LOW POWER CONSUMPTION IN MULTIPLIERS

To substantiate the power consumption in any CMOS circuits the sources of power consumption should be explored first. Figure (1) represents the sources of power consumed in a CMOS.
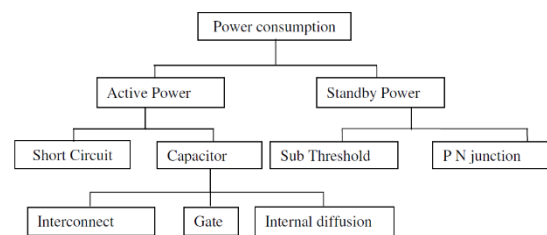

Fig. 1. Sources of low power consumption in VLSI

The active power comprises of two machine modules: (i) Capacitive or Dynamic power (ii) Short Circuit power. Capacitive power is due to capacitive loads. Capacitive loads include interconnects, output gate capacitance and input gate capacitance. The standby mode consists of two components: (i) Sub threshold (ii) Junction. The junction power is due to PN junctions in a MOS device. The gate capacitance CM is an internal capacitance, connected between the common point of the gate of NMOS and PMOS with drain of NMOS. The Load capacitance CL is made up of bulk to drain capacitances of both PMOS and NMOS, interconnect capacitance and gate capacitance of the load. During transition of input and output of an inverter, charging current (Ip), discharging current (In), ICM and ICL are of prime importance for power analysis as they are used to charge and discharge the load capacitance. These currents are the sources of power dissipation, as they get diffused into the ground during circuit transition. Capacitive or Dynamic or Switching Power: During the output voltage logic transition period (charging and discharging of the load capacitance), the power dissipated at that period is called as dynamic power. When the input changes from 0(Low) to 1(High), PMOS device changes its state from ON to OFF. During this state, PMOS transistor changes from linear to cut off region. The charging current from VDD charges the load capacitance during input being logic '1'. When input switches from logic '1' to '0', NMOS goes from cut off region to saturation and PMOS remains in cut off condition.

Short-Circuit Power: During input switching, there would be a point at which both NMOS and the PMOS transistors are conducting simultaneously and the power supply is directly connected to ground for a short interval of time.

IV. LOW POWER DESIGN TECHNIQUES ON MULTIPLIERS

Several low power techniques have been reported in the literature for power drop. At the entry level and circuit level, power reduction is achieved by incorporating additional logic that can control the charging and discharging of current. David Flynn elucidated the power reduction methods that are known as mature technologies. The four power different power reduction techniques are (i) Clock gating (ii) Gate level power optimisation (iii) Multi Vdd technique (iv) Multi Vt technique. The below figure (2) shows the different types of techniques of multiplier.
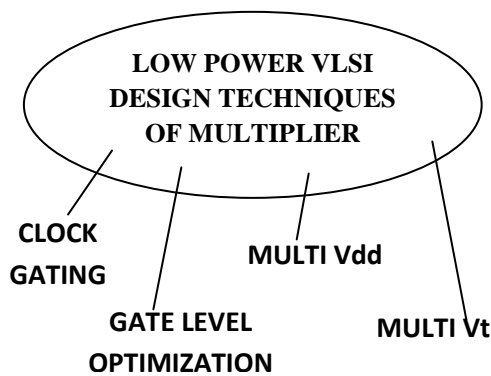

Fig. 2. Techniques of low power multipliers

Clock Gating: A substantial function of dynamic power in chip is in the circulation system of clock. The most well-known approach to diminish this power is to turn OFF clock when not required. A computerized clock-gating is performed by distinguishing synchronous load-enabler register banks, and actualizing them by gating the clock with a functioning empower rather than distribution of the information when the empower is inactive.

Gate Level Optimization: Energy interruption item (control) can be enhanced by keeping away from wastage of wastage. This should be possible by staying away from number of node transition that are a bit much. By recording the node transition in a given circuit for a given information, one can control the power scattering by limiting node changes. This prompts a critical decrease in Without Clock-gating With Clock-gating.

Multi V_{dd}: Dynamic power P_{dyn} is proportional to and lowering supply voltage V_{dd} on selected blocks helps to reduce power significantly and also increases the delay of the gates.

Multi Vt: As geometries have contracted to 130 nm, 90 nm, 65 nm and beneath, utilizing Multi Vt has turned into a typical method for diminishing spillage current. Numerous libraries today offer a few adaptation of their cells, for example, Low Vt, Standard Vt and High Vt. The usage apparatuses can exploit these libraries to enhance timing and power at the same time. It is presently basic to utilize "Double Vt" combination. The objective of this approach is to limit the aggregate no., of fast, defective low Vt transistors by sending them to meet planning whenever required. The plan should meet with least usefulness, before enhancing power, i.e., incorporating the structure with superior, high spillage library firstly, and afterward unwinding back any of the cells on any basic swapping way for their lower execution, bring down spillage reciprocals.

V. IMPLEMENTATION OF LOW POWER VLSI MULTIPLIER

Multiplier logic modelled using Verilog HDL and substantiated using Model Sim. The performances of various multipliers, is explored by FPGA implementation and ASIC implementation.

BCSD (Binary Canonic Sign Digit) multiplier is a sequential multiplier involving shifting register for each clock cycle and accumulating partial products. It is totally characterized by the characteristics of clock and a load signal is taken to load registers with inputs synchronized with clock. Since the multiplier designed is of 12 bits wide it takes 12 no., of 24 hour cycles to reproduce the same outcome This multiplier is synchronized with clock i.e. is any changes in input signal will be recognized only at the rising edge of clock.

Array multiplier is a combinational circuit; no storage elements synchronized with clk. Delay in the output is caused by the change in the input that depends on the propagation delay of circuit elements used in the hardware implementations by the designer. Carry propagation is the critical factor and use carry save adder chain for improving the speed. Modified booth is a sequential multiplier which is synchronized with clock for each and every operation. In general, Booth multiplier will take 'n' clock cycles depending on the word length of operand and Modified booth of radix-4 takes n/2 clock cycles to complete one operation. Further, it can be reduced by increasing radix with a penalty in complexity of hardware.

Wallace tree multiplier is the fastest multiplier with irregular structure, pure combinational circuit with carry save adder chain and more complex hardware loop structure. First add all the available product terms and then the partial products in a tree structure without affected by delays in carry propagation. Baugh Woolley multiplier is a modified version of array multiplier, is combinational multiplier to handle the signed numbers multiplication. The speed of sequential multipliers can be increased by encoding them with high radix, with a penalty of increase in complexity. All simulated programs cannot be synthesized and restricts the designer in making effective hardware description. Further simulation tools verify the functionality of logic only. All these existed multipliers produce less efficiency.

The vedic multiplier is a specimen of interest because of its integrated design where even the smaller blocks can be employed to generate a design for the bigger ones. Booth's Multiplier surveys adjacent pairs of bits of the 'N'-bit multiplier Y including an implicit bit below the least significant bit as in figure (3) showing the architecture of proposed low power VLSI multiplier.

Compared to above multipliers, this multiplier produces better results. Let us discuss about this multiplier in detail manner. The main parts of this multiplier are CSAT, MBE, PPRG. Let us discuss the entire operation in detail manner.
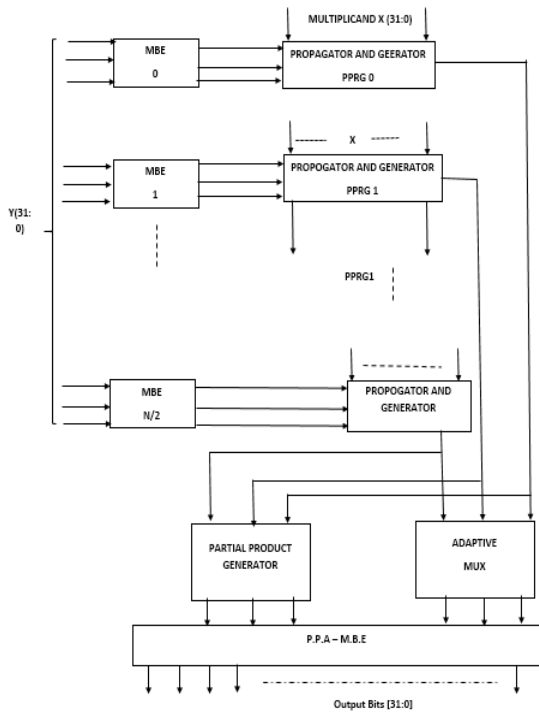

Fig. 3: Block diagram implementation of low power VLSI multiplier

The new architecture proposed consists of Partial Product Generation (PPG) logic, 2's complement logic and a carry save adder tree. Firstly some partial product arrays are produced by using multiplication algorithm. But the partial product rows are small in size and fast in speed. MBE technique will reduce the partial products. Now the multiplier Y is divided into group of 3 bits. The each bit will be reduced from n to n/2. Here the carry save adder tree will perform the reduction technique. Compared to existed system, the proposed system produces effective results as show in above architecture operation.

VI.   RESULTS

From below figure (4), it can observe the RTL Schematic of proposed multiplier. Basically, RTL schematic is a traditional design abstraction which a synchronises signals (data) between hardware registries, and the logical operations.
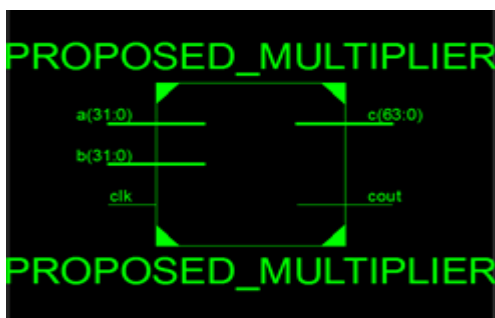

Fig. 4: RTL Schematic

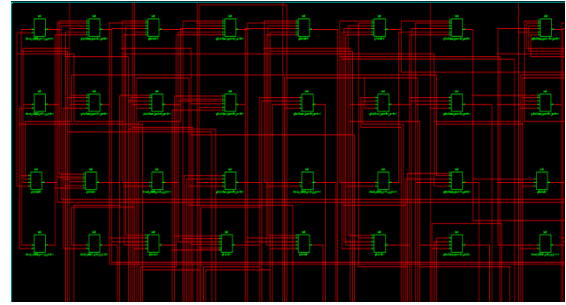From below figure (5) we can observe the Technology schematic view of proposed multiplier.

Fig.5: Technology schematic

Table. 1: Report of proposed multiplier

Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2017	46560	4%
Number of fully used LUT-FF pairs	0	2017	0%
Number of bonded IOBs	129	240	53%

Table. 2: Comparison of multipliers in terms of power, logic delay and route delay.

NAME OF MULTIPLIER	AREA	LOGIC DELAY	ROUTE DELAY
PROPOSED MULTIPLIER	60.3%	7.9%	92.1%
VEDIC MULTIPLIER	52.4%	18.4%	113.7%
BOOTH MULTIPLIER	47.2%	22.9%	142.6%

The table (1) represents the simulation report of proposed multiplier. From above table (2) we can observe the comparison of multipliers. As the proposed multiplier is 32 bit it occupies less area and high speed operation as shown in table (2). However 60% of area is consumed, delay is reduced up to 7.9% and route delay is reduced up to 92%. So compared to all multiplier, proposed multiplier produces effective results as shown in below figure(6).
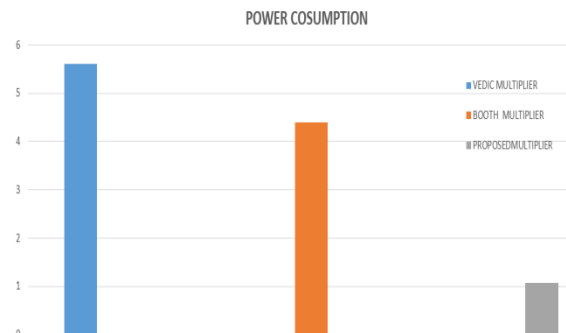

Fig. 6: comparison of power consumption

VII. CONCLUSION

Low power VLSI multiplier algorithm which is more beneficial in power has been presented provided, the sub modules can be made reusable for higher order bits and can also be employed implementation techniques for analysing the speed requirement in huge set of large bit multiplication processes. The Multiplier simply yields less power consumption. Various low power strategies for power reduction optimization techniques have been incorporated for the reduced power. The proposed low power VLSI multiplier architecture produces better efficiency. The optimal speed is acquired using implementing technique compared with the general multiplier procedures. From results it can conclude that proposed low power VLSI multiplier forms an important aspect in complex signal processing applications.

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