A New Multilevel Inverter Topology with Reduced Switch Count for Domestic Solar PV Units

Prem P, Bharanikumar R

Abstract: ***The introduction of state of the art solid state technologies has made the multilevel inverters attractive for stand alone or grid connected renewable energy resources. A multilevel inverter can provide an alternating voltage at its terminals from the available isolated dc sources is capacitors. Recent researches in multilevel inverters are focusing on reduction of required components and maximizing the levels of terminal voltage. This work proposes a sub multilevel inverter topology with least number of circuit components. The simulation has been done in MATLAB/Simulink software package and the results obtained from the proposed topology has been compared with the topologies given in recent works in the aspects like number of IGBTs, number of drivers and switching losses. The comparison shows that the proposed topology is more efficient.***

Keywords: Power Electronics, Multilevel, Inveter, Converter, Renewable Energy.

I. INTRODUCTION

Renewable energy is getting importance these days due to rise in energy demand all over the world and depletion of fossil fuels. Particularly wind and solar energy systems are much suitable to share 10% to 20% of the total load fed by conventional energy resources. However the terminal voltage of renewable sources is highly fluctuating. In order to get a regulated voltage from these resources solid state converters and intermediate storage elements are being used. Particularly multilevel inverters are gaining much attention in the field solar photovoltaic power generation due to their ability to provide near sinusoidal voltage at its terminals by utilizing multiple dc sources.

A multilevel converter will convert the DC voltage from available single/multiple sources in to AC voltage of desired magnitude. The magnitude of the AC voltage at the converter's terminal will be dependent on the number of sources/capacitors available in the input side. The alternating voltage obtained at the terminal will be a stepped sinusoidal wave and the number of steps in the wave is in proportion to the number of sources/capacitors utilized. This makes the multilevel converters realizable for MV and HV applications with standard LV matured technology switches. In addition to that with higher number of levels, it is possible to obtain a nearly perfect sine wave with higher amplitude of fundamental components at the terminal with reduced output voltage THD, dv/dt stress and the electromagnetic interference . Several topologies have been proposed earlier and in recent research, all these topologies can be categorized under one of these three conventional topologies i.e., 1) Cascaded H-Bridge converter (CHB), 2) Neutral Point Clamped (NPC) converter and 3) Flying Capacitor (FC) based converters.

The unequal voltage sharing due to load power factor and requirement of large volume of clamping diodes increases the cost and complexity of control circuitry in NPC converters, thus reducing their reliability [1][2]. Even though the extension of number of levels more than three is relatively easier in FC converters, requirement of large capacitor banks, pre-charging circuitry and the possibility of uneven voltage distribution makes these converters less attractive [3] [4]. The CHB converter topology with its capability of modularization and simple expansion has less number of components when compared to NPC and FC converters. However, the rise in number of voltage levels drastically increases the requirement of number of isolated dc sources and switches in this topology.The recent research is focused on reducing the cost and improving the reliability of the CHB converter topologies by reducing the number of switches and number of gate driver circuits for the given number of sources. A generalized topology has been presented in [5] which can be used in both symmetrical and unsymmetrical mode. But the number of switching components required is very high when compared to its ability to generate number of levels and the required number of dc voltage sources n. A new topology has been presented in [6] and it is capable of handling even number of voltage sources. In this topology there is a possibility for the switches to get short circuited if turned on simultaneously due to firing circuit issues. A sub-cell based symmetric and asymmetric voltage source multilevel inverters are presented in [7]. The number of switches in each cell is 4 and when the number of such subcells increases the switch count will increase to higher values. There are several other works [8-14] presented different topologies based on modular multilevel inverter, sub module based multilevel inverters etc. But in all the cases the number of switches and the number of driver circuits required are high. This results in increased switching and conduction losses.The successive content of this paper is arranged as given: The structure of the proposed sub module for multi level inverter is discussed in section 2, simulation results of the converter have been discussed in section 3, comparison charts depicting the

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superiority of the given module when compared to other topologies are given in section 4 and the conclusion is given in section 5.

II. PROPOSED TOPOLOGY

The basic unit of the proposed ladder type sub multilevel inverter is depicted in Fig 1. This topology comprises of an H bridge and a ladder based level adder. The switches used in the ladder i.e., S1, S2, …..Sn are IGBT switches with snubber resistance and the switches employed in the H-Bridge i.e., B1, B2, B3, B4 are comprised of an IGBT and an anti-parallel diode. Any number isolated dc sources can be added to this sub module. The rating of the switches has to be chosen according to the number of isolated switches used. If the number of voltage sources used is taken as n, then number of switches required can be expressed as given in (1)

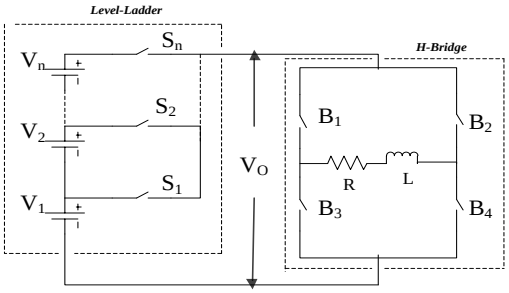

Fig.1. Structure of the basic topology

$$N_{switch} = n + 4 \qquad (1)$$

The switches can be controlled using various available PWM scheme through a suitable driver circuit. The number of such required driver circuit for the proposed topology can be generally expressed as given in equation (2)

$$N_{driver} = N_{switch} \qquad (2)$$

The number of diodes in the circuit will be equal to 4 for any number of levels and the maximum voltage at the terminals of the H bridge can be using equation (3)

$$V_{Omax} = nv_{dc} \quad (3)$$

The switches in the converter have to be chosen according to the necessary blocking voltage across the corresponding switching terminal and the current through it. The blocking voltage across each switch in the converter and the maximum blocking voltage in the converter circuit are depicted in equations . The blocking voltage of the switches in level ladder i.e., S_1,S_2,S_3 ..... S_n can be given as

$$V_{block} = v_{s1} = v_{s2} = v_{s3} = V_{dc} \qquad (4)$$

The blocking voltage of the switches in the H-bridge B1, B2, B3¬ and B4 will be

$$V_{block} = v_{B1} = v_{B2} = v_{B3} = v_{B4} = nv_{dc} \qquad (5)$$

The maximum blocking voltage in the converter circuit can be expressed as

$$V_{blockmax} = nv_{dc} + 4 \times nv_{dc} \quad (6)$$

Table 1 Switching States for 2n+1 levels

State	Switching States										Voltage
	Switches in level ladder						H-Bridge Switches				V_0
	1	2	3	4	-	N	1	2	3	4	
0	1	0	0	0	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1	0	0	1	V_1
2	0	0	1	0	0	0	1	0	0	1	V_1+ V_2
3	0	0	0	1	0	0	1	0	0	1	V_1+ V_2+ V_3
⋮	⋮										⋮ ⋮
n	0	0	0	0	0	1	1	0	0	1	$\sum_1^n V_i$
n+1	1	0	0	0	0	0	0	1	1	0	-(V_1)
n+2	0	1	0	0	0	0	0	1	1	0	-(V_1+ V_2)
⋮ ⋮											⋮ ⋮ ⋮
2n	0	0	0	0	0	1	0	1	1	0	$-\sum_1^n V_i$

III. PWM SCHEME

There are numerous PWM schemes available for multilevel inverters. In this work a level shifted carrier PWM scheme has been used. In this scheme a common sine reference with frequency 50 HZ and a dedicated carrier for each level with frequency 1 kHZ has been used. The number of carriers compared with the generator will be based on the number of levels to be generated in the terminal. During every conduction period one switch from the level ladder and two switches of the H bridge will be turned on. The reference sine wave and the six carriers are shown in the Fig.2 for a seven level prototype inverter to be discussed in the next section

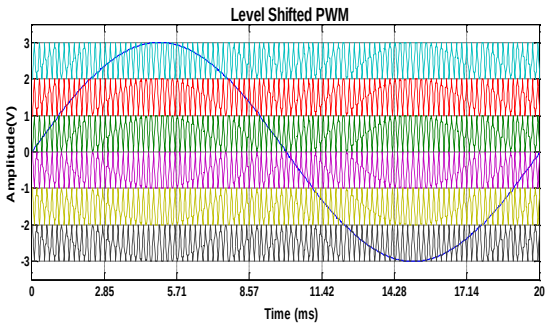

Fig.2. Level Shifted PWM scheme for proposed topology

IV. PROTOTYPE SEVEN LEVEL INVERTER

A seven level inverter has been developed based on the above discussed level ladder based multilevel inverter module. A seven level inverter requires six carrier waves to generate +vdc, +2Vdc and +3Vdc and the corresponding values. The zero state can be simulated by comparing the level 1 Carrier with reference and complementing the resultant pulse. The reference sine wave with 50 Hz frequency and the carriers with a frequency of 1 kHz, the generated multilevel pulse pattern are portrayed in Fig.2 and Fig.3 respectively.

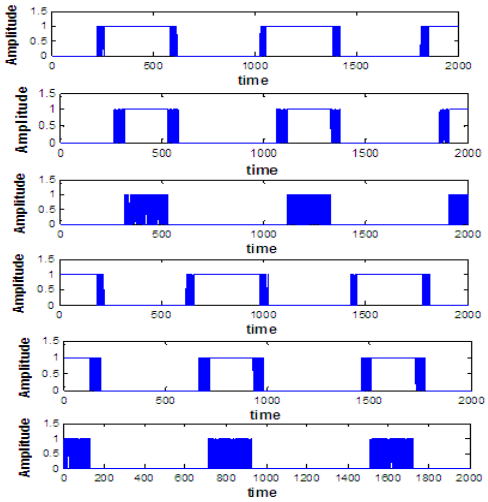

Fig.3 Multilevel pulse pattern for 7 level invereter

The voltage obtained before the H-bridge is unipolar. The positive and negative cycle at the terminals of the inverter are obtained by switching on the switches B_1, B_4 and B_2, B_3 of the H-bridge respectively. The levels $+V_{dc}/2V_{dc}/3V_{dc}$ can be obtained by switching $S_1/S_2/S_3$, B_1 and B_4 as shown in Fig. 4(a), 4(b) and 4(c)

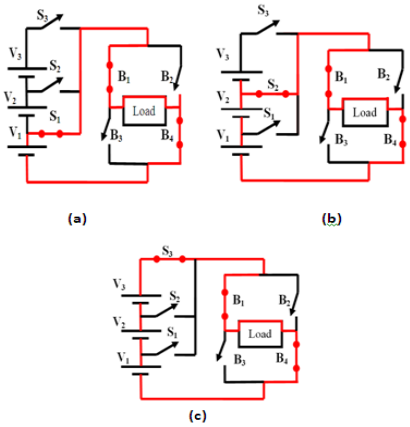

Fig.4 Switching circuit for positive half cycle of the inverter

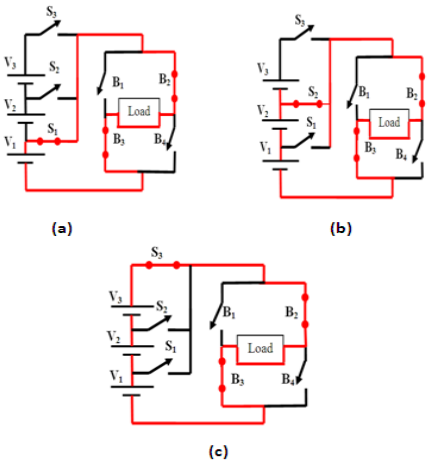

Fig.5 Switching circuit for negative half cycle of the inverter

The levels $-V_{dc}/-2V_{dc}/-3V_{dc}$ can be obtained by switching $S_1/S_2/S_3$, B_2 and B_4 as shown in figure 5(a), 5(b) and 5(c)

V. Simulation and Results

The Matlab/Simulink software package is used to simulate the sub module. The number of isolated dc voltage sources has been considered as three. Therefore the number of output volte levels will be seven (2n+1). The magnitude of the voltage from each isolated dc voltage source is considered as 30 V. The on state resistance of IGBT is considered as 0.01 ohm. The snubber -resistance of the IGBTs used in level ladder is considered as 1e5 ohms. The simulation circuit is shown in the Fig.6

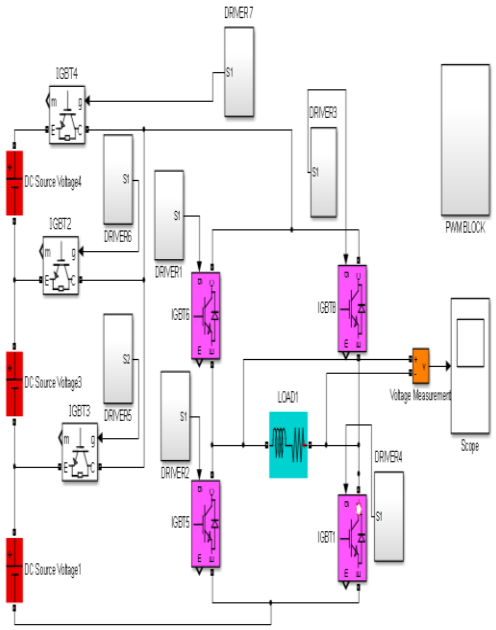

Fig.6 Simulation circuit of the inverter in Simulink environment

Table 2 Comparison of proposed topology with other topologies

Parameter	Reference 5	Reference.6	Reference.7	Conventional CHB	Proposed
Number of IGBTs	$[2(n+1)]+4$	$4n+2$	$\frac{4n+10}{3}$	$4n$	$n+4$
Gate Divers	$n+6$	$4n+2$	$\frac{4n+10}{3}$	$4n$	$n+4$
Number of diodes	$[2(n+1)]+4$	$4n+2$	$\frac{4n+10}{3}$	$4n$	4
Maximum Blocking voltage	$[2(n+1)]+4nv_{dc}$	$4\times[(3\times5^{n-1}+1)^n-1]V_{dc}$	$(6n-4)v_{dc}$	$n\times16nv_{dc}$	$nv_{dc}+4nv_{dc}$

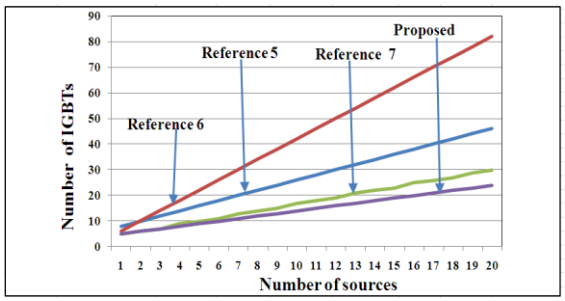

Fig.7. Number of Sources Vs Number of IGBTs

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The Fig.7 portrays the relationship between the number of sources and number of IGBTs for the considered references and the proposed topology. It can be understood that the number of switches required in the proposed topology increases linearly with the increase in number of voltage sources. However the rate of increase is very much less when compared to the considered references.

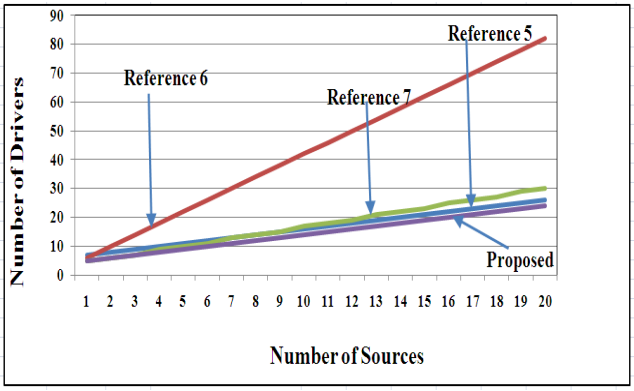

Fig.8. Number of drivers Vs Number of levels

The Fig.8 depicts the increase in required driver circuits with respect to increased voltage sources. The number of driver circuits required for the proposed topology is less when compared with its referred counterparts. This makes the circuit compact and improves the reliability.

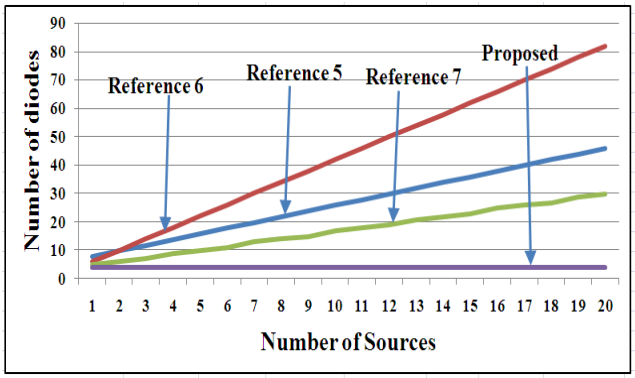

Fig.9. Number of drivers Vs Number of levels

The controllability of any power electronic circuit will be tedious when the number of uncontrolled devices like diodes employed in the circuit is high. The Fig.9 shows the number of diodes required for different voltage levels. From the figure it can be observed that the number of diodes needed for the proposed topology is only four for any level. Whereas this number increases with increase in levels in the topologies taken for reference.

VI. EXPERIMENTAL VERIFICATION

To validate the simulation results an experimental set up has been done with three voltage sources with 30V each and the load value is given as R = 100Ω. The nearest level modulation technique has been embedded in to a FPGA Spartan XE3S250E controller whose gate driver circuit comprises of a Schmitt trigger, opto-coupler and a buffer. The terminal voltage and load current obtained experimentally are shown in the figure.

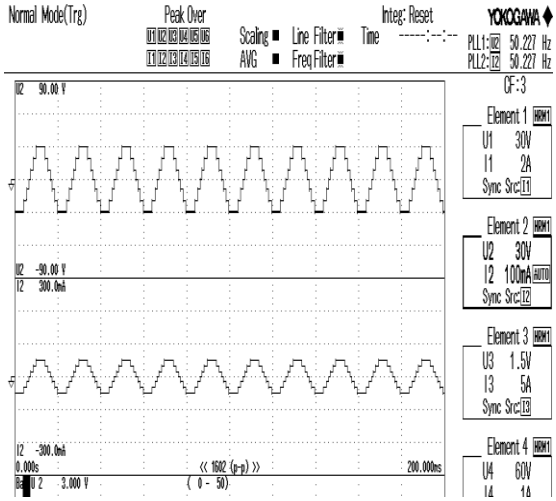

Fig.10. Experimental Terminal voltage and current waveforms

The number of components required for fabricating a seven level inverter with the proposed topology and the topologies used in other references are shown in Table 3

Table 3 Component chart

Topology	Number of IGBTs	Gate Divers	Number of diodes
Reference 5	12	9	12
Reference 6	14	14	14
Reference 7	7	7	7
Proposed topology	7	7	4

VII. Conclusion

A novel sub-multilevel module has been proposed in this work. The number of circuit component required for the presented topology is relatively less when compared with the topologies suggested in references [5] [6] [7]. The switching scheme for the inverter has been explained and the performance of the topology has been verified using Matlab/Simulink software package. Even though the output THD of the proposed inverter is a bit high, it can be reduced by using a filter circuit in the load side. The filter circuit will not increase the size of the converter much. Since, the number of components in the proposed circuit is very less the reliability of the circuit will be high.

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