

Design and Analysis of Memristor Memory Cell Using Different Windowing Functions

K. Paramasivam , R. Sathiya Priya, V. Saminathan

Abstract: In recent years, rapid growth of battery operated devices has made the low power memory design a desire in the industry. As the number of transistor increases, the leakage current has made the SRAM unit a power hungry block from both the static and dynamic perspectives. Nowadays, the SRAM block is an important part in SOC design. For memory design, the power dissipation and area are the main factors. Alternative technologies are needed to meet recent challenges in memory design. Memory cell can be designed by using memristor whose memristance M is function of charge q in it. Memristor is passive non-linear device that controls the current and able to retain the charge in it. Hence, memristor is considered as resistor with non-linear characteristics and memorizing feature. In this project Memristor and its performance is analysed by using two different window functions in MATLAB. Hysteresis curve is obtained for analysis. Memristor based memory cell is designed using memristor with proposed window function to analyse the performance using LT in 180nm technology. Peak and average power results are compared. It shows that 94% of power is reduced in the proposed memory cell.

Keywords: SRAM, Memristor, Hysteresis, window function, non volatile memory.

I. INTRODUCTION

A device which is utilized to store digital information is called memory. Main function of memory is to store and retrieve the information. Each cell is activated with set condition to store 1 and reset condition to store 0. Semiconductor memory can be randomly accessed at faster rate than other memory devices. Read and Write operations are key process in memory to fetch the stored bit and to store the bit in required location. Different memory cells are available in the literature and are characterized by number of transistors. Out of which 6T SRAM cell [1, 2, 3] is very popular and considered in this research work to model memristor based memory cell.

II. MEMRISTOR

Memristor was first described by Leon Chu[4] and has been developed in HP Laboratories with experts led by StanleyWilliams. Memristor is a memory resistor available in the form of passive circuit element. Resistance of the memristor is changed by varying the charge in the circuit. Direction of current decides the resistance which raises in one direction while falls in opposite direction. However,

resistance cannot go below zero. When the current is stopped then the resistance remains in the previous value that has flowed in it. Thus memristor “remembers” the current in it. So it can hold data similar to conventional RAM but without having any additional energy to retain the data. Thus non-volatile characteristic exhibited in the memristor makes the development of non-volatile memristor memory.



Figure 1: Memristor symbol

A memristor is defined as one non-volatile two terminal device in which the magnetic flux between the terminals is a function of the quantity[4] and has been designated M by the charge Q and it is given by $M(q) = d\phi/m$. Symbol of memristor is shown in figure 1. Relation between memristance and charge is given by Strukov et al [5] Figure 2 depicts the model developed by HP with TiO_2 and TiO_{2-x} material which is sandwiched between two platinum wires. Memristor in forward and reverse biasing offers two resistance states as R_{ON} and R_{OFF} respectively.

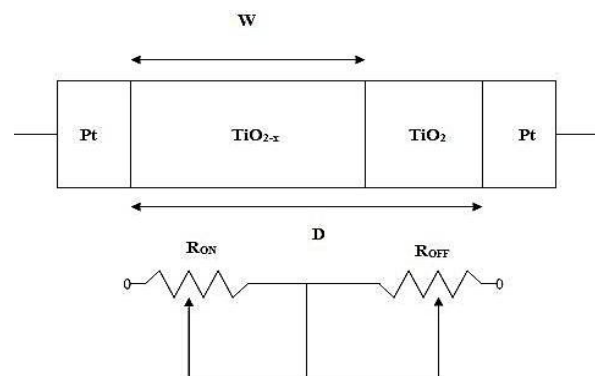


Figure 2: Physical Memristor model

A. Window functions

The velocity of electron movement in the edges of doped and undoped materials is to be maintained at zero. The condition is called as nonlinear dopant drift and it can be achieved by characteristic function called window function $f(x)$.

Revised Manuscript Received on December 08, 2018.

Dr. K. Paramasivam, Professor, Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, Coimbatore, Tamilnadu, India.

R. Sathiya Priya, PG Scholar, Department of Electronics and Communication Engineering, Kumaraguru College of Technology, Coimbatore, Tamilnadu, India.

V. Saminathan, Assistant Professor, Department of Electronics and Communication Engineering, Maharaja Engineering College, Avinashi, Tamilnadu, India.

The different kinds of window functions are:

1. Strukov window function
2. Benderli window function
3. Joglekar window function
4. Biolek window function
5. Prodromakis window function

Joglekar et al. proposed novel window function [7] gives zero drift at the edges but it has terminal state problem. Hence the memristor may not work properly at the edges. Biolek et al. proposed another window function [8] in which parameter current I is introduced to minimize the terminal state problem. Discontinuity in window function is its disadvantage. Strukov et al. offered the window function [5] and it can be altered in the form of $f(x) = x-x^2$, by Benderli and Wey [9] to develop a spice macro model of TiO₂ memristor. Prodromakis et al introduced the scalable window function [10] with parameter j which solves the problem of restriction on maximum value of unity. A window function [11] proposed by Sangho Shin et al. with non-zero value (\ddot{a}) even at boundaries can be used to eliminate the backing problem but it causes the excess accumulation charge at memristor. Further developments in memristor also shown in [12, 13] which uses modified window function to characterize the device. Memory cells[14, 15] also developed based on the memristor with modified window functions.

III. IMPLEMENTATION RESULTS

A. Memristor without window function

The tool used in this project is LT spice. Figure 3 shows the schematic representation of memristor (U1) model with sinusoidal input voltage of 1V and the frequency is 1Hz. Current and voltage relations are given in hysteresis curve shown in figure 4.

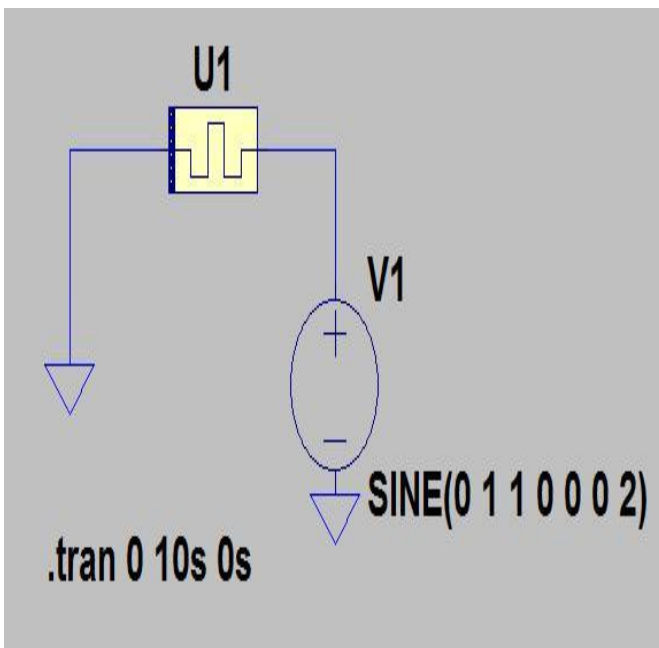


Figure 3: Schematic Model Of Memristor With Sinusoidal Input Voltage.

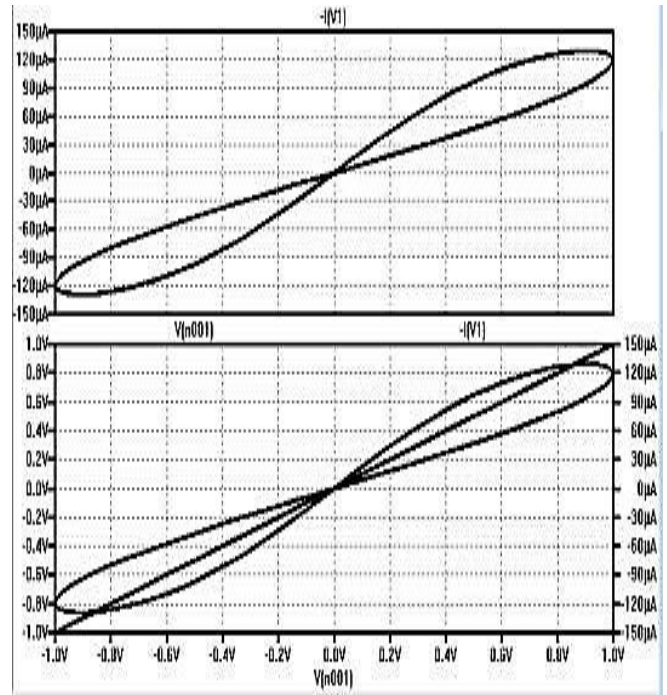


Figure 4: Hysteresis curve of the memristor without window function.

B. Memristor model using Joglekar window function

The Joglekar window function and its MATLAB simulation result are given in Figure 5 where state variable and control parameter are given as x and p respectively. Figure 5 shows MATLAB simulation for Joglekar window function which has high value at the center and reaches to zero at edges. As p has higher value function looks like a rectangular window and minimizes non-linear drift conditions.

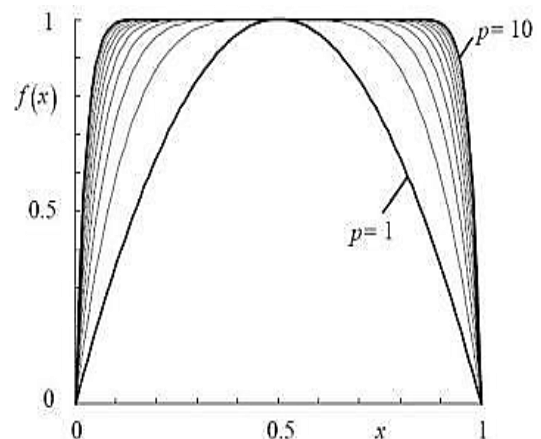


Figure 5: MATLAB Simulation Output For Joglekar Window Function.

The Joglekar window function based memristor is given in Figure 6 and its sub circuit file is added in it. The hysteresis curve for memristor model using Joglekar window function is given in Figure 7.

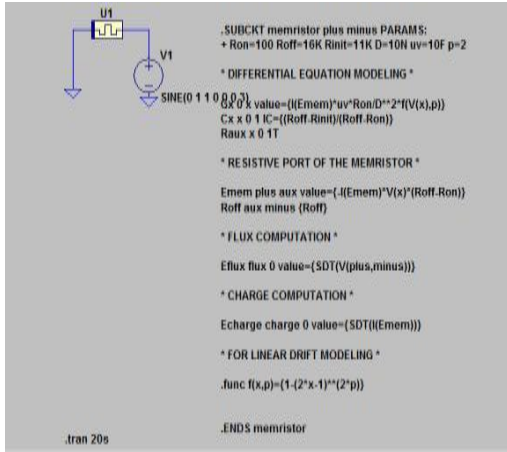


Figure 6: Schematic Model For Joglekar Window Function Based Memristor.

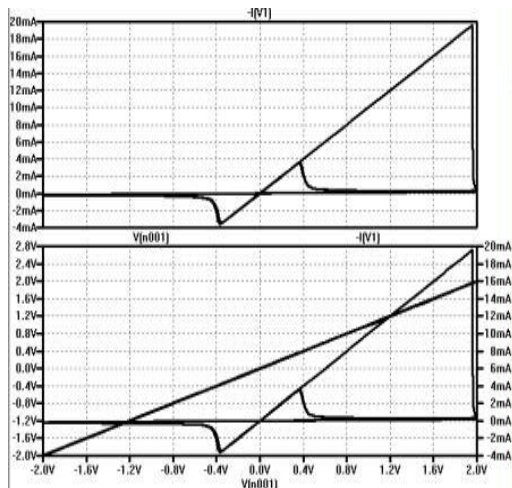


Figure 7: Hysteresis Curve For Joglekar Window Function Based Memristor.

In this the sine voltage is of 2V and frequency is about 1Hz. If the frequency is increased to 2Hz the corresponding hysteresis curve will be shrunk which is shown in Figure 8.

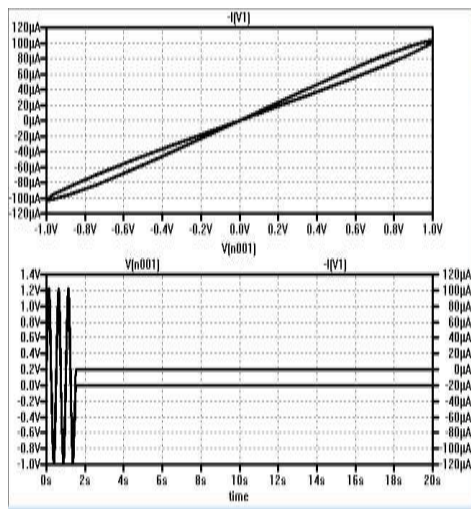


Figure 8: Schematic Model Of Joglekar Window Function Based Memristor For Increased Frequency.

C. Memristor model using Prodromakis window function

The Prodromakis window function which is given and its MATLAB simulation result is shown in Figure 9 where the control parameter gives maximum value of the function whose value is above or below 1.

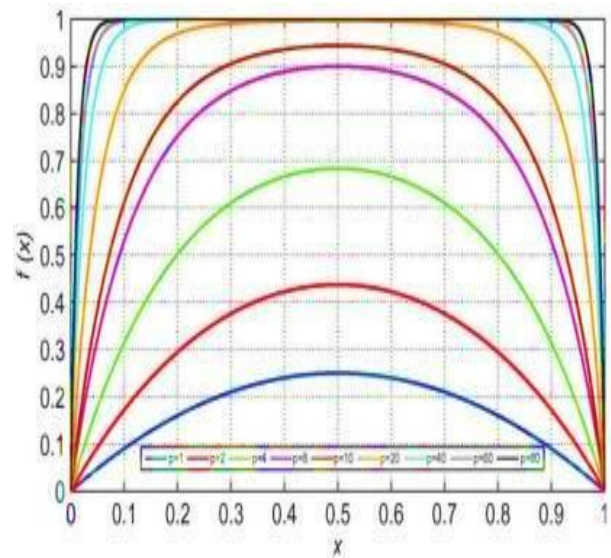


Figure 9: MATLAB Simulation Output For Prodromakis Window Function.

The Prodromakis window function based memristor model with amplitude of 2V and frequency of 2Hz which is shown in Figure 11.

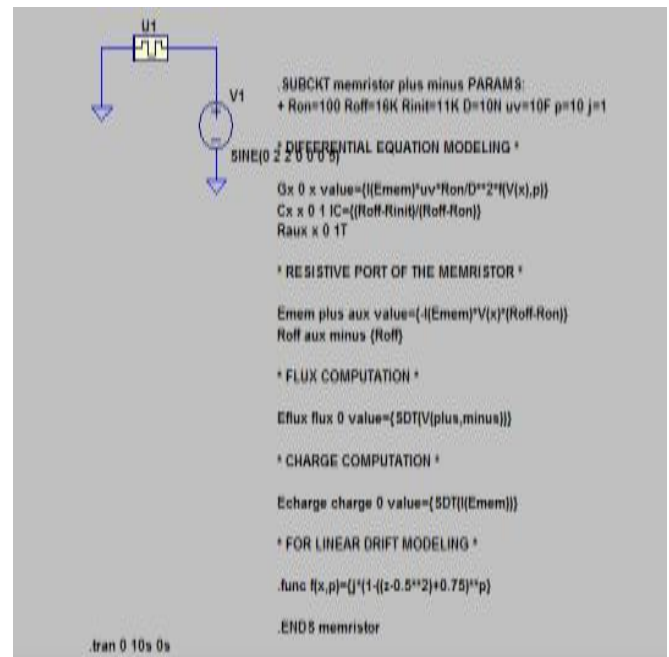


Figure 10: Schematic Model For Prodromakis Window Function Based Memristor.

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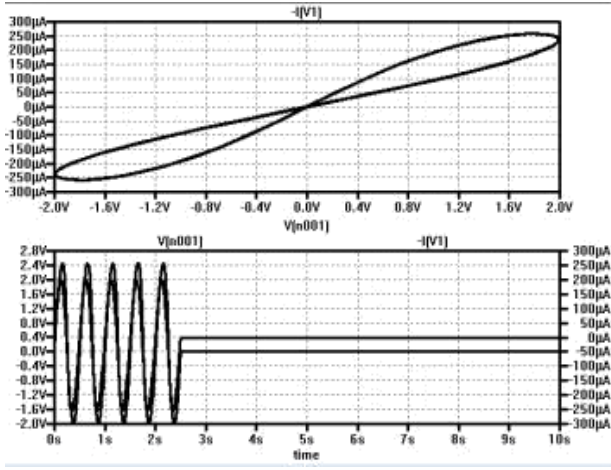


Figure 11: Hysteresis Curve For Prodromakis Window Function Based Memristor Model.

D. Memristor based 6T SRAM Memory cell

The Memristor based 6T SRAM memory cell is designed and simulated in LT spice and it is shown in Figure 12. The technology used in this is 180nm technology.

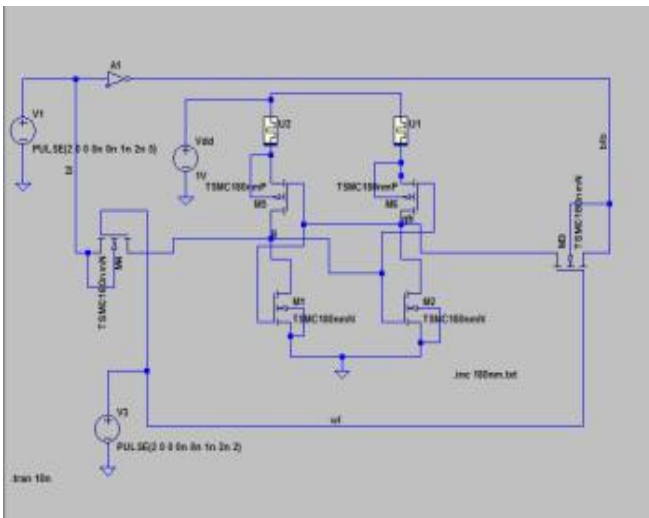


Figure 12: Memristor Based 6T SRAM Memory Cell.

The output waveform for Memristor based 6T SRAM memory cell is given in Figure 13.

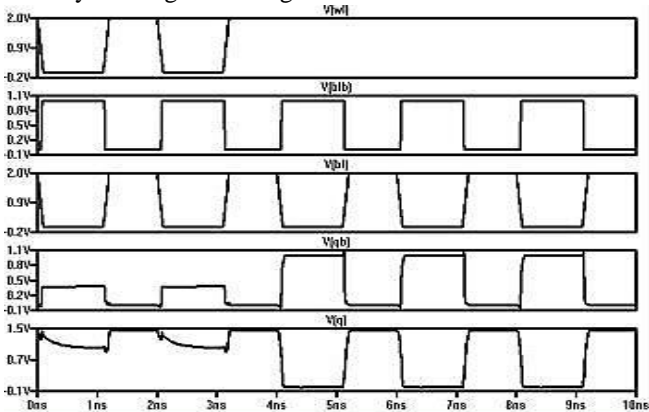


Figure 13: Output Waveform For Memristor Based 6T SRAM Memory Cell.

E. Conventional 6T SRAM Memory cell

The conventional 6T SRAM memory cell is simulated in LT spice and power analysis is calculated as shown in figure 14.

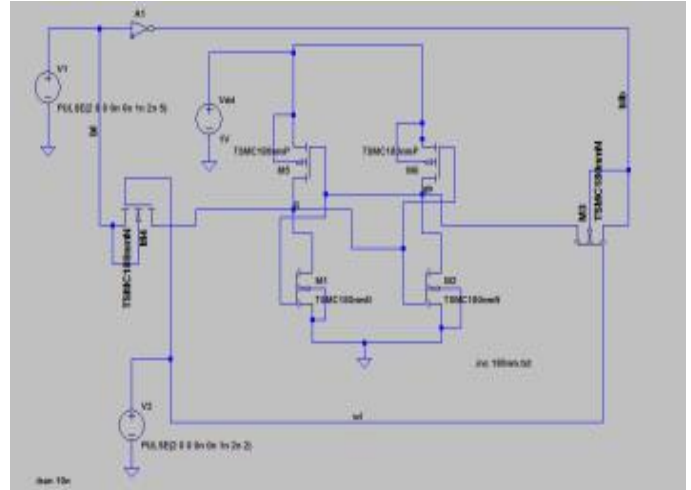


Figure 14: Conventional 6T SRAM Memory cell.

F. Power Calculation

| circuit Node | Peak Power (Watts) | Average Power (Watts) |
|-----------------|--------------------|-----------------------|
| At Memristor U1 | 24.496u | 398.78n |
| At Memristor U2 | 30.636u | 6.648 u |
| At M5 | 176.7u | 1.0371u |
| At M6 | 185.25u | 133.12n |
| At VDD | 53.846u | 16.84 u |

Table 1: Peak Power And Average Power For Joglekar And Prodromakis Window Function Based Memristor Memory Cell.

| Circuit Node | Peak Power (Watts) | Average Power (Watts) |
|--------------|--------------------|-----------------------|
| At VDD | 837.2u | 86.539u |
| At M5 | 199.5u | 33.538u |
| At M6 | 196.2u | 45.76u |

Table 2: Peak And Average Power For Conventional 6 T SRAM Memory Cell.

| Circuit Node | Peak Power In -al 6T SRAM (Watts) | Peak Power In -r Based Memory Cell (Watts) | % In reduction |
|--------------|------------------------------------|--|----------------|
| At VDD | 837.7u | 53.846u | 93.572 |
| At M5 | 199.5u | 176.7u | 11.428 |
| At M6 | 196.2u | 185.25u | 5.581 |

Table 3: Comparison Of Peak Power In Conventional 6T SRAM And Memristor Based Memory Cell.

From Table 3 it clearly shows that the peak power in memristor based 6T SRAM memory cell is reduced compared to that of the conventional 6T SRAM memory cell. Thus power consumption is reduced by using memristor.

IV. CONCLUSION

An analysis of various window functions for the linear ion drift model of memristor is carried out. Relation between voltage and current at edges of memristor is addresses by different window functions. The Joglekar and Prodromakis window function based Memristor is simulated and its I-V characteristics is analysed using LT spice tool. Memristor based 6T memory cell at 180nm technology is designed and power is calculated. Thus memory cell using memristor is designed and simulated for its operation. For both the Joglekar and Prodromakis window function, total and average power results are same and the power is not influenced by window function. By comparing the memristor based memory cell with that of the conventional memory cell the consumption of peak power is reduced.

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