Design and Analysis of Memristor Based Memory Cell

K. Paramasivam, R. Sathiya Priya, V. Saminathan

Abstract: ***In recent years, the progression of battery functioned devices has made the low power memory design an urge in the industry. As transistor count increases, the leakage current has made the SRAM unit a power hungry block from both the static and dynamic perspectives. Also the SRAM block is an important part in SOC design nowadays. Here the power dissipation and area are the main factors in designing the memory. SRAM's are also volatile in nature; they lose what was stored in them if the power is turned off. Memristor is a new circuit device and it can be used forconstructing memory cell. It can be seen that memristance M depends on charge q, which is defined as the time integral of the memristor current. This paper is based on memory cell using memristor. It has the property of non volatileness. It raises the packing density and minmize the power in system on chip (SOC). This concept can help to reducing the leakage power in the memoery element without loss of stored data. SRAM takes large part of power & area, therefore memristor based SRAM is designed to improve power & speed of memory cell. The memristor based memory cell is designed using LT spice EDA tool in 180nm technology. Conventional 6T SRAM cell is modified with memristor and CMOS - Memristor based memory cell is designed and simulated in LT spice for its performance in 180nm technology. Peak and average power are obtained for conventional 6T SRAM cell and proposed memristor memory cell. Power results are compared and shows that power reduction is achieved in memristor based memory cell when compared with conventional 6T SRAM cell. Read and write operation is simulated to evaluate the read time and write time of proposed memory cell.***

Keywords: Memristor, Hysteresis, Non – volatile.

I. INTRODUCTION

Semiconductor based electronics is the base of the information technology society. Semiconductor memories and microprocessors are two important fields, which are benefited by the enlargement in semiconductor technology. The technological enhancement has improved its performance as well as packing density of these devices over the years.In 1965 Gordon Moore observed an exponential growth in the number of transistors per integrated circuit in which nearly doubled every two years. SRAM is a binary Randim access memory that can be used to store binary digit. It diverges from Dynamic RAM which uses capacitor for memorizing data and also requests refreshment process [1]. Power consumption is a main problem in portable consumer device due to restricted battery life and expensive package and also requires heat sink for compensate excessive energy dissipation. Due to the demand of raising capacity, the SRAM designers are encouraged to increase the packaging density [2].

II. MEMRISTOR MODEL

Memristor is a memory resistor theoreticaly described by Chua and practically has been establishedby S.Williams at HP Lab [3]. Memristor is a passive circuit element which produces charge by the time integrals of current and flux by time integral of voltage.The change in resistance depends on the charge that passed through the element.The memresistance is high due to the current flow in forward direction and opposite in negative direction. When the applied signal is stopped, it holds the change in resistance when the current that last flowed through it.

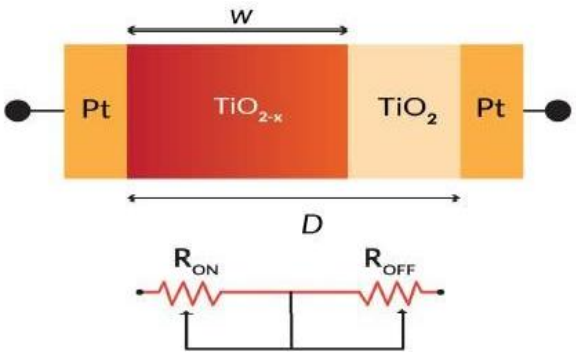

Figure 1: HP LabMemristor model

As practical model of memristoris proposed by Strukov et al. and gives a relationship between the memristance and electric current which is passed through the memristor [4]. The realistic HP Lab model of memristor is depicted in Figure 2 and it is composed of a titanium oxide and oxygen deficient titanium layer which is joined between two platinum layers. RON (high resistance) and ROFF (low resistance) state can be obtained by the application current either in forward or reverse direction.

If the input signal is applied in positive configuration, the margin of the doped region moves right to the memristorensuing in lower resistance as oxygen vacancies drift from the doped (TiO2-x) to the undoped (TiO2) region as depicted in figure 1. Higher resistance state (ROFF state) can be attained by applying opposite signal polarity.

Revised Manuscript Received on December 08, 2018.

Dr. K. Paramasivam Professor Department of Electronics and Communication Engineering, Kumaraguru Collegeof Technology, Coimbatore, Tamilnadu, India.

R. Sathiya Priya PG Student Department of Electronics and Communication Engineering, Kumaraguru Collegeof Technology, Coimbatore, Tamilnadu, India.

V. Saminathan Assistant Professor Department of Electronics and Communication Engineering, Maharaja Engineering College, Avinashi, Tamilnadu, India.

III. LITERATURE SURVEY

After the development of memristor model[5] by HewletPackyard (hp), manymemristorbuilt memory elements are available in the literature. Research paper [6] has emphasized on power dissipation variations in 6T, 9T and ST10T SRAM cells. Here the effect of power dissipations is perceived on various temperatures at different voltages. It is observed that the power dissipation varies from 0.007mw to 0.019mw for 270 C to 1270 C respectively and it is less compared to 6T, 9T and ST10T SRAM Cells. In [7], a simple circuit model of the memristor in nonlinear doponant drift has been designed and implemented using LT spice software. In this model, current drawn by the memristor is obtained for sinusoidal input voltage with the amplitude and frequency of of 1volts 3Hz, 2volts 3Hz and 3volts 3Hz and the corresponding current values are 100µA 200µA and 400µA respectively.

In [8], authors described a memristor model with new window function obtained from sigmoidal function that prevents the boundary problem and the proposed window function have afitting parameter to model the more type of memristors. In [9], proposed a design of NVSRAM memory cell bybthe combination memristor and CMOS device. Read and write time is suggestively minimized. The write time is higher than the conventional memory cell and Read time is minimized.

In [10], authorspresented a memristor model with novel flexible window function obtained from sigmoid logistic and Richards equation to solve the boundary issue problem.Different behavior of characteristics is observed by varying scaling parameters.

Memory cell is base unit for memory and hence to design nonvolatile memory by incorporate memristor with conventional CMOS 6T RAM cell to propose new type of NVRAM memory cell in this research paper.

IV. SIMULATION RESULTS

A. Conventional 1 bit memory cell

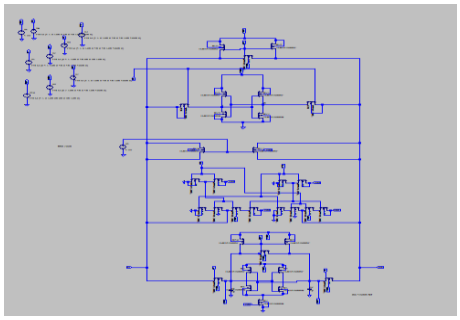

Figure 2: Schematic of conventional 1 bit memory cell

Figure 2 shows the schematic of conventional 1 bit memory cell. The technology used in this is 180nm technology. This schematic design includes conventional 6T SRAM memory, precharge circuit, write driver circuit and sense amplifier. It's read and write operation is shown in Figure 3 and Figure 4. bl, blb, di, we, re, q, qb, out and out1 in the Figure 3 and Figure 4 represents bit line, bit line bar, data input, write enable, read enable, storage nodes q , qb and sense amplifier outputs out , out1. The power supply is given as 2.5V.

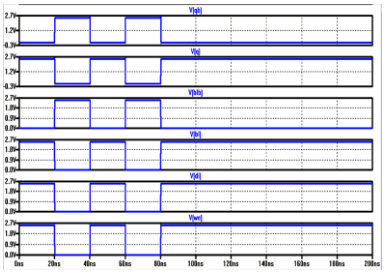

Figure 3: Output Waveform Of Conventional 1 Bit Memory Cell During Write Operation

From Figure 3 it shows that the write access time for logic 1 is 0.1275ns and for logic 0 is 0.1136ns. Read access time to achieve logic 1 is 5.95ns and to achieve logic 0 is 3.07ns.

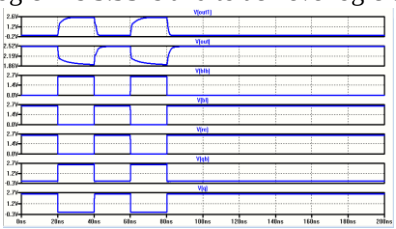

Figure 4: Output Waveform Of Conventional 1 Bit Memory Cell During Read Operation

B. Memristor based 1 bit memory cell

The diagram of Memristor based 1 bit memory cell is given in Figure 5. From the schematic U1 and U2 represents the memristor.

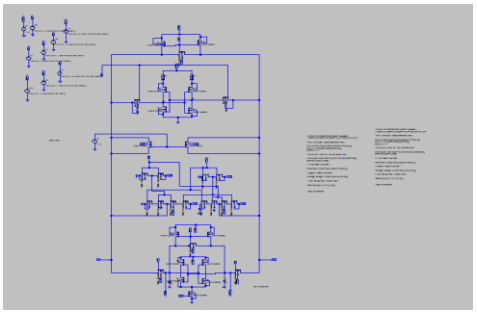

Figure 5: Schematic of Memristor based 1 bit memory cell

Figure 6 and figure 7 represents the output waveform of hybrid memory cell during write and read operation. For writing logic 1 it takes about 0.629ns and for logic 0 it is 0.1029ns. For reading logic 1 it takes 7.51ns and for logic 0 it is 2.8103ns.

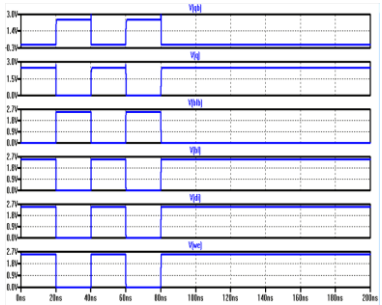

Figure 6: Output waveform of Memristor based 1 bit memory cell during write operation

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

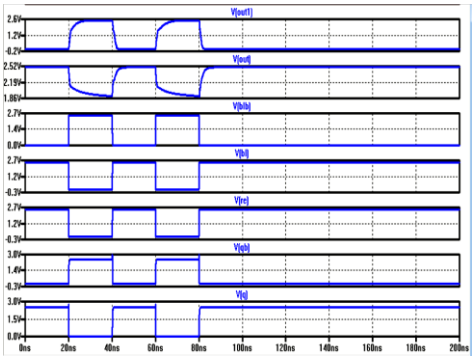

Figure 7: Output Waveform Of Memristor Based 1 Bit Memory Cell During Read Operation

C. Power Analysis

At Circuit node	Peak Power (Watts)	Average Power (Watts)
VDD	-180µ	-2.260 m
PMOS 24	1.096m	91.225n
PMOS 23	690µ	100.41n

Table 1: Peak And Average Power For Conventional 1 Bit Memory Cell

At Circuit node	Peak Power (Watts)	Average Power (Watts)
VDD	-344.04µ	-2.26 m
PMOS 24	742.48 µ	34.916n
PMOS 23	408.6µ	27.183n

Table 2: Peak And Average Power For Memristor Based 1 Bit Memory Cell

At Circuit node	Peak Power in Conventional 1 bit memory cell (Watts)	Peak Power in Memristor based 1 bit memory cell (Watts)	Power reduction (%)
VDD	-180 µ	-344.04µ	47.68
PMOS 24	1.096m	742.48 µ	32.25
PMOS 23	690 µ	408.6µ	40.78

Table 3: Comparison Of Peak Power Between Conventional 1 Bit Memory Cell And Memristor Based 1 Bit Memory Cell

The Average power in VDD is approximately same for both Memristor based memory cell and Conventional memory cell. Peak power for Memristor based memory cell is minimized as given in Table 3. It shows that peak power of Memristor based memory cell is minimized up to 48% when compared with Conventional memory cell.

V. CONCLUSION AND FUTURE WORK

Memristor based memory cell at 180 nm technology is designed in LT spice tool and power is calculated. Read and write operation is performed. Comparison of power results between conventional one bit memory cell and memristor based one bit memory cell presents that power minimization in memristor memory cell is 48%. The work can be extended to design simple memory unit using the proposed memory cell. Also the hardware model of memristor based memory cell can be realized once the hardware model of memristor is manufactured by industry and compared with simulation results.

REFERENCES

1. Nirali K. Khokhara and Bharat H. Nagpapa, 'Comparative Analysis of one bit SRAM using different SRAM cells in 45nm CMOS Technology', Int.J.of Innovative Research in Computer and Communication Engineering, Vol. 5, Issue 1, January 2017.
2. K,Navdeep, K,Loveleen,k,Gurpreet, 'Comparative Study Of 64 Bit SRAM Memory Using 6T and 7T SRAM Cells', ISSN: 2394-0697, Volume.2, 2015.
3. Chua L.O, "Memristor – the missing circuit element', IEEE Transaction on Circuit Theory, volume.18, no. 5, pp.507-519, Sep. 1971.
4. M,N,Sakib, RHS,Biswas, 'Performance Analysis of a Memristor-based Hybrid Memory Cell with Rapid Bidirectional Storage Capability',International Conference on Electrical Engineering and Information Communication Technology 2016.
5. Strukov,D.B, Snider G,S, D. Stewart, D,R, and Williams,R,S, 2008, "The missing memristor found", Nature, volume. 453, pp. 80–83.
6. Saminathan,V,Paramasivam,K,'Analysis of the Effect of Temperature and Power Dissipation Variations in SRAM Cells, Int. J. of Sci. Research, Vol.2, pp: 164-166, Dec2013.
7. V.Saminathan, Dr.K.Paramasivam,2015, "A New Forth Element Memristor Model with new windowing functions using LTspice Programs", Int. J. of Applied Engg.Research, ISSN 0973-4562 Vol. 10 (2015) pp: 29026- 29031.
8. Saminathan ,V , Paramasivam,K,2016, "Missing Fourth Element Memristor Modeling with New Window Function Derived from Sigmoid Logistic Equation" International Journal of Advanced Engineering Technology E-ISSN 0976-3945 ,Vol. 7, pp.384-386.
9. Saminathan,V, Paramasivam,K,2016, 'Design and Analysis of Low Power Hybrid Memristor-CMOS Based Distinct Binary Logic Nonvolatile SRAM Cell', Circuits and Systems,Volume.7 No.3 , pp. 119-127.
10. Saminathan, Dr. K. Paramasivam,2016, 'A Novel Flexible Window Function for Modelling Nonlinearity of a Titanium Oxide Memristor for next generation emerging Nonvolatile Memory Applications', Asian Journal of Research in Social Sci. and Humanities Vol. 6, No. 8, pp. 338-349.
11. A,K, Nigam, S, Singh and A,Tiwari, 2015, '6T SRAM Cell: Design and Analysis', Int. Journal of Engg.Sci. and advance research.