Design of 15-Level inverter topology with reduced number of semiconductor switches for Stand-Alone Power Systems (SAPS)

Ramachandran, TamilarasuViswanathan, SuryaprakashShanmugasundaram

Abstract: ***Stand-Alone Power Systems (SAPS) help us to supply energy to remote or regional places where electrical infrastructure is not available. SAPS usually has a power generation sources like photovoltaic panels, micro-wind turbines, battery bank, inverter, battery charger and often a diesel generator for power back. Solar or wind has erratic outputs, so frequent changes in power cannot be tolerated by sensitive loads. Hence, Battery banks play a significant role by storing charges directly from renewable energy sources through charge controllers and then delivers inverter for residential uses. SAPS are deliberated to be expensive because of the cost associated with battery banks and renewable energy sources; concurrently reducing the cost and increasing the power quality of inverter is approachable. This paper proposes the importance of multilevel inverter (MLI) by reducing the number of semiconductor switches which inevitably decreases the cost of MLI circuitry and diminishes the harmonics by increasing the level of output. The new topology of MLI inverter is designed and simulated using PSIM (9.0) tool.***

Keywords: ***SAPS, Multilevel inverter, Topology, Total Harmonic Distortion***

I. INTRODUCTION

ultilevel inverters are increasing viably for converting the most valuable renewable DC sources into a staircase waveform (AC). A Multilevel inverter key role is to give an AC waveform that should approach near to a sine wave. Conventional MLI gives two or three level output has more distortion, harmonics and hysteresis losses in case of motors.[1,2] Many basic MLI are incorporated to obtain a better output but economical consideration need to be focused more. More number of semiconductor switches incorporated in MLI is again a drawback as it increases switching losses, driver circuit and cost.

Research on MLI is in the area of reduction in number of switches, diodes, capacitor, DC sources and harmonics is a focus area as renewable energy is essential for our future. [1,2] Renewable energy resources are very economical form of energy so measures should be taken to make the resource economical and efficient, so a new proposed multilevel inverter is designed to give 15 level output with minimum number of semiconductor devices.

Nowadays addition of different sources can be effectively performed using asymmetric multilevel inverter topologies which help us in choosing rated input sources economically.[3,4] This is incorporated for stand-alone power system where micro wind generator and solar panel are major source of input energy.

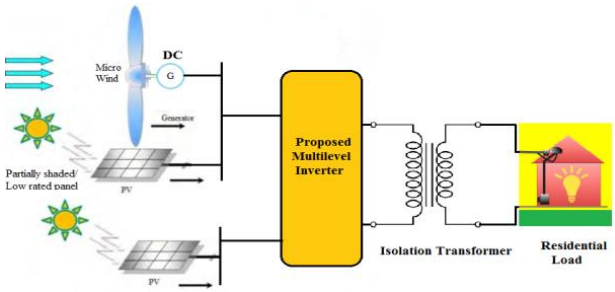

Fig.1.Schematic diagram of proposed multilevel inverter

II. INVERTER TOPOLOGY

The proposed multilevel inverter is designed for standalone power system where additions of DC sources are decided based on the rated voltage andprevious monitoring of energy sources. The general structure of proposed topology

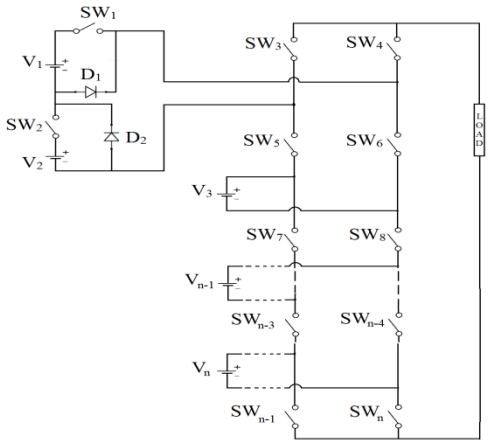

Fig.2.General structure of proposed topology

The proposed MLI has been compared with various other multilevel inverters to know the effective construction of the topology. The control and working of proposed multilevel inverter for 15-level inverter is simulated and results are obtained.

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III. CONFIGURATION OF PROPOSED 15-LEVEL INVERTER

The proposed MLI has fifteen stages of operation for obtaining 15-level output.

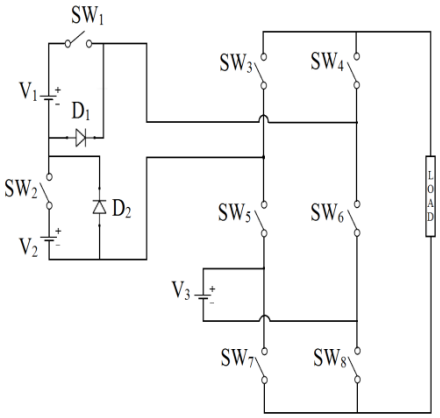

Fig.3.Proposed 15-level inverter

The topology depends on number of input sources being necessarily connected. Number of voltage sources decides the number of output levels, usage and rating of semiconductor devices in constructing a multilevel inverter.The switching ONstate duration of switches differs with respect to the output levels and stress onparticular switches can be identified based on the following table [4].

Switches	*T_{on}Period*
SW_1	11.2ms
SW_2	9.8ms
SW_3, SW_4, SW_5, SW_6, SW_7,SW_8	9.1ms
D_1,D_2	5.6ms

Table I Levels OfPeroids

$SW_{1\&2}$contributes more as it helps in adding with all other input sources.

The switching strategies for different frequency have been given below with respective voltage levels for one complete cycle.

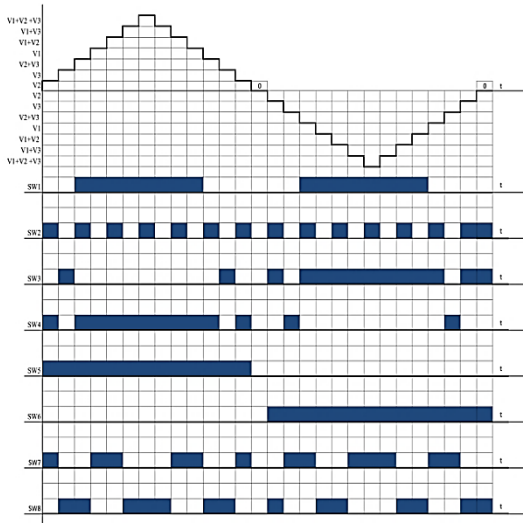

Fig.4 Switching Strategies

State	Switching States								Output Voltage
	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	
1	0	0	1	0	1	0	0	1	V_3
2	0	1	0	1	1	0	1	0	V_2
3	1	0	0	1	1	0	1	0	V_1
4	1	1	0	1	1	0	1	0	V_1+V_2
5	1	0	0	1	1	0	0	1	V_1+V_3
6	0	1	0	1	1	0	0	1	V_2+V_3
7	1	1	0	1	1	0	0	1	$V_1+V_2+V_3$
8	0	0	0	0	0	0	0	0	0
9	0	0	0	1	0	1	1	0	$-V_3$
10	0	1	1	0	0	1	0	1	$-V_2$
11	1	0	1	0	0	1	0	1	$-V_1$
12	1	1	1	0	0	1	0	1	$-(V_1+V_2)$
13	1	0	1	0	0	1	1	0	$-(V_1+V_3)$
14	0	1	1	0	0	1	1	0	$-(V_2+V_3)$
15	1	1	1	0	0	1	1	0	$-(V_1+V_2+V_3)$

Table II Switching State For 15 Level Inverter

IV. STATE OF OPERATION

The current path for different state of output voltages are mentioned

State 1: V_2

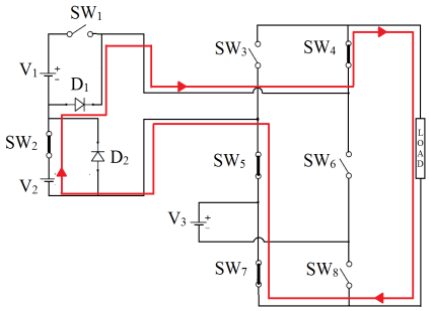

Fig.5.Current Path For Obtaining 1st step Output Voltage (Lowest Voltage)

State 2: V_3

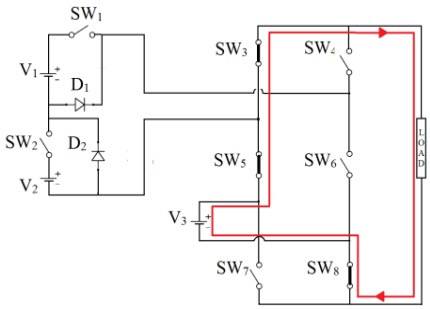

Fig.6.Current Path For Obtaining 2nd Step Output Voltage

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State 3: $V_2 + V_3$

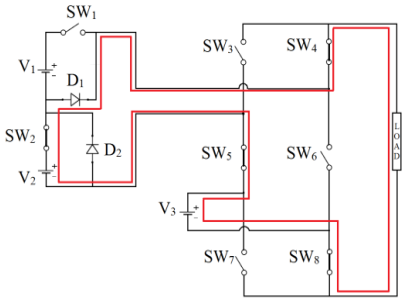


Fig.7.Currvolent Path For Obtaining 3rd Step Postive Output Tage

State 4: V_1

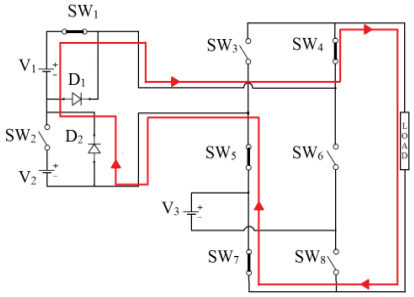


Fig.8.Current Path For Obtaining 4th Step Output Voltage
(Maximum Of Individual Input Sources)

State 5: $V_1 + V_2$

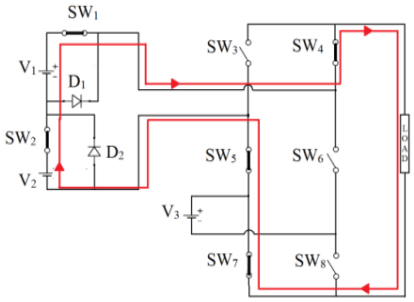


Fig.9.Current Path For Obtaining 5th Step Output Level

State 6: $V_1 + V_3$

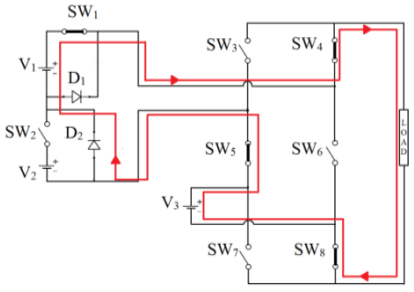


Fig.10.Current Path For Obtaining 2nd Step Output Voltage

State 7: $V_1 + V_2 + V_3$

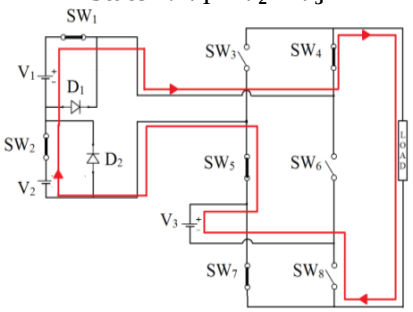


Fig.11.Current Path For Obtaining The Maximum Step Output Voltage

State 8: $-V_2$

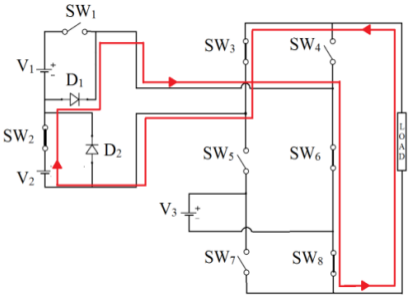


Fig.12.Current Path For Obtaining The Negative Least Step Output Voltage

State 9: $-V_3$

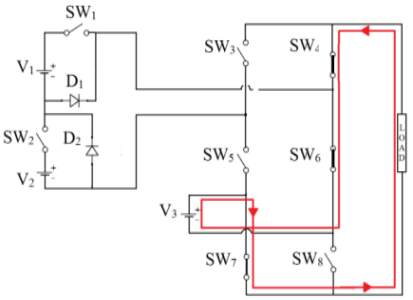


Fig.13.Current Path For Obtaining The Least Negative Voltage

State : $-(V_2+V_3)$

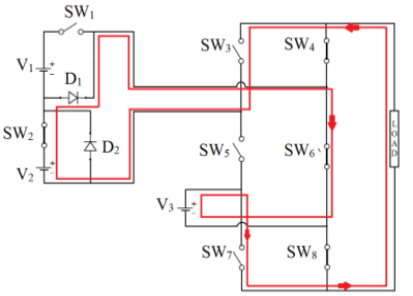


Fig.14.Current Path For Obtaining 3rd Step Negative Output Voltage

State: - V_1

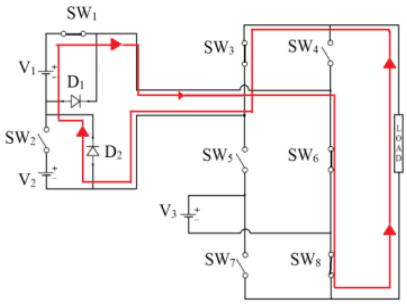


Fig.15.Current Path For Obtaining 4th Step Negative Output Voltage

State : -(V_1+V_2)

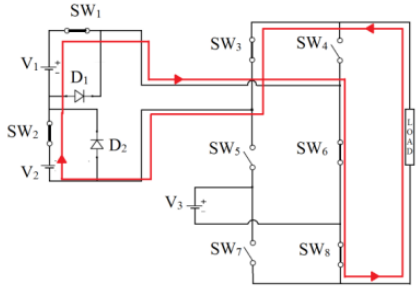


Fig.16.Current Path For Obtaining 5th Step Negative Output Voltage

State : -(V_1+ V_3)

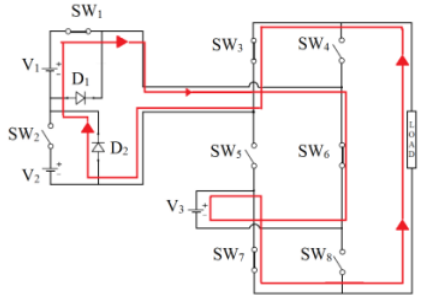


Fig.17.Current Path For Obtaining 6th Step Negative Output Voltage

State: - (V_1 + V_2 + V_3)

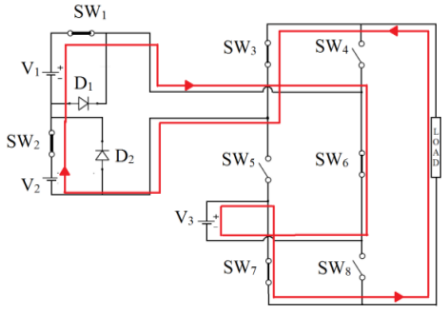


Fig.18.Current Path For Obtaining Step Negative Maximum Output Voltage

V. SIMULATION RESULTS

A. Standing Voltage

One of the significant parameter for operating MLI smoothly is the standing voltage[4]. The maximum blocking voltage of the switch is the standing voltage which decides the cost of MLI.

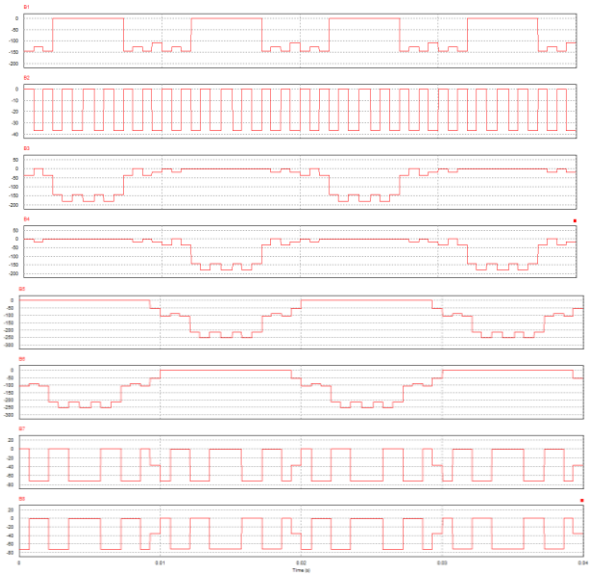


Fig.19. Blocking Voltage Of MOSFET Switches From SW_1 To SW_8

TABLE III

Switches	*Standing Voltages*
SW_1	150 Volts
SW_2	38 Volts
SW_3, SW_4	180Volts
SW_5, SW_6	260 Volts
SW_7, SW_8	70 Volts

B. Waveform

The proposed topology is constructed in PSIM tool and output voltage &current waveform are obtained. The simulation tool is implemented by keeping constant input energy sources are V_1=96 volt, V_2= 24 volt, V_3=48 volt, (in terms of ratio 4:1:2) as this paper concentrates more about topology of MLI.

C. Total Harmonic Distortion

The presence of harmonic distortion in output leads to increased cost of filtering components, accelerated ageing of equipment due to heating and other harmonic effects.[5,6] The proposed topology gives a THD for current waveform is 2.09% for R-Load.

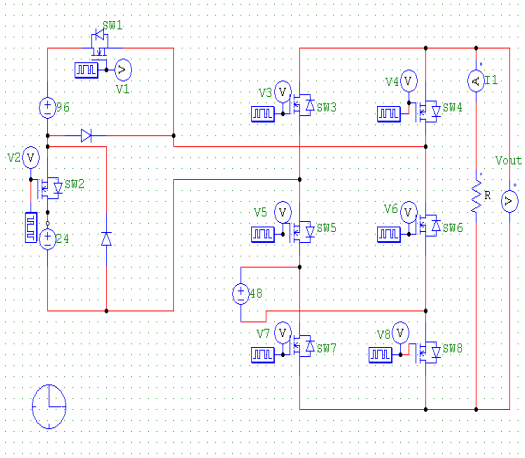


Fig.20. In Proposed Topology Of 15 Level Inverter PSIM Tool

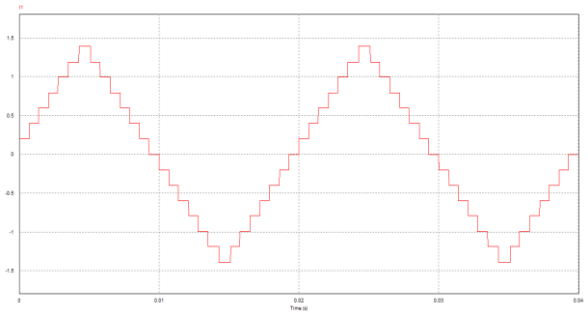
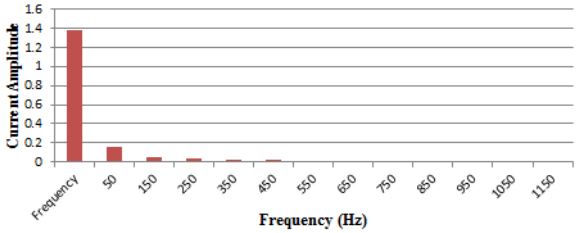


Fig.21. Current Waveform Of Proposed Topology For R-Load

Harmonic Order	Frequency	Current Amplitude	Square of current
1	50	1.385240159	
3	150	0.152901575	0.023378892
5	250	0.053911748	0.002906477
7	350	0.031021849	0.000962355
9	450	0.019175302	0.000367692
11	550	0.01990896	0.000396367
13	650	0.01298793	0.000168686
15	750	0.011271498	0.000127047
17	850	0.010821154	0.000117097
19	950	0.008895081	7.91225E-05
21	1050	0.009752793	9.5117E-05
23	1150	0.014936585	0.000223102
24	1250	0.013748234	0.000189014
			0.029010967
			0.020942915
		THD%	2.09429154

THD = 2.09 %



VI. COMPARISON

It is compared with conventional multilevel inverters which give good percentage reduction of switches. [8]

Components	NPC	FC	CHB	SMLI [7]	Proposed topology
DC Sources	1	1	7	4	3
Diodes	12	12	-	-	2
Capacitors	60	-	-	-	-
Switching Devices	24	24	28	13	8

VII. CONCLUSION

This paper proposes new topology which drastically reduces the use of power electronic components meanwhile reducing the cost of the inverter for SAPS. The proposed MLI has a scope to extend flexibility on design and to optimize the converter for change in input renewable sources.

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