Inverter Design using Junction less GAA Tunnel Field Effect Transistor

T.JasparVinithaSundari, K.Karthika

Abstract: ***The escalating pressure to defeat the drawbacks of conventional MOSFET such as physical limitations due to its short channel effects has inspired the production of a number of superior materials and device goemetries. In the midst of these novel devices are FinFET, Carbon Nanotube and Nanowires based FETs, having the attributes such as quasi 2-D and 1-D channel geometries for enhanced electrostatics. While a lot of of these modernizations aims only on building up high-performance devices, the making of a roadmap to forecast in-circuit performance combined with large scale integration for these technologies is highly desirable. In this paper we have incorporated Junction less gate all around TFET thus leading to ease of fabrication because of absence of doping concentration gradients for specific regions. In addition low power consumption is obtainable by TFETs as they are less prone to second order effects. The basic inverter circuit has been designed using the device and their performance is examined.***

Keywords: Tunnel diode, Field effect transistor,MOSFET, TFET

I. INTRODUCTION

In the earlier period, a major amount of study has been carried out to invent transistor topologies that can break MOSFETs below 10 nm. Amidst many proposals, TunnelFETs (TFETs) have shown to be a hopeful choice for digital circuits. [1] TFETs can have a subthreshold slope swing less than 60 mV/dec, facilitating a superior on to off current ratio. In addition to lower Subthreshold Slope, which offers good energy efficiency for the design of digital circuits, TFETs can also offer lower parasitic capacitances and an outstanding saturation behavior.[2] At low supply voltages, TFET-based digital circuits have a better energy efficiency in contrast to conventional CMOS designs. The asymmetric current flow of Tunnel Field Effect Transistors affects the digital circuits with pass-transistors . [7][10]

In order to overcome low on current problem with effective gate modulation for the improvement of tunneling probability, a modified better architecture in terms of p-n-p-n tunnel source with a highly doped n-type region between the source and channel resulting in an abrupt and highly doped tunnel junction.[8] The performances of circuits embedding TFETs have been reported with increasing popularity in both direct-current as well as radio-frequency applications. In many projects, a germanium gallium arsenide heterojunction Tunnel FET having a nanowire channel is used for analog circuit applications.[11][3] Even though good performance do not always offer a noteworthy advantage at the circuit level, any development in circuit performances are evaluated as development combined with proper designing of deviccomponents.Drivecurrent is highly enhanced by the narrow energy bandgap of Germanium and the ambipolar behavior is effectively suppressed by the wide energy bandgap of GaAs. On current of TFET is commonly determined by energy bandgap of source material and effective tunneling mass of the carriers.[4][5] The Band To Band tunneling in TFETs than the drift-diffusion transports in conventional MOSFETs offers steeper subthrehold slope.

Gate All around Tunnel FET Architectures have been revealed to have high drive current, low leakage current, near ideal Subthreshold behavior, and reduced temperature sensitivity due to the excellent gate electrostatic control over the narrow channel.[6] In this paper, the performance of Junctionless Gate all around TFETs have been analyzed by incorporating the device in the design of inverter. [13], [14]The robustness and the peculiar advantages of its suitability for circuit design based on its operational parameters is analyzed.

II. SIMULATION AND METHODOLOGY

In order to forecast effective performance of the circuits, we performed the mixed mode simulation of Inverter. We performed simulations using Sentaurus TCAD software tool. The various sections of the simulation, the files and the methods involved in it are briefed below. A brief overview on the method of simulation and the tool is explained.

A device simulation offers information about the inner limitations and the terminal characteristics of the device by which the device behaviour is predicted. The device to be simulated is taken as a meshed finite-element structure. Every node of the device has special characteristics such as material type and doping concentration. For all the nodes, the carrier concentration, current densities, electric field, generation and recombination rates, and many other parameters are found using simulation.

The purpose of Sentaurus Structure Editor is to build two dimensional and three dimensional device structures. Input file is basically a script file that holds commands describing the steps to be carried out as well as the physics section describing the specific material properties. It also contains the simulation timing details with respect to other parameters. Sentaurus Device simulates numerically the electrical behaviour of a device or circuit in separation or quite a few physical devices joint in a circuit.

Revised Manuscript Received on December 08, 2018.

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The grid of the the circuit simulated holds an account of a variety of regions such as the boundaries, material types, and any electrical contacts. Sentaurus Visual is referred to picturise the results produced by sentaurus simulation tools in all three dimensions.

The following steps are followed in simulation of the circuit.

- The modelled p-type and n-type device files are included within the DEVICE sections separately for n type and p-type devices with unique names. The "output " files are removed from the device sections.
- Both the n-type and p-type devices are declared within the DEVICE sections and a common output file is declared within a separate file section which is shared by both the p-type and n-type devices.
- The interconnections between the transistors are specified within the system section.
- Also they are specified within the instances of the devices declared. The voltage sources and any other electrical components are also declared within the system section.
- The voltage sweeps are given within solve section using quasi- stationary statements for all the specified voltage sources.
- Then the file is simulated using the sDevice command.
- The plot is specified within the system section and the output plot is viewed through sVisual.

III. DEVICE SIMULATION

Fig. 1(a) shows the cross sectional view of Junctionless GAA-TFET. The inmost arrangement is denoted as the Junctionless cylindrical core and the gate is structured all around the cylindrical core with respect to the gate coverage region. Tox and Tsi are referred as the thicknesses of the oxide region and the Junctionless cylindrical core. The total channel length is 20 nm. The effective oxide thickness is 2 nm and the gate material work function is of the range 4.7 – 5.91 eV. As it is anJunctionless architecture, the doping concentrations for source, drain and channel are similar and is of the range (Junctionless core) 1019 to 1021. The non localtunnelling process entails the band gap narrowing effects (BGN model) to be incorporated. The Shockley-Read-Hall recombination model, Fermi-Dirac ststistics are involved due to the heavy doping concentration.

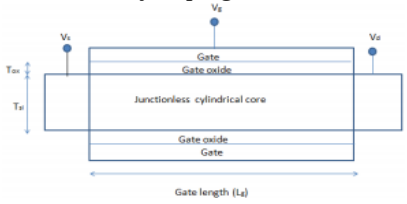

Figure 1 (a)Cross sectional view of Junctionless GAA TFET

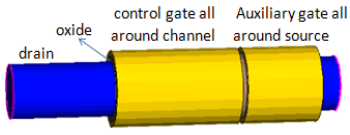

Figure 1 (b)3 Dimensional View Of The Device

The basic scheme installed here is to translate the Junctionless cylindrical core structure of JLFET into a (N+-I-P+) structure thereby facilitating quantum mechanical tunneling injection of carriers from source to channel

In order to predict dynamic performance of the circuit using , mixed mode circuit simulations of an inverter was done using Sentaurus TCAD software.

IV. RESULTS AND DISCUSSIONS

Figure 2 shows the schematic of CMOS inverter. Figure 3(a) & (b) shows the transient and switching characteristics of CMOS Inverter designed using Junctionless GAA TFET.

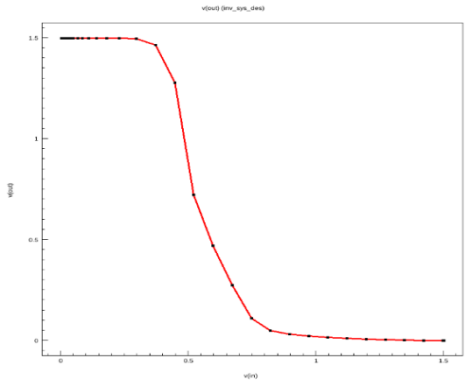

Figure 3 (a)Inverter switching characteristics

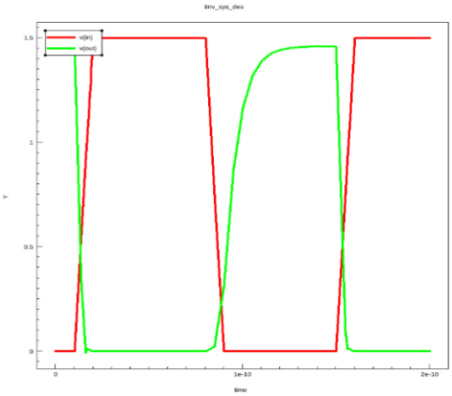

Figure 3 (b)Transient response of inverter

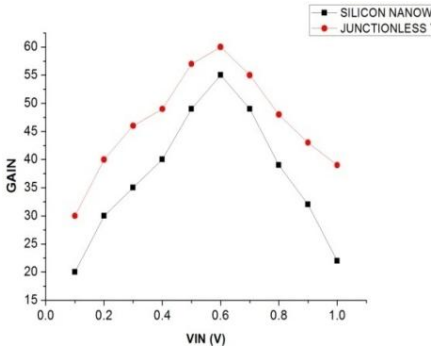

Figure 4(a)Gain Of Conventional Silicon Nanowire Compared With Junctionless TFET Nanowire

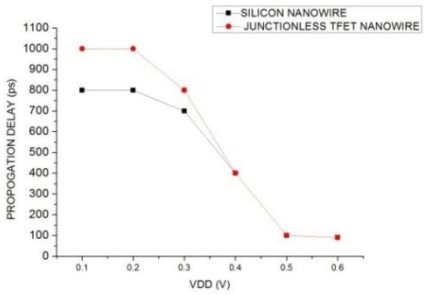

Figure 4(b)Propagation delay of Conventional Silicon

The voltage transfer characteristics (VTC) of the inverter using Junctionless GAA TFET are shown in Fig. 3(a) and (b). The corresponding inverter gains VOUT/VIN at various VDD were analyzed. A high gain of 60 is obtained at VDD =1 V. The inverter was designed using conventional MOSFET and Junctionless TFET Nanowire and to analyze the performance parameters, propagation delay and gain of the Junctionless TFET Nanowire is compared with Silicon Nanowire. Silicon Nanowire is designed and simulated for the same dimensional parameters in order to analyze appropriately. A better gain is achieved compared to conventional structure because of the topology of the Transistor and its transconductance.The combination of cylindrical structure and superior switching characteristics of TFET can achieve high level of electrostatic control of gate as all field lines originating from Drain can terminate at gate without the significant penetration into channel. This leads to steeper slope and diminished delay. The gate controllability and proper choice of hetero junction materials can further enhance the gain and delay characteristics.

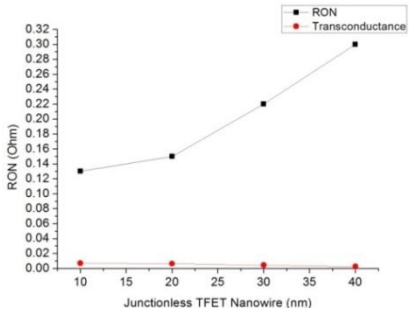

Figure 5(a)Variation Of Ron And Gm Based On Nanowire Diameter

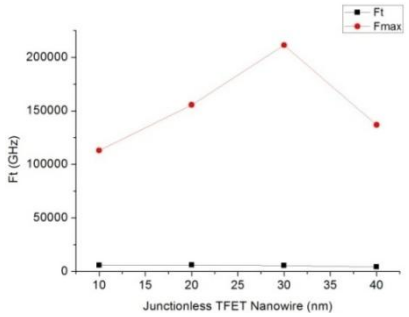

Figure 5(b)Variation Of Ft And Fmax Based On Nanowire Diameter

The on resistance and transconductance of the device varies based on the nanowire diameter which interprets that the choice of dimensional parameter influences the performance parameters necessary for circuit design like frequency, gain and delay. The device was analyzed for various diameters inorder to choose appropriate frequency, capacitance, cut off frequency, maximum frequency and so on. The variation of gm& Ron, Ft &Fmax based on nanowire diameter is shown in the figure 5(a) and 5(b). Based on various analysis of these type, the dimensional and operational parameters were chosen in such a way that it enhances the device's suitability for RF circuit design as well as digital circuit design.

V. CONCLUSION

In this paper, the inverter design using Junctionless TFET Nanowire, especially impact of operational as well as dimensional parameters on the Junctionless GAA TFET based inverter were studied. The performances of Junctionless Tunneling Nanowire based inverter have been analyzed for its delay and gain. It can be concluded that thinner channel contributes only for gain whereas a thinner channel and an optimized frequency and gm along with optimized Ron contributes for high gain sustaining a optimized delay compared to conventional silicon nanowires provided Junctionlessheterostructure is used. Also, the results are compared with conventional silicon nanowires.

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