Power Efficient Successive Approximation ADC With Double Tail Dynamic Latch Comparator

Nagarathinam S

Abstract: ***Analog to Digital converters (ADC) are used in medical instruments that serves as an essential part as the interface between analog and digital signal processing system. Low power design is needed for large battery life. Commonly used ADC is the successive Approximation Register (SAR) ADC. The other ADC models are Pipeline ADC, Flash ADC, integration ADC, Sigma Delta ADC. ADCs are chosen by considering resolution, power, size, frequency, performance and so on. A SAR ADC is selected for such applications because of its low power and tiny size. The essential engineering of SAR ADC comprise of sample and hold circuit, SAR, ADC and voltage comparator. This paper deals with double tail dynamic latch comparator which is replaced with thecomparator of SAR ADCs. The parameter estimations, like utilization of power, Signal to Noise ratio and resolution are carried out for SAR ADC. The schematic of SAR ADC has been designed using Tanner tool.***

Keywords-Analog to Digital converters, Sample and Hold circuit, Low power, Resolution, SAR ADC.

I. INTRODUCTION

Usually, low power consumption is needed for an extended battery time period. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) can be preferred for medium- to high-resolution operation. SAR ADCs can provide 5Msps sampling rates with resolutions from eight to eighteen bits.Mismatches in the internal components due to feature scaling, process variation and noise cause changes in the resolution of a comparator. So ADC Implementation requires full resolution quantization for all bits, that successively slows down the SAR loop and consumes additional power. the solution to the above problem is that replacement of typical comparator with the improved double tail dynamic latch comparator. Because it will make input-output isolation which reduces noise and latch delay time.

II. ADC ARCHITECTURES

ADC architecture has been selected by considering the parameters such as resolution, power, size, samplingfrequency, performance and etc. A Flash type ADC is the fastest amongst all other ADCs. A Sigma-Delta ADC is preferred for its high resolution. SAR ADC has been proposed due to its low power, tiny size and medium resolution.

A. Performance Metrics of ADCs

A. Spurious-Free Dynamic Range(SFDR)

SFDR is given mathematically in Equation, SFDR = 20 log10(Vsignal/(Vnoise+VHD)).

Vsignal represents the signal voltage,Vnoise represents the noise voltage and VHD represents the harmonic distortion voltage.

B. Signal to Noise Distortion Ratio (SINAD)

SINAD is a degree of the quality of a signal from a communications device, often defined as

$$SINAD = \frac{P_{Signal} + P_{noise} + P_{distortion}}{P_{Signal} + P_{distortion}}$$

wherePsignal, represents the signal power, Pnoise represents the noise power and Pdistortion represents distorted power.

C. Number of Bits (ENOB)

Effective number of bits (ENOB) is a measure of the dynamic range of an ADC.

$$ENOB = \frac{SINAD-1.76}{6.02}$$

III. SUCCESSIVE APPROXIMATION REGISTER ADC

In this paper, an improved double tail dynamic latch comparator has been proposed for 8 bit SAR ADC and is designed in 130nmin tanner tool with the power consumption of 326.9µW.The Schematic of SAR ADC is represented in Figure 1.

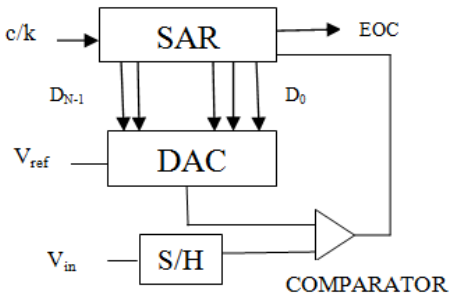

Figure 1. Basic Block of SAR ADC

A. R-2R LADDER DAC

This paper concentrates R/2R ladder networks which provide a simple means to convert digital information to an analog output.

Revised Manuscript Received on December 08, 2018.

Nagarathinam S,Asstprofessor,Electronics and Communication Engineering,Kumaraguru College of Technology, Coimbatore, TamilNadu,India

B. Successive Approximation Register

Figure 2 shows a simplified SAR logic proposed by Anderson. It is designed using a ring counter and shift registers.

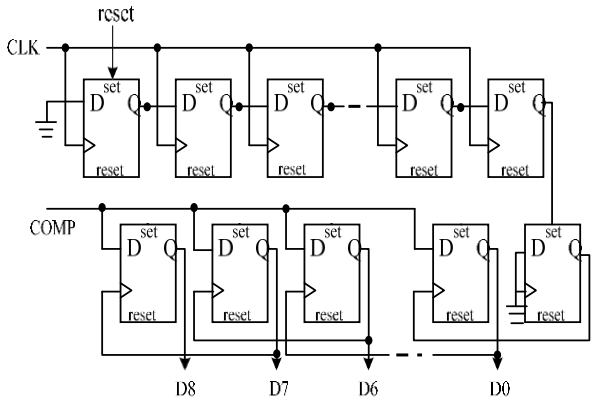

Figure2. Simplified SAR Logic

C. Sample And Hold Circuit

Sample and hold circuit is designed using a switch and a capacitor. If the sampling signal is low switch is connected and tracking will take place otherwise itholds the value.This operation provides a constant voltage at the input of the ADC during data conversion.

D. Comparator

Comparator is a fundamental component for ADC. So, the requirement of a good comparator is growing. Some comparators are clocked and only provide an output after the transition of the clock. Clocked comparators are also called dynamic Comparators. Clocked comparators plays a major role in designing faster ADCs.

E. Proposed Double Tail Dynamic Latch Comparator

The double-tail dynamic comparator is used in low voltage applications, the comparator is designed based on the double-tail structure. The main idea of the comparator is to increase ΔVfn/fpin order to increase speed.[3].

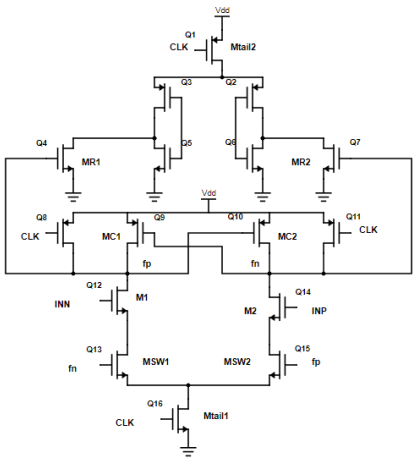

Figure 3. Proposed Double Tail Dynamic Latch Comparator

IV. IMPLEMENTATION OF SAR ADC

SAR ADCs are commonly used structure for designing applications with different ranges of resolution levels and alsofew mega samples per second (Msps) sampling rates. ADCs resolution level ranges betweeneightandsixteen bits, and these type of ADCs can be able to provideminimum power consumption and a lesser value of form factor. The voltage level of ADC is varying between negative reference value to the positive reference value, which allows the designer to use negative voltage levels.

The structures of SAR ADC with the predictable comparator,[10] and the proposed comparators are simulated using Tanner software tool and the performance metrics are compared.Schematic design of SAR ADC with the proposed comparator is shown in figure4

V. RESULTS

Schematic design of conventional comparator is shown in figure.4

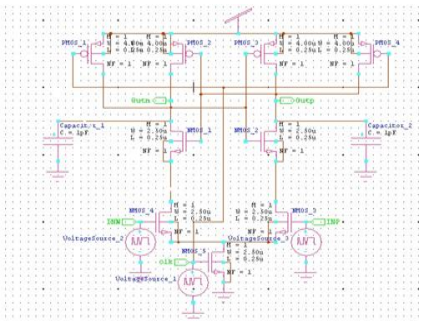

Figure 4. SAR ADC Designed With Proposed Comparator Structure

Figure 5. Conventional Dynamic Latch Comparator

Schematic design of proposed comparator is shown in figure 6.

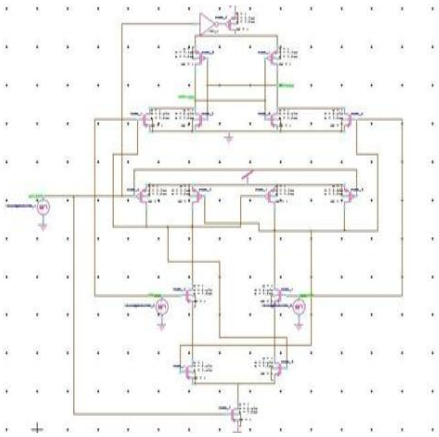

Figure 5 Proposed Double Tail Dynamic Latch Comparator

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

VI. PERFORMANCE METRICS OF TWO SAR ADCS

The various parameters which measure the performance of the ADC such as power consumption, Signal to noise distortion ratio, Spurious free dynamic Range, Effective number of bits are processed by the software and comparison is made as shown below in table 2.

Parameters	ADC with Conventional Comparator	ADC with Proposed Dual tail comparator
Power(μW)	370.86	326.9
SINAD(DB)	34.5698	32.0412
SFDR(DB)	65.3256	79.7216
ENOB(bits)	5.0456	5.0301

Table 2. Power And Noise Parameters Of SAR Adcs Designed With Conventional And Proposed Comparator

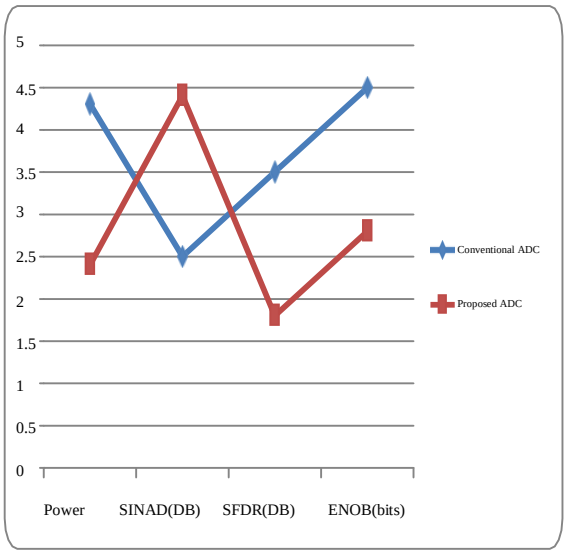

Figure 6 Comparison Plots Of Two ADC

VII. CONCLUSION AND FUTURE SCOPE

Today's portable and other electronic applications are using ADC for higher resolution and data rates with low power in scaled CMOS technology. The speed of the ADC is limited by the design of comparator.The SAR ADC is designed using double tail dynamic latch comparator. This comparator consumes less power consuming ADC.The low power consumption of SAR ADC which makes more efficient applications. This work explores design of SAR ADC with the proposed dual tail comparator that employs reduced latch delay time and offers low power consumption at small supply voltages. The current work presents implementation of 8-bit SAR ADC operating at 12.5MS/s and supply voltage of 1.2 V in 130nm CMOS technology. The ADC employs an R-2R DAC, a dual tail dynamic latch comparator and a SAR control logic containing a sequencer and a ring counter. The ADC exhibits good performance and achieves ENOB of 8 bit. The priority of the future improvement is to design a more efficient SAR ADC with a lower supply voltage.

REFERENCES

1. B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65,"IEEE Tran. Cir. Sys. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.
2. S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS, "Int. J. Analog Integ. Cir. Sig. Pro., vol. 66, no. 2, pp. 213–221, Feb. 2011.
3. Amin Nikoozadeh and Boris Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch", IEEE Tran. on Cir. And Sys. II: Express Briefs, Vol. 53, No. 12, December 2006.
4. SamanehBabayan-Mashhadi and Reza Lotfi," Analysis and Design of a Low-Voltage Low- Power Double-Tail Comparator", IEEE Tran. On VLSI Sys., Vol. 22, No. 2, February 2014.
5. Fan.H, Han.X, Wei.Q, Yang.H, "A 12-bit self-calibrating SAR ADC achieving a Nyquist 90.4-dB SFDR", Springer Analog Integ. Cir. Sig. Process (2013) 74:239–254.
6. Mohammad Taherzadeh-Sani and Anas A. Hamoui," A Reconfigurable and Power-Scalable 10–12 Bit 0.4–44 MS/s Pipelined ADC With 0.35–0.5 pJ/Step in 1.2 V 90 nm Digital CMOS", IEEE Tran. On Cir. And Sys.I: Regular Papers, Vol. 60, No. 1, January 2013
7. Si-Seng Wong, U-Fat Chio, YanZhu, Sai-Weng Sin, Seng-Pan U and Rui Paulo Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC", IEEE Journal Of Solid-State Cir., Vol. 48, No. 8, August2013.
8. B. P. Ginsburg and A. P. Chandrakasan, "Dual Time-Interleaved Successive Approximation Register ADCs for an Ultra-Wideband Receiver," IEEE J. Solid-State Cir., vol. 42, no. 2, pp. 247–257, Feb, 2007.
9. Nagarathinam S, David S. An Improved Comparator Structure For 8-Bit SAR ADCs : A Review. IJPAM, Dec 2017. Vol. 117 No. 8 2017, 145-148
10. M.Ramakrishnan,C.Nalini,"Analysis And Classification Of Risk Assessment In Patients Suffering From Congestive Heart Failure By Using Computer Based Statistics", International Journal of Innovations in Scientific and Engineering Research (IJISER), Vol 1 Issue 2 FEB 2014/107,pp88-93.
11. P. JebaSanthiya1 and D.Murugan, "Soft Computing Based Classification of Electrogastrogra M Signals", International Journal of Engineering
12. Vijayanandh R, Senthil Kumar M , Vasantharaj C , Raj Kumar G , Soundarya S, "Numerical Study On Structural Health Monitoring For Unmanned Aerial Vehicle", Journal of Advanced Research in Dynamical and Control Systems,Vol-9,Sp– 6 / 2017,pp1937-1958.