High Performance Baugh-Wooley Multiplier Using HPM

Nagarathinam S, Shanthi D

Abstract: ***This paper proposes a high speed multiplier designusing VHDL (Very High Speed Integrated Circuits Hardware Description Language). In Booth multiplier multiplication process is done by both encoding and decoding. The Baugh-Wooley algorithm is performing signed multiplication and two's complement. In both modified Baugh-Wooley and modified Booth recoded multiplier the critical path delay has been reduced by using HPM tree concept and the speed is enhanced. Here the design of 8-bit Modified Baugh-Wooley multiplier and Booth multiplier has been designed and implemented byconventional method and also using High-Performance Multiplier Reduction tree (HPM) method. The speed of Modified HPM Baugh-Wooley operation is increased by appending ripple carry adder. The results are evaluated and synthesized using Xilinx ISE 14.7and Spartan 6 device has been chosen for simulation.***

Key Words: HPM tree, FPGA, VHDL, Ripple carry adder, Xilinx, Modified Baugh-Wooley multiplier.

I. INTRODUCTION

The multipliers are such an important element in the digital signal processing for convolution and Filtering. It is a source function for various multipliers. In the serial multipliers single digit operation is carried out between several digits[1]. Any system such as filter or a processing system, the performance depends on multipliers because they are generally slower elements. These multipliers have moderate performance in both speed and area.The main topologies.

Partial-product generator (PPG)
Partial-product reducer (PPR)
Vector merge adder (VMA)

An 8-bit Modified Baugh Wooley and ModifiedBooth multiplier uses ripple carry adder (RCA) which is designed to have delay time reduction. In the radix-2 Baugh-Wooley (BW2) multiplier presents a simple and consecutive way implementation, and the radix-4 Booth-recoded (BR4) multiplier is quite complex structure and high-speed multiplier[2]. Initially the multiplication process was carried out by using addition, subtraction and shifting operations as a sequence.The multiplication method has been extended for both signed and unsigned numbers, through a two's complement number system. Both topologies are using fixed point two's complement as number representation andit is implemented to perform signed multiplication. The proposed multiplier differs from partial product method and it usespartial-products reducer (PPR) and the vector-merging adder (VMA),

this has been implemented as a carry-save adder with (m,2) compressors and a carry-propagate adder, respectively in radix-28-bit Baugh-Wooley multiplier and radix-4 booth multiplier[2].Thegated instance of the multiplicand is delayed and placed in asame column of the shifted partial product matrix. While the carry-save adder and a carry-propagate adder is replaced with ripple carry adder in 8-bit modified HPMBaugh-Wooleymultiplier[3].

II. LITERATURE SURVEY

Baugh-Wooley multiplier is the efficient and high-speed multiplier compared with other conventional multipliers. Here the regularity of the multiplier is maximized. The Baugh-Wooley multiplier switches on signed operands with 2's complement number to make the signs of all the partial products to be positive. Proposed method uses two modules

- Brent-Kung adder,
- Prefix adder

which is introduced for the better performance and balancing at a power cost as well as area. This prefix adder has an inverse carry and complex carry tree. A tree can be divided into 2types they are the tree and an inverse tree. The partial products is added to a signed number while multiplying Two's complement numbers directly. After thiseach partial product has been extendedwith respect to thewidth of the final product term in order to have a correct added sum by the Carry Save Adder referred to as PM (partial products with magnitude part) and spawn by one NAND and three AND operations[4].

In digital signal processing applications multiplication in number is performed by the Baugh-Wooley algorithm. It is the best well-known algorithm. The delay is minimized by using this algorithm and the speed is increased. By using decomposition logic method a high-speed multiplier is designed and implemented in a Baugh-Wooley algorithm. The result is compared with modified booth multiplier and Vedic multiplier. In use of different Multipliers, they applied the Baugh-Wooley algorithm and it is implemented to get the minimum delay, low power distraction and minimum area than Vedic and modified Booth multipliers[5].

Magnus Sjalander and Per Larsson-Edefors, An 8-bit Baugh-Wooley algorithm case, According to Hatamian's scheme the partial-product bits have been reconstructed. Here they clearly verified that the reduction arrays are based

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on BW implementations. In this paper,[16][17]however, they have chosen the HPM reduction and the implementation of BW algorithm.By using a 2-input AND gate for every pair of multiplicand bits of the partial-product bits are generated.

Where the partial-product bit to be inverted, rather they used a 2-input NAND gate[6].

III. EXISTING WORK

Baugh-Wooley algorithm is based on unsigned binary multiplication. At each level of addition, Carryout obtained from the chain of Half-Adders and Full-Adders will be the most significant bit. The multiplier Baugh-Wooley may also perform multiplication in negative bits. This radix-2 multiplier is a simple structure multiplier which provides moderate silicon area and it is ease of making medium operating speed[7]. Fig. 1 illustrates the step by step process of partial-product multiplication concept of this topology.

The two input bits are given to the PPG to execute the Baugh-Wooley and Booth scheme, then it has been given to PPR implementation in carry-save adder with (m,2) compressors[2].

At each side of the compressors, Half-Adders and Full-Adders are placed in a tree structure pattern for the reduction of the critical path of partial-product reducer. In the region of a vector-merging adder, the PPR sums and carries are feeds to the carry-propagate adder as a VMA implementation which gives the final result of the multiplication. In multiplier structure, the PPR structure is quite complex and therefore consumption of the power is more.

The shift and add is the first and foremost operation of the PPR. In this design the partial products are generated using shift and add operation and this is carried out in the main building blocks of a multiplier, but it is to be implemented with Half-Adders and Full-Adders. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content[6][7].The diverting function of logic gates can be diminished by increasing the possibility of having balanced logic-zeros at the inputs, which resemble imposing more number of partial products to be equal to zero. This can be attained by bringing an enormous sum of bits which are equal to zero in the gutter of one of the two input words. In the operation, the approximations are the abode, we can feat this equity to anxiously select perpetual multiplier coefficients to cut down the power utilization at runtime[8].

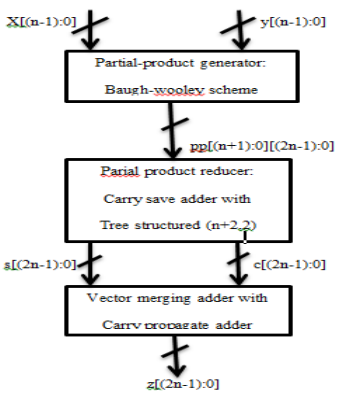

Fig 1 Structure of n×n bit Baugh-Wooley multiplier

To calculate the probable idea, the switching activity is calculated while one input operand is held steady and the other input operand accepts arbitrary data. In Booth multiplier, each partial bits are merged with vector adder. The number of partial products will also affect the power dissipation of a system. Hence we can reduce the non zero partial products to achieve power saving.[2].

Normally in the signed multiplication method the number of partial products and their duration is much larger. So a newalgorithm was used for signed multiplication called as Baugh Wooleyalgorithm[5]. The Baugh-Wooley multiplication is one of the best and cheap method to carry out signed bits. This algorithm is developed for designing regular multipliers, with 2's complement numbers. This multiplication process uses a left shift algorithm also it uses a multiplexer for choosing the multiplication bit.

IV. MULTIPLICATION PROCESS

Baugh-Wooley multiplier is the simple and well-known algorithm. The Booth multiplier is straightway and fastest algorithm. In this paper objective and implementation of a conventional method for an 8-bit Baugh-Wooley multiplier and Booth multiplier has been done and compared the result achieved with a Modified HPM Baugh-Wooley and Booth multiplier algorithm. The Baugh-Wooley multiplier is a motivating implementation of a multiplier. The High-Speed Booth Encoded Multiplier the multiplicand, multiplier and products are defined as number to be added, number of times that it is added, and the result and alsoeach full adder in the multiplier performs the same number of computations, with the crosswise ripple carry Propagating the input signal a constant as well as same number of times[9][10].

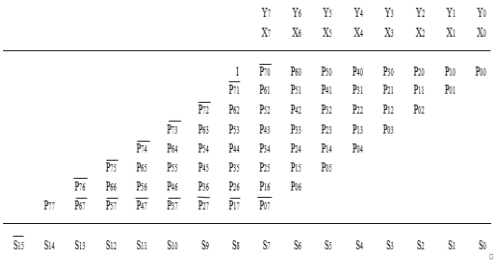

Fig 2An 8×8 bit Baugh-Wooley Multiplication

V. MODIFIED BOOTH MULTIPLIER

The Modifiedradix-4 Booth's algorithm has inevitable encoding time in 16x16 bit multiplication. The BoothAlgorithm has a 3 cross term which means that a partial product cannot be achievedby shifting[11]. Accordingly, it is needed in encoding processing. It is feasible to minimize the number of partial products by half, by using the method of Radix-4 Boothrecoding[12]. If we use three or four operands in a two operand adder the carry propagation will

also repeated many times. We applied the modified Booth encoding (MBE) technique proposed in [2].

This will be the best method for encoding and decoding with respect to booth algorithm. In the design of reduction trees with log logic depth the number of partial products are limited and the total performance has been enhanced.

The main limitation of this authentic Booth algorithm is that the number of recoded partial products generated on the input operand, this may lead to improper hardware design[13].

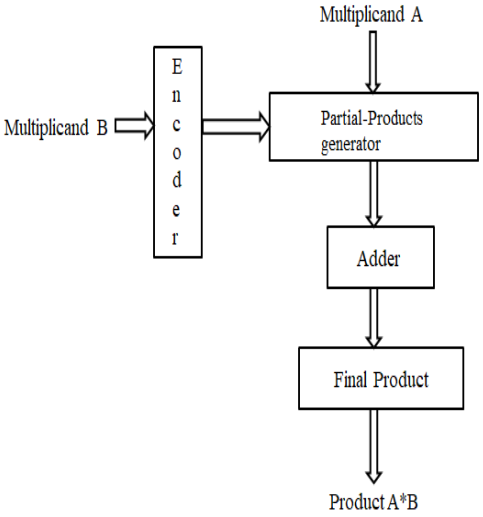

Fig 3 Block diagram of Modified Booth Multiplier.

VI. PROPOSED WORK

Here the 8-bit Baugh-Wooley and Booth multiplier is designed and implemented by using conventional method. This Baugh-Wooley Multiplier provides an impressive implementation by using the shift and adds method with high-speed Multiplier. Some of the parallel multipliers are designed with lesser iterative steps and lesser adders.

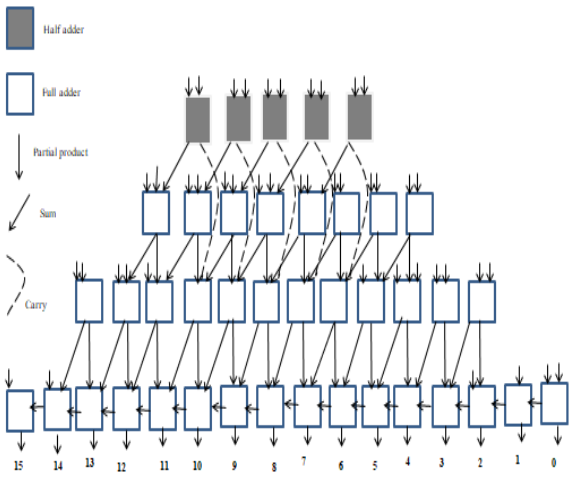

Fig 4 HPM block of Modified Booth Multiplier

Booths algorithm involves encoding of multiplier bits and partial product generation. It is very important that the high expression system and fabrication of chips require components as small as possible.

Different modified booths algorithms have been proposed according to how many numbers of bits are used to encode multiplier. Baugh-Wooley multiplier is treated with straightforward multiplication for both signed and unsigned operands. Since the partial products are quite harder hence it need to be maximized for the regularity of multiplication array and lifted negative signs are used in the last stages.

Modified booth algorithm may lead to minimized number ofpartial products. The implementation of Baugh-Wooley multiplier is a frustrating implementation of a multiplier. This enables the design of a quite standard cell shape for easy manufacturing. User can design a very largeBooth multiplier by adding large number of multiplicands.

The full adder in the multiplier design executessame number of computations,with the crosswise ripple carry propagating the input signal.The stoppage of a multiplier is determined by the number of additions to be executed.

In this proposed work, the Modified HPM Baugh-Wooley multiplier and Booth multiplier has been designed and implemented.

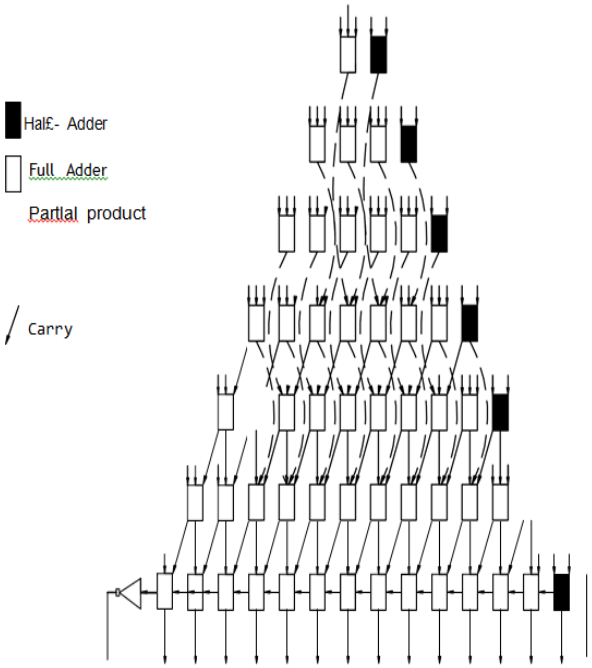

Fig 5HPM block of Baugh-Wooley

At the time of multiplication process, all the partial-products are multiplied as per the actual method in Baugh-Wooley multiplier wherein the Modified HPM Baugh-Wooley multiplier, half of the partial-products are reduced by taken the triangular tree pattern multiplication and it has been inverted finally with adding 1 at the final result. The same process has been done in Modified Booth multiplier.

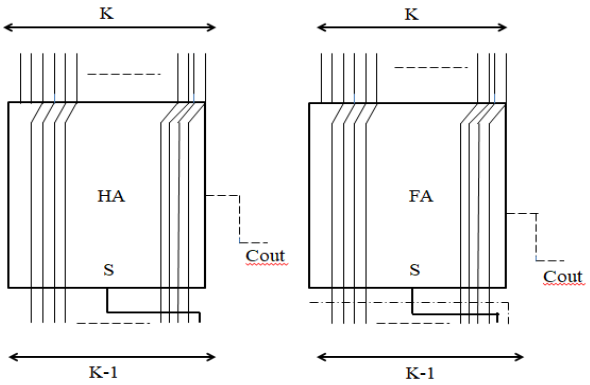

Fig 6 HPM Half-Adder and Full-Adder Cell

The triangular cell pattern has been done with the partial-products reducer, the reason for applying triangular tree pattern is to reduce the tree technique and to achieve a shorter wire length. In the sense modified means changing the structure of the adders and the HPM concept is multiplying the bits with triangular tree pattern.Thus the size of the partial-products is reduced half of the length. Therefore finally we could get the reduced delay time with high performance. The comparative analysis has been done to make sure that the Modified HPM Baugh-Wooley multiplier design is faster and performed better than other conventional multipliers.

VII. SIMULATION RESULTS

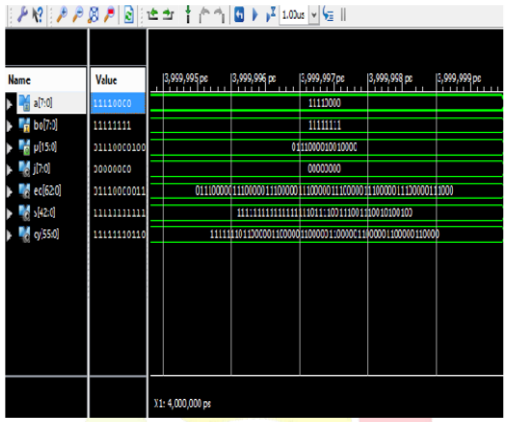

Fig 7 Simulation result of 8-bit Baugh-wooley multiplier

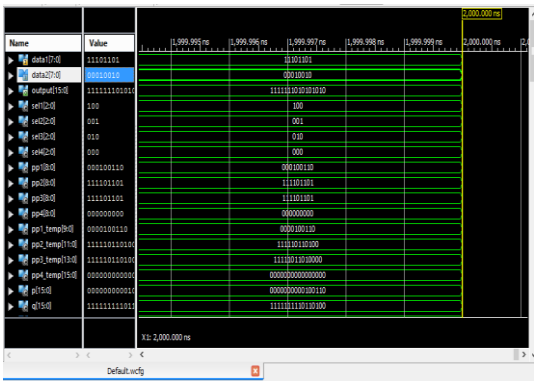

Fig 8 Simulation result ofmodified HPM Booth Multiplier

VIII. DEVICE UTILIZATION TABLE

Logic utilization	Used	Available	Utilization
Number of slices	73	963	7%
Number of 4 input LUTs	127	1920	6%
Number of bonded IOs	32	108	29%

Fig 9 Device Utilization Table For Baugh-Wooley Multiplier.

Logic utilization	Used	Available	Utilization
Number of slices	73	960	7%
Number of 4 input LUTs	135	1920	7%
Number of bonded IOs	32	108	29%

Fig 10 Device Utilization Table For Modified HPM Baugh-Wooley Multiplier

IX. CONCLUSION

Analysis of Modified HPM Baugh-wooley multiplier and Booth multiplied using conventional methods has been designed and implemented as well as synthesized in Xilinx ISE 14.7 simulator. The simulation result and RTL schematic of the Modified HPM Baugh-Wooley and Booth multiplier is shown in Figure 8.2. The Baugh-wooley multiplier of the delay time is calculated as 32.153ns.Then the Modified HPM Baugh-Wooley multiplier is calculated as 24.32ns. From the delay calculation it is found that, the Modified HPM Baugh-Wooley multiplier performs better.

FUTURE SCOPE

Baugh-wooley multiplier can be compared with performance of other multiplier such as Booth, Dadda, Wallace tree multipliers and also it is possible to reduce the power and delay using HPM. the proposed multiplier can be further extended for 16X16, 32X32 bits. The efficient multipliers can be designed as well as implemented on FPGA[18] and can be used for designing digital signal processing, VLSI signal processing, Cryptography applications.

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