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FPGA based Speed Control of Three Phase Induction Motor

P.Selvabharathi, V.Kamatchi Kannan, S.Sathish kumar

Abstract: ***Three phase induction motor is controlled using three phase sinusoidal FPGA controller with constant V/F ratio. The controller is designed in a single integrated circuit to control both voltage and frequency simultaneously. The single control IC is implemented using FPGA and controller outputs like voltage, frequency are controlled by clock frequency. Single edge sinusoidal PWM technology is proposed for this controller and it operates up to 2 kHz of fundamental frequency and 30 kHz of switching frequency. Delay time is provided for inverter switches to avoid shoot through fault in the inverter legs. IGBT switches are used in inverters for variable voltage variable frequency drives and switching power supplies. Dead time for the IGBT switches is adjustable. FPGA controller is used to generate Sinusoidal Pulse Width Modulation signal to operate induction motor at variable voltage and variable frequency.***

Keywords: FPGA, speed control, induction motor, PWM technology.

I.INTRODUCTION

In many industries induction motor drives are widely used for variable speed applications and power conditioning systems. Three phase induction motor is operated at variable voltage and variable frequency and it is controlled electronically. Three phase inverters are exclusively used in conversion process where dc voltage is converted into three phase ac voltage. In three phase AC drives, PWM technique is plays a vital role in minimizing the harmonics and switching losses in the power converters [1-2].

Many PWM techniques had been employed to control the speed of AC drives with improved performance in digital control. Different voltage control schemes of three phase inverters are sinusoidal PWM, third harmonic PWM, space vector pulse width modulation, selected harmonic injection PWM, selected harmonic elimination PWM techniques [1-2]. But most commonly used methods are SPWM and space vector PWM technique.

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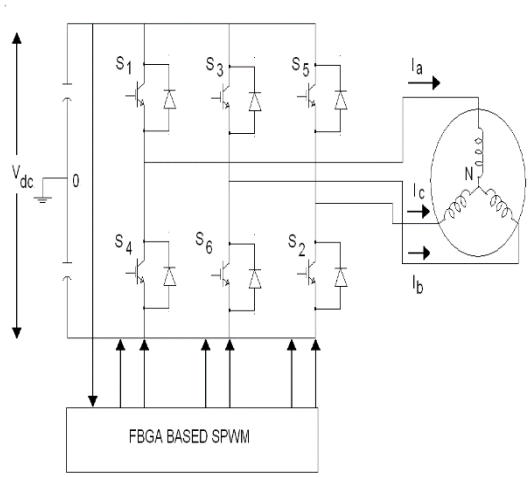

Fig.1 Controller for three phase Induction Motor

II. PRINCIPLE OF SINUSOIDAL PWM

Most commonly used PWM technique is sinusoidal pulse width modulation to reduce the harmonics in the output voltage. In SPWM pulses are generated by comparing sinusoidal reference signal and triangular carrier signal as shown in fig.2

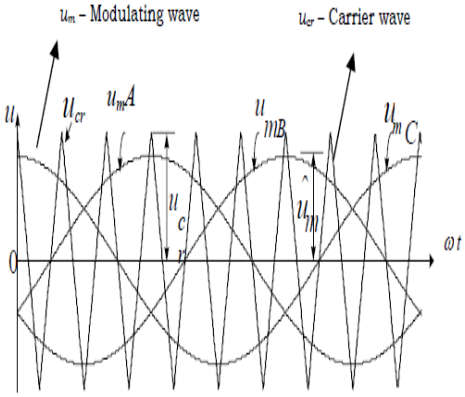

Fig 2.SPWM Pulse Generation

Amplitude modulation ratio is given by

$$M_a = \frac{\hat{u}_m}{\hat{u}_{cr}} \quad (1)$$

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Frequency modulation ratio is given by

$$M_f = \frac{f_{cr}}{f_m} \quad (2)$$

Where fcr is the carrier frequency and f_m is the modulating frequency.

The working principle of designed controller is sinusoidal PWM technique. The PWM pulse generation, as shown in figure 3.

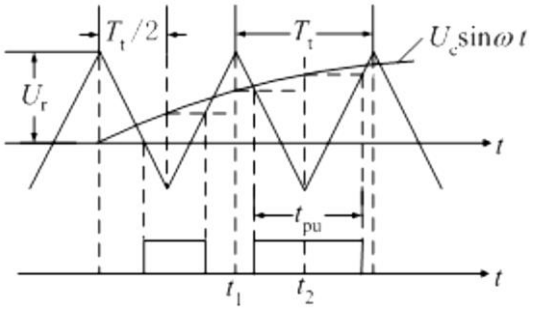

Fig.3. Asymmetric regular sample

Ur is the maximum value of carrier signal, and *Uc* is the maximum value of the sinusoidal reference signal. T_t - time period of triangular carrier and ω - angular frequency of the sinusoidal reference signal. SPWM pulse width is T_{pu} and modulation index is M

$$t_1 = \frac{T_t}{2}k \quad (\text{when } k = 0,2,4,6,\cdots)$$
$$t_2 = \frac{T_t}{2}k \quad (\text{when } k = 1,3,5,7,\cdots) \quad (3)$$

Where the time t_1, t_2 are the sampling points.

III. ANALYSIS OF CIRCUITRY PARAMETERS

To eliminate harmonics and guarantee three phase symmetrical waveform, the layout adopts modulation technique and the whole frequency is break up into 8 segments, each segment similar to a exclusive switching frequencies. Motor speed is high for lower switching frequency and motor speed is low for higher switching frequency.

A. Clock frequency is represented as

$$f_{\text{clkfc}} = 3360 \times f \quad (\text{Hz}) \quad (4)$$

B. The fundamental output voltage of the inverter is controlled using fundamental voltage control clock. Modulation index is varied between zeros to one; when modulation index is equal to one. The output frequency reaches maximum value during 100% modulation. If modulation index is greater than one it is called over modulation.

The relation between *f*clkvc and f_M is expressed as

$$f_{\text{clkvc}} = 6720 f_M \quad (5)$$

Relationship between the fundamental voltage and fundamental frequency as shown in the fig 4.

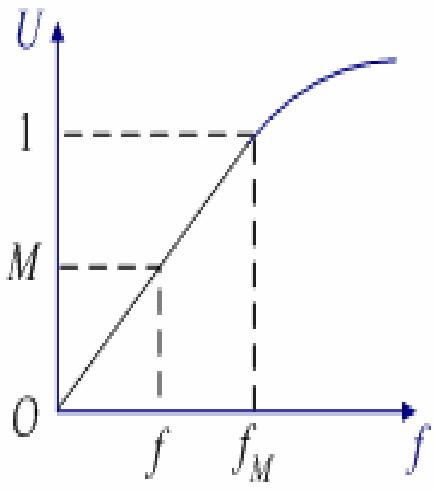

Fig.4.Relationship between modulating frequency and fundamental Frequency

When fundamental frequency is less than modulating frequency the relationship between modulating frequency and fundamental is linear but if fundamental frequency is greater than modulating frequency U and f *is* nonlinear. If the fundamental clock control voltage is constant, voltage to frequency (U / F) ratio is constant.

C. The relationship between clock frequency and maximum switching frequency is expressed

$$f_{\text{clkrc}} = 280 f_{\text{rmax}}$$
$$f_{\text{rmin}} = 0.6 f_{\text{rmax}} \quad (6)$$

D. Dead time clock pulse is represented as Clkdead. Where td is a dead time and K is the select signal. Clock pulse frequency for dead time block is given below.

$$f_{\text{clkdead}} = \begin{cases} 8/t_d & (\text{when } K = 0) \\ 16/t_d & (\text{when } K = 1) \end{cases}$$

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IV. FPGA BASED CIRCUIT DESIGN

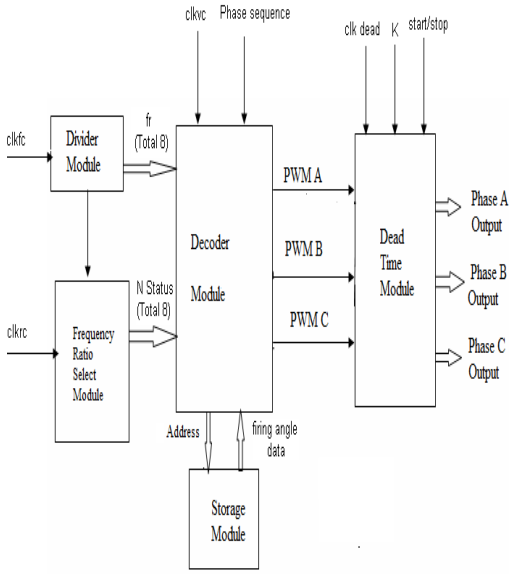

Figure.5.Block diagram of SPWM IC

Block diagram of SPWM IC as shown in fig 5. The whole Sinusoidal Pulse Width Modulation controller IC is divided into five parts [7-8]. Decoder module is used to generate PWM pulses for three phase inverter. Delay time is provided for inverter legs to avoid shoot through Fault. Storage module has the firing pulse data and its address which is given to the decoder module.

A. Divider Module

Frequency divider module as shown in fig 6. The input clock frequency is divided into eight frequency segments. Two types of module counters and reshape circuit is used to divide the input clock pulse frequency into different frequency ratios.

B. Frequency Ratio Select Module

Frequency ratio select module as shown in fig 7. It consists of nine bit counter and frequency halves circuit. The reference frequency is divider output clock pulse. The state of N is decided by frequency ratio select module. The State switching diagram as shown in figure.8

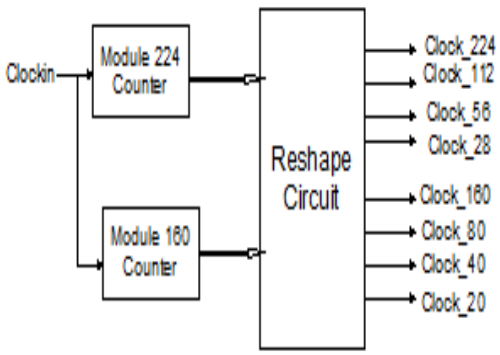

Fig.6. Frequency Divider Module

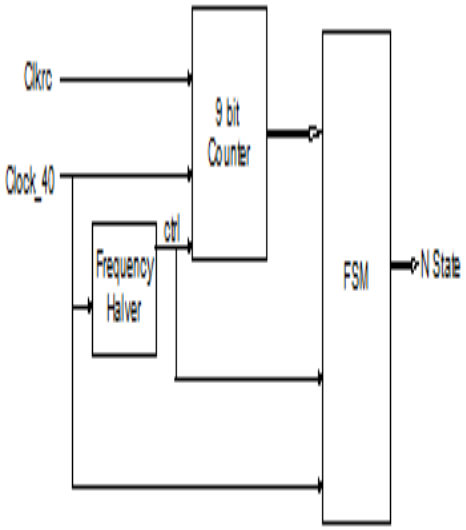

Fig.7. Frequency ratio select module

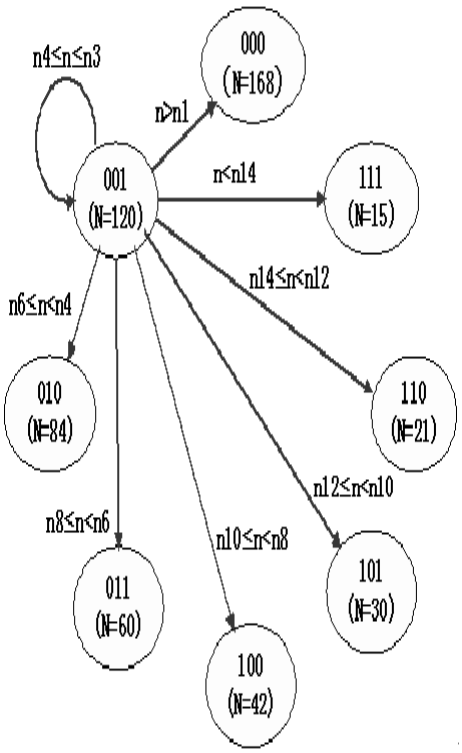

Fig.8. State Switching diagram

C.Decoder And Storage Module

PWM pulses are given to the three phase inverter by decoder module. Decoder module consists of positive counter, negative counter and PWM generator.PWM signals are generated from the counter based on the firing angle. Firing angle may be positive or negative. Decoder and memory module as shown in figure 9.

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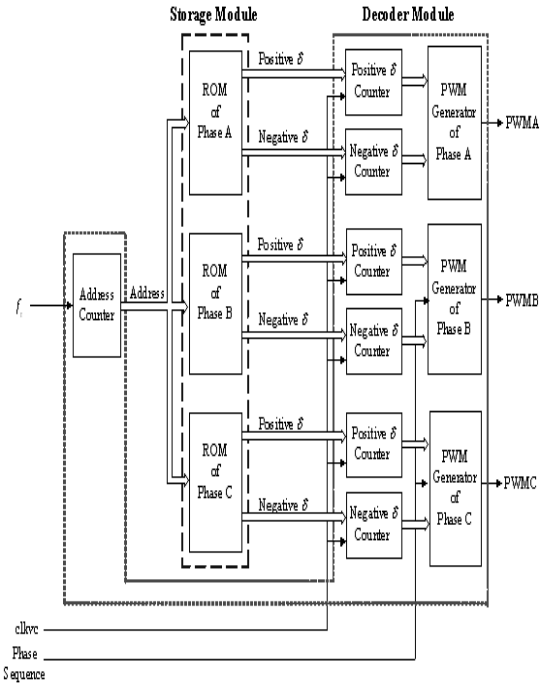

Fig.9. Decoder and Memory Module

D.Dead Time Module

Inverter consists of semiconductor switching devices like MOSFET and IGBT. The power semiconductor switching devices are not ideal. Two switching devices are turn on simultaneously in same inverter leg it leads to shoot through fault in the inverter. To avoid this fault delay time is introduced between two switches in the inverter leg. The delay time is called dead time. Dead time is chosen as microseconds for fast operating switching devices like MOSFET and IGBT.

V.SIMULATION

Simulation of FPGA based sinusoidal pulse width modulation has been done using MODELSIM.Circuits are designed by VHDL language. It stands for VHSIC hardware description language. SPWM pulse generation for three phase inverter is shown in figure 10. Simulation waveforms of FPGA based sinusoidal pulse width modulated controller and inverter switching frequency at 2.63 KHz as shown in the fig.11.

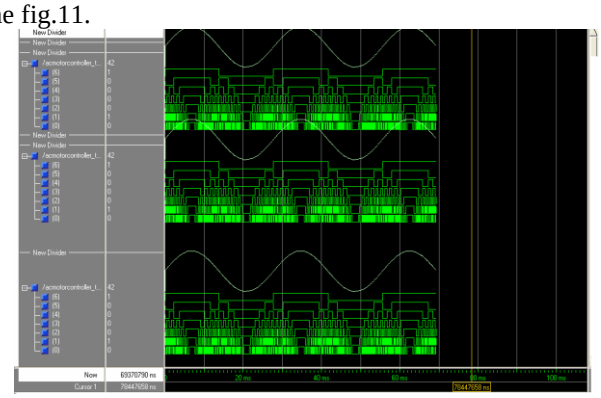

Fig.10.SPWM pulses for three phase inverter

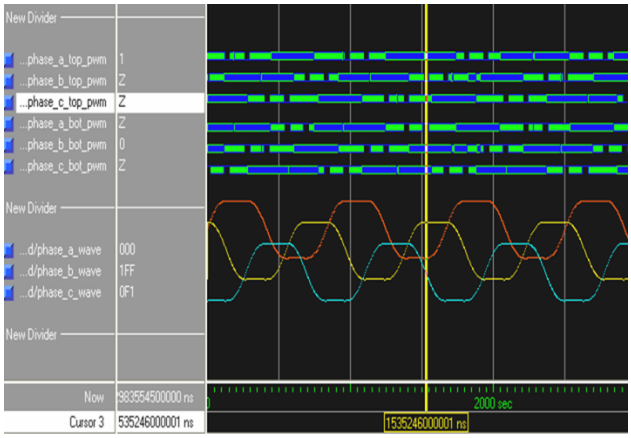

Fig.11. Inverter Switching Frequency 2.63 KHz

Fig.12.Experimental setup of SPWM controller

Experimental setup consist of input power module, FPGA controller SPARTRAN XC3S400,three phase inverter,driver circuit,isolation transformer and induction motor.The experimental setup is shown in fig.12.Input power module consist of bridge rectifier,filter and voltage regulator.The three phase inverter consist of six power MOSFETs IRF840.Isolation is provided between the FPGA controller and three phase inverter module using opto isolator SFH615a.Three phase induction motor have following specifications. 0.25HP, 1Amps, 1350 rpm. FPGA controller is used to generate SPWM pulses at various switching frequencies to operate induction motor at variable voltage and variable frequency.

VI.CONCLUSION

Design of FPGA based SPWM control IC for three phase induction motor has been implemented. This SPWM control IC was implemented using FPGA technology to operate induction motor drives at variable voltage and variable frequency. SPWM pulses are generated for three phase inverter using Xilinx simulation tool and experimental results are verified.

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The inverter is operated at wide range of switching frequencies and SPWM pulses are generated at various fundamental frequencies.

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