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Performance and Dynamic Analysis of Single Switch AC-DC Buck-Boost Buck Converter

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Abstract*: Dynamic analysis of proposed single switch ac-dc buck-boost buck converter is presented in this paper. The proposed converter is an integrated converter contains two inductors, one is at input side and other one is at output side. To achieve unity power factor at input terminals, the input inductor is designed for discontinuous mode (DCM). This condition will eliminate extra control technique for power factor correction (PFC). The output side inductor is operated in DCM to reduce the bus capacitor voltage, thereby reducing the capacitance size. A PI controller is designed to regulate the pulses for the converter. The proposed converter is designed in MATLAB software for 60V output voltage. The analysis has been done for three different cases (variable frequency, variable input and variable load) to verify the converter performance.

Index Terms*: Single switch, ac-dc converter, buck-boost, power factor correction (PFC), dynamic analysis.

I. INTRODUCTION

To achieve quality input power from the supply, the PFC system is required for ac-dc converters. Compared with two-stage configurations the single stage configurations have many advantages. Several single-stage PFC configurations have proposed by using one active switch with a single control loop. These configurations are best examples for achieving both PFC and fast output voltage regulation. Using single switch with a simple control loop gives a cost-effective solution. The switch voltages are dependent on intermediate bus capacitor voltage generally varied with input and load [1]–[3]. So, single-switch converters experience high switching voltage stresses because of high ripple voltage on the dc bus capacitor. As a result, a large dc bus capacitor, and high-rated switches (both active and passive) will be needed to design single stage converters. This condition leads to increase in size and cost of the converter which also affects the efficiency as well as reliability of the converter. It limits the single-switch converters, in many applications whose voltage is greater than 400V.

To decrease the voltage on the bus capacitor, many techniques have been initiated [4]–[6]. Though, many of these configurations contain a boost converter at the input side for PFC capabilities. But, these topologies can't fit for low voltage applications. Many applications require large range of input to output voltage conversions M(d). This requirement asks the switch to operate at extremely low duty cycles, which is not possible with higher switching frequencies because of minimum turn-on time. This limits M_{min}

To extend the conversion range, the two conventional converters are cascaded in this paper. In this paper, buck–boost converter is used as input converter due to its better PFC qualities compared with other converters [7]. Buck converter is used at output to attain lower output voltages. The buck–boost converter is capable of producing both step-up/down voltages with unity power factor. The buck-boost converter is operated in DCM to avoid extra control technique which makes the converter simple and cost effective. Hence, the proposed converter is capable of achieving extended voltage conversion ratio M(d) along with high power factor. Additionally, the intermediate bus capacitor voltage is made independent to load variations by operating the buck converter in DCM [8]. The main objective of this paper is to overcome the drawbacks of the single-switch topologies available in literature.

II. PROPOSED SINGLE SWITCH AC-DC CONVERTER

Figure.1 shows the circuit diagram of proposed single switch ac-dc converter. To analyze the converter the assumptions considered are, input voltage V_s is ideal sinusoidal wave with a line frequency f_L of 50 Hz, zero losses, constant capacitor voltage V_{Cr} and output voltage V_0, *the* inductor current i_{Lr} reaches zero before the current i_{L0}. With the above considerations, the converter operation in steady-state is given in four modes over a switching cycle T_s. the operating modes with theoretical waveforms are shown in fig. 2&3 respectively.

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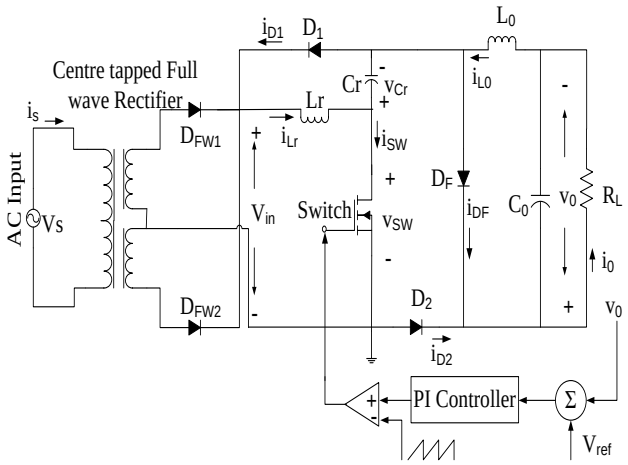


Fig. 1: Proposed single switch ac-dc converter

A. 1st Mode:

The switch *S* is turned on at t = t_0, S carries load current i_0 and i_{Lr}. The inductor L_r current i_{Lr} increases from zero. The D_2 is forward biased where the other diodes are reversed bias. Fig. 2(a) shows the 1st mode operation with current flow.

B. 2nd Mode:

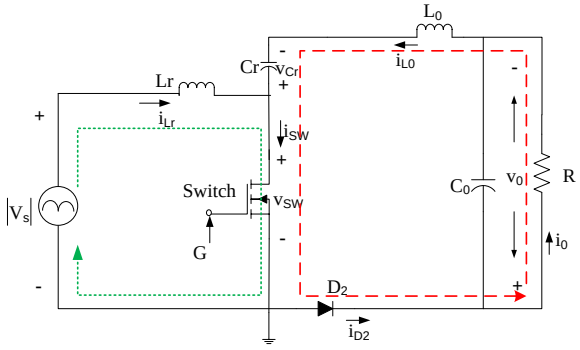
The switch S is turned off at t=t_1, the inductor discharges its energy to the capacitor C_r via diode D_1. The current i_{L0} discharges through diode D_F as shown in Fig. 2(b). This mode of will stop when the current i_{Lr} reaches to zero.

C. 3rd Mode:

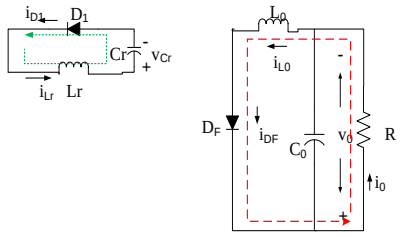
Fig. 2(c) shows the mode-3 operation. In this mode the current i_{Lr} is zero but i_{L0} delivers it energy continuously to the load. The mode continues until the current i_{L0} reaches to zero.

D. 4th Mode:

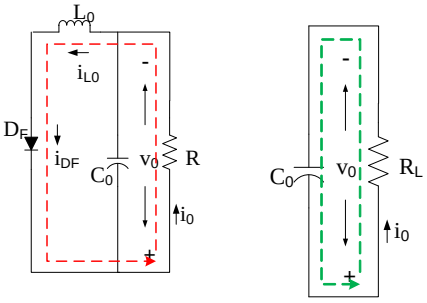
This is a small duration formed due to DCM operation of the buck inductor as shown in 2(d).



(a)



(b)



(c) (d)

Fig. 2 Operating modes of proposed converter

III. ANALYSIS & MODELLING

The proposed converter voltage conversion ratio M(d_1) can be calculated based the operation of the converter. If the proposed converter is operating in continuous conduction mode (CCM), then the M(d_1) can be derived as following.

A. Voltage conversion ratio M(d_1) in CCM

When switch S is ON, the inductor voltage equations are

$$L_r \frac{di_{Lr}}{dt} = v_s$$

$$L_0 \frac{di_{L0}}{dt} = v_{Cr} - v_0 \qquad (1)$$

When switch S is OFF,

$$L_r \frac{di_{Lr}}{dt} = -v_{Cr}$$

$$L_0 \frac{di_{L0}}{dt} = -v_0 \qquad (2)$$

Voltage across the bus capacitor v_{Cr} and output voltage v_0 are given by

$$v_{Cr} = \frac{d_1}{1-d_1} v_s$$

$$v_0 = d_1 v_{Cr} \qquad (3)$$

Therefore the conversion ratio M (d_1) can be derived as

$$M(d_1) = \frac{v_0}{v_s} = \frac{{d_1}^2}{(1-d_1)} \qquad (4)$$

From eq. (4) it can be noted that the proposed converter is a quadratic function of duty ratio (d_1). Hence the proposed converter has wide voltage conversion ratio.

But, in this paper the converter is operating in complete DCM mode (input-DCM & output-DCM). So eq. (4) cannot be valid for the proposed analysis.

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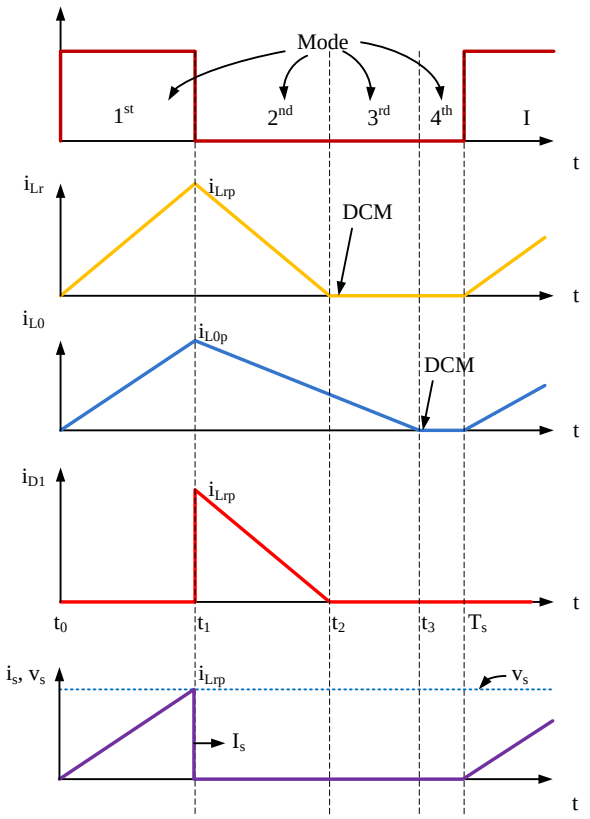

Fig. 3 Theoretical waveforms over a switching cycle (T_s)

B. Voltage conversion ratio M(d_1) in DCM

The input current at line frequency is given as [1]:

$$\langle i_s \rangle = \frac{i_{sp}}{2T_s} d_1 T_s = \frac{{d_1}^2 V_S}{2L_r f_s} sin\omega_L t \qquad (5)$$

where $\langle i_s \rangle$ is input current at time t, i_{sp} is the peak current of each current pulse, V_S is the peak voltage of the supply.

The input power P_s can be written for a single phase source with unity input power factor is given by

$$P_s = \frac{1}{2} V_s \langle i_{sp} \rangle = \frac{{d_1}^2 {V_s}^2}{4L_r f_s} \qquad (6)$$

Similarly, the output power is given as

$$P_0 = \frac{{V_0}^2}{R} \qquad (7)$$

Using Eqs. (6) and (7), the average output voltage V_0 can be obtained as

$$V_0 = \frac{d_1 V_s}{2} \sqrt{\frac{R}{L_r f_s}} \qquad (8)$$

From eq. (8) the voltage conversion ratio M(d_1) for the converter operating in complete DCM is given as

$$M(D) = \frac{d_1}{\sqrt{2k}} \qquad (9)$$

The factor k is given by

$$k = \frac{2L_r f_s}{R} \qquad (10)$$

From eq. (9) it is clear that the voltage conversion ratio M(d_1) for the proposed converter has wide range compared with conventional converters.

C. Modeling Equations:

The modeling equations of the converter operating in complete DCM can be written as [7]

$$L_r \frac{di_{Lr}}{dt} = \begin{cases} |v_s| & for[t_0, t_1] \\ -v_{Cr} & for[t_1, t_2] \\ 0 & for[t_2, t_3] \end{cases}$$
$$C_r \frac{dv_{Cr}}{dt} = \begin{cases} -i_{L0} & for[t_0, t_1] \\ i_{Lr} & for[t_1, t_2] \\ 0 & for[t_2, t_3] \end{cases} \qquad (11)$$
$$L_0 \frac{di_{L0}}{dt} = \begin{cases} v_{Cr} - v_0 & for[t_0, t_1] \\ -v_0 & for[t_1, t_2] \\ -v_0 & for[t_2, t_3] \end{cases}$$

Using eqs. (1) & (2), the average rate of change of I_{Lr} over a switching cycle (T_s) is given as

$$\frac{d}{dt} I_{Lr} = \frac{T_{on}}{T_s L_r} V_s - \frac{T_2}{T_s L_r} V_{Cr} \qquad (12)$$

Similarly for I_{L0} and V_{Cr} are given as

$$\frac{d}{dt} I_{L0} = \frac{-R}{L_0} I_{L0} + \frac{T_{on}}{T_s L_0} V_{Cr}$$
$$\frac{d}{dt} V_{Cr} = \frac{T_2}{(T_{on} + T_2) C_r} I_{Lr} - \frac{T_{on}}{T_s C_r} I_{Lo} \qquad (13)$$

The above Equations can be represented in state space form as

$$\begin{bmatrix} \frac{d\langle I_{Lr} \rangle}{dt} \\ \frac{d\langle I_{L0} \rangle}{dt} \\ \frac{d\langle V_{Cr} \rangle}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{d_2}{L_r} \\ 0 & -\frac{R}{L_0} & \frac{d_1}{L_0} \\ \frac{d_2}{(d_1 + d_2) C_r} & -\frac{d_1}{C_r} & 0 \end{bmatrix} \begin{bmatrix} \langle I_{Lr} \rangle \\ \langle I_{L0} \rangle \\ \langle V_{Cr} \rangle \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L_r} \\ 0 \\ 0 \end{bmatrix} |v_s| \qquad (14)$$

where $d_1=(t_1-t_0)/T_s$ and $d_2=(t_2-t_1)/T_s$

IV. CONTROL & DESIGN

A. Design:

The design equations for the converter parameters L_r, C_r, and L_0 are discussed in this section. The output filter capacitor C_0 is chosen according to the allowable ripple in the output voltage.

From eq. (6), the inductor L_r can be calculated by

$$L_r = \frac{{d_1}^2 {V_s}^2}{4P_0 f_s} \qquad (15)$$

The bus capacitor ripple (ΔV_{Cr}) is given as [7]

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$$\Delta V_{Cr} = \frac{{d_1}^2 {V_s}^2}{8\pi L_r f_s f_L V_{Cr}} \frac{1}{C_r} \quad (16)$$

So the dc bus capacitor C_r, for a given voltage ripple (ΔV_{Cr}) is given by

$$C_r = \frac{{d_1}^2 {V_s}^2}{8\pi L_r f_s f_L V_{Cr} \Delta V_{Cr}} \quad (17)$$

The value of L_0 given by Eq. (18) also depends on d_1, similar to the capacitance voltage (v_{Cr}):

$$L_0 = \frac{(V_{Cr} - V_0) d_1}{f_s \Delta i_{L0}} \quad (18)$$

Table-I
Design parameters

Parameter	Value
Supply Frequency (f_L)	50 Hz
Switching Frequency (f_s)	10 kHz
Input inductor L_r	2.25mH
Bus capacitor C_r	5uF
Output inductor L_0	3mH
Output filter capacitor C_0	1000uF
Centre tapped T/F Rating	230/60-0-60 V
Converter Input Voltage (V_s)	60Vrms

B. Controller:

Various transfer functions can be determined from Eq. (14). To compare the analytical model with converter simulated model, I_{L0} in Eq. (14) is linearized. The control-to-output transfer function $G(s)$ from $\langle I_{L0} \rangle$ (s) to d_1 (s) is obtained from Eq. (14) as

$$G(s) = \frac{\langle I_{L0} \rangle (s)}{d_1(s)} = \frac{V_{Cr}}{(s + R)} \quad (19)$$

Figure 4 shows the magnitude and phase plots of $G(s)$ for the analytical and simulated models. It can be noticed that the simulated results match the derived analytical model.

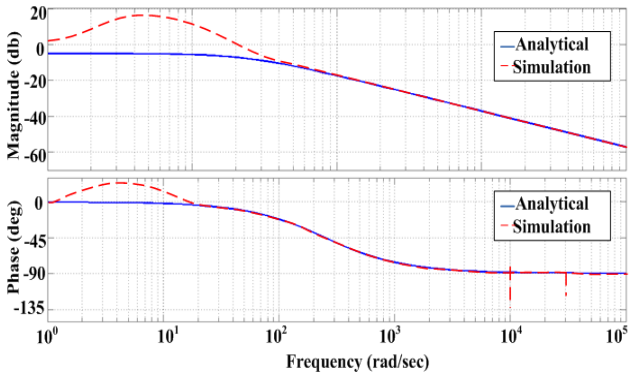

Fig. 4 The magnitude and phasor plots of $G(s)$ for the analytical and simulated models

C. Averaged Model:

The proposed single-switch ac-dc converter averaged circuit model is presented by averaging input current and the diode D_1, and D_2 currents over a switching time T_s and averaging the voltage across diode D_F.

From Fig. 3, the average input line current for a switching time T_s is given by

$$\langle i_s \rangle_{T_s} = \frac{1}{2} d_1 i_{Lrpk}(t) = \frac{v_s}{R_s} \quad (20)$$

where $R_s$is the input resistance (since L_r is in DCM) of the converter.

The average voltage across free-wheeling diode D_F is given as

$$\langle v_{DF} \rangle_{T_s} = a_0 v_{Cr} \quad (21)$$

where a_0 is given by

$$a_0 = \frac{L_r R_L}{2 L_0 R_s} \left(\sqrt{1 + \frac{4 L_0 R_s}{L_r R_L}} - 1 \right) \quad (22)$$

Similarly, the averaged currents of diodes D_1 and D_2 are given as (assuming zero losses)

$$\langle i_{D1} \rangle_{T_s} = \frac{v_s^2}{v_{Cr} R_s} = \frac{\langle p_s(t) \rangle_{T_s}}{v_{Cr}} \quad (23)$$

$$\langle i_{D2} \rangle_{T_s} = \frac{V_0^2}{v_{Cr} R_L} = \frac{\langle p_c(t) \rangle_{T_s}}{v_{Cr}} \quad (24)$$

Using eqs. (20) – (24), the complete averaged circuit model for the proposed single-switch ac-dc converter is attained, and is as shown in Fig. 5 [9], [10].

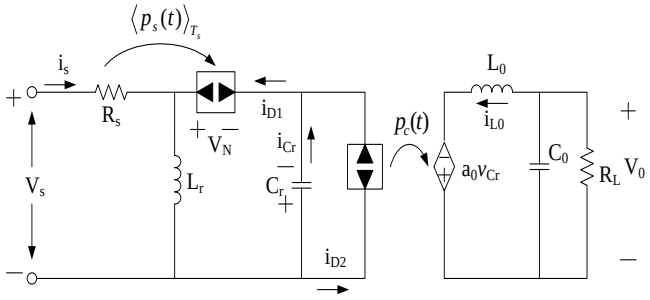

Fig. 5 Averaged model of the proposed converter in DCM

V. RESULTS AND DISCUSSION

The proposed single-switch ac-dc converter is simulated using MATLAB/SIMULINK software. The designed parameters are calculated using above analysis and is given in table-I. The performance of the converter with dynamic analysis is presented for three different cases. For all three cases the converter is working in complete DCM mode only.

A. 20% change in switching frequency (f_s):

In this case, the converter is subjected to 20% step change of switching frequency to its designed value 10 kHz. Fig. 6 shows the supply voltage and current with 10 kHz – 8 kHz step change in frequency.

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It can be observed that the input voltage and currents are in sinusoidal shape with unity power factor. The %THD of line current is also low which is represented in table-II. Fig. 7 represents the output voltage for this case. The settling time (s) and peak overshoot (V) is represented in table-III.

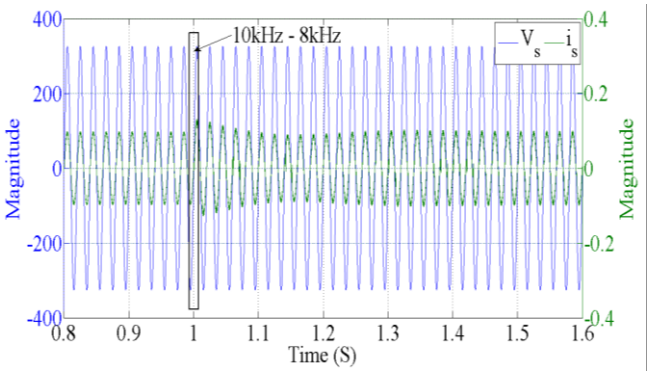

Fig. 6 Supply voltage and current for 10 kHz – 8 kHz step change in frequency

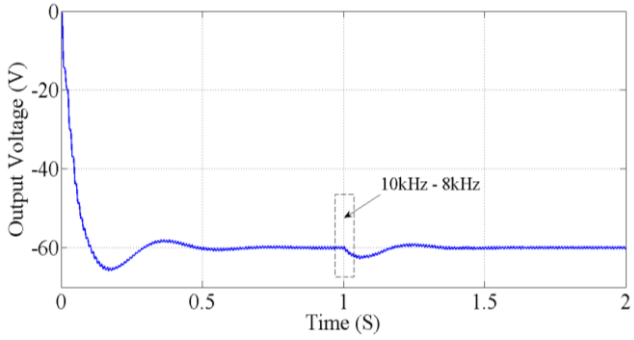

Fig. 7 Output voltage of the converter for 10 kHz – 8 kHz step change in frequency

Table-II
Performance of converter with ±20% frequency
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Switching frequency f_s	Input current i_s (A)	%THD	P.F (%)	V_0	% Ripple	%η
8KHz	0.0666	6.51	100	60	1	94
10KHz	0.0667	2.41	99.9	60	1	94
12KHz	0.0668	1.87	99.9	60	1	93.7

Table-III
Output Response of converter with ±20% frequency
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Switching frequency f_s	Setting time (S)	Peak overshoot (V)
10 - 8 KHz	0.16	2.8
10 KHz	0.44	5.8
10 - 12 KHz	0.16	2.1

Fig. 8 represents the supply voltage and current with 10 kHz – 12 kHz step change in switching frequency. It is observed that the input voltage and currents are sinusoidal and in phase. The %THD of line current is low as given in table-II. Fig. 7 shows the output voltage with step change in frequency. The settling time (s) and peak overshoot (V) is also shown in table-III for this condition.

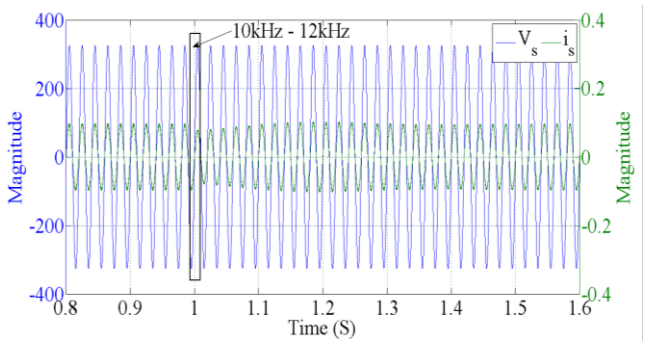

Fig. 8 Supply voltage and current with 10 kHz – 12 kHz step change in frequency

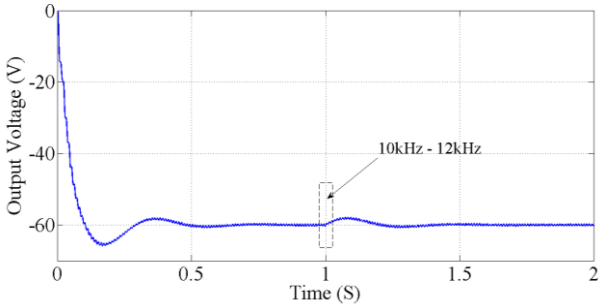

Fig. 9 Output voltage of the converter with 10 kHz – 12 kHz step change in frequency

B. 20% change in supply voltage:

In this case, the converter is operated with 230V – 200V & 230V – 260V step change in supply voltage. Fig. 10 shows the supply voltage and current with 230V – 200V step change in input. It can be noticed that the line current is sinusoidal shape and in phase with voltage. The %THD is also low as represented in table-IV. The performance of the converter with output voltage ripple is also given in table-IV. Fig. 11 represents the output voltage. The settling time (s) and peak overshoot (V) for this case is represented in table-V.

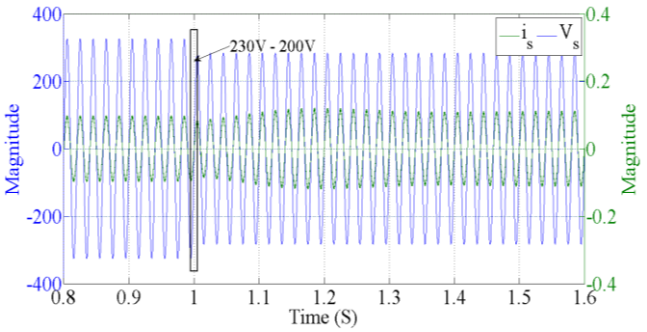

Fig. 10 Supply voltage and current with 230V – 200V step change

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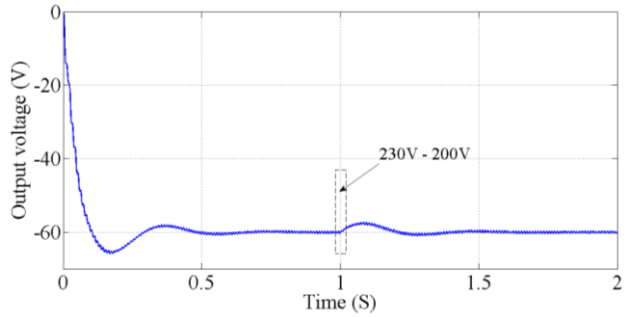

Fig. 11 Output voltage with 230V – 200V step change

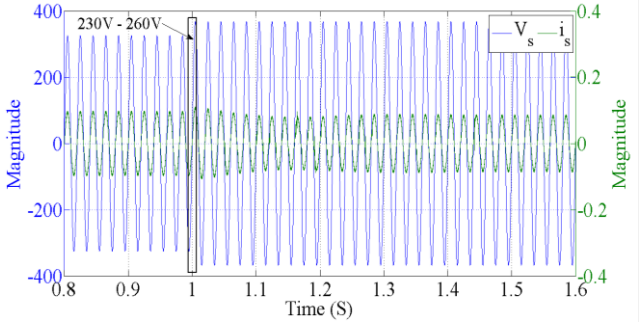

Fig. 12 Supply voltage and line current with 230V – 260V step change

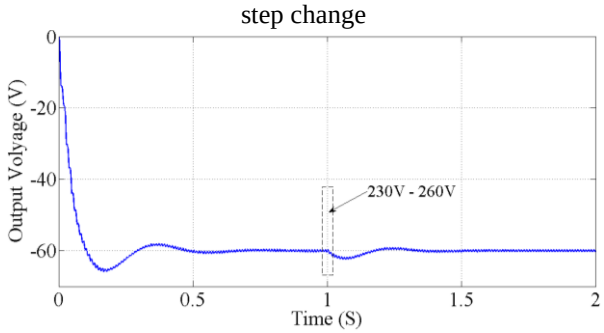

Fig. 13 Output voltage with 230V – 260V step change

Fig. 12 shows the input voltage and current with 230V – 200V step change in supply. The input line current is with less %THD as given in table-II. Fig. 13 shows the output voltage with step change in supply voltage.

Table-IV
Performance of converter with ±20% input
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Input Voltage (V)	Input current I_s (A)	%THD	Input P.F (%)	V_0 (V)	% Ripple	%η
200	0.07658	2.35	100	60	1	94
230	0.06667	2.41	99.96	60	1	94
260	0.05922	2.47	99.89	60	1	93.6

Table-V
Output Response of converter with ±20% input
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Input Voltage (V)	Setting time (S)	Peak overshoot (V)
230 – 200	0.16	2.5
230	0.44	5.8
230 – 260	0.16	2.4

C. 20% change in Load resistance:

In this case the load resistance is changed from 250Ω - 200Ω and 250Ω - 300Ω while all other parameters are kept constant. Fig. 14 and 15 shows the input voltage with current and output dc voltage subjected to 250Ω - 200Ω step change in load. Fig. 16 and 17 represents the input voltage with current and output dc voltage subjected to 250Ω - 300Ω step change. The performance of the converter is represented in table-VI and VII.

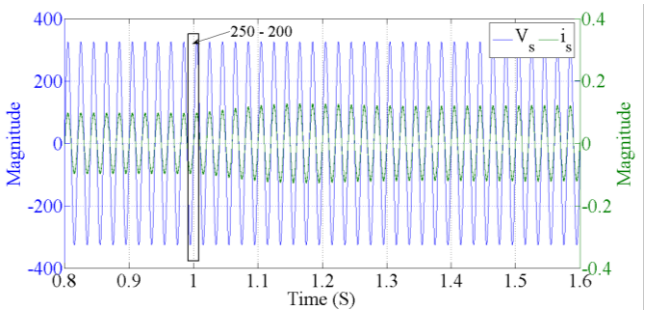

Fig. 14 Supply voltage and input current for 250Ω - 200Ω load change

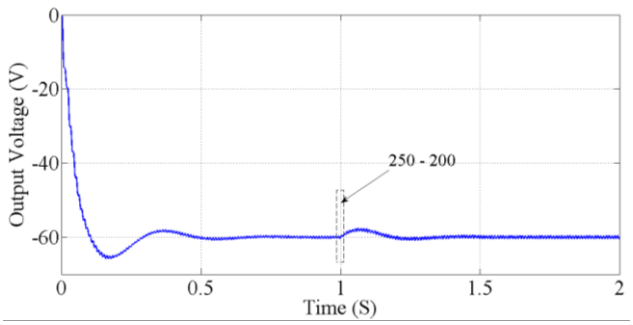

Fig. 15 Output voltage is subjected to step load change 250Ω - 200Ω

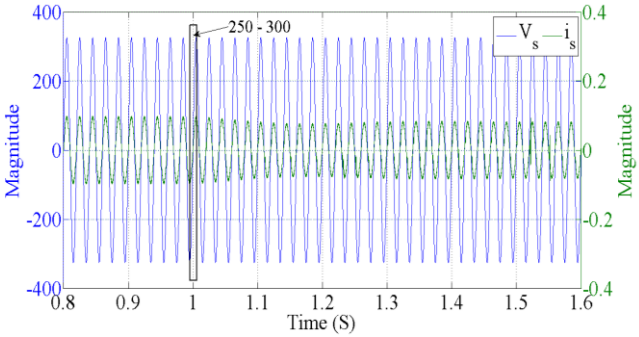

Fig. 16 Supply voltage and input current for 250Ω - 300Ω load change

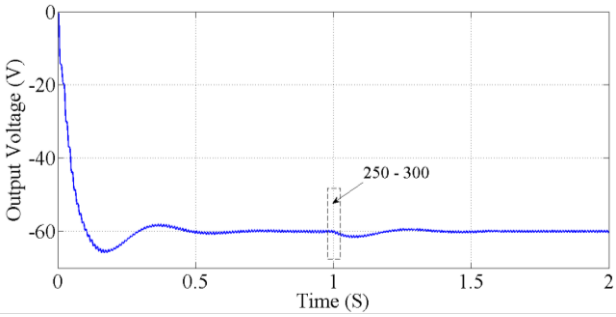

Fig. 17 Output voltage is subjected to step load change 250Ω - 300Ω

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Table-VI
Performance of converter with ±20% load
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Load (Ω)	Input current I_s (A)	%THD	Input P.F (%)	V_0 (V)	% Ripple	%η
200	0.08325	2.3	100	60	1.3	94.2
250	0.06667	2.41	99.96	60	1	94
300	0.05595	7.04	99.96	60	0.8	93.5

Table-VII
Response of converter with ±20% load
(V_{0ref} = 60V, P = 0.004, I = 0.25)

Load (Ω)	Setting time (S)	Peak overshoot (V)
250 – 200	0.16	2.2
250	0.44	5.8
250 – 300	0.16	1.7

VI. CONCLUSION

In this paper, the dynamic analysis of proposed single switch ac-dc buck-boost buck converter is examined for three cases. The proposed converter is an integrated converter connected to ac supply via centre tapped transformer based full-wave rectifier. The input inductor L_r is designed for DCM operation to attain unity power factor at input. To reduce the bus capacitor C_r size, the output inductor L_0 is also operated in DCM. Detailed analysis is performed and modeling equations are derived for the proposed converter.

A PI controller is designed based on the modeling equations. The proposed converter is simulated in MATLAB for 60V reference voltage. Results are shown for step change in switching frequency, input supply and load. Performance tables are given for the above conditions to show capability of the converter. From all the results, it can be concluded the proposed converter has shown better performance under these operating conditions.

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