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FPGA Based Convolutional Encoder for GSM-900 Architecture

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Abstract*: This paper presents one of the most popular current techniques of enhancing the reliability, accuracy and security in data communication systems i.e., error-correcting codes such as convolutional codes. To correct and decode the errors that occur during data transmission on communication channels by introducing some redundancy in their encoding. In advanced wireless communication, reliability and accuracy are two main constraints of hand held devices such as mobile phones. Now a days, mobile phones uses wireless standards such as Code Division Multiple Access (CDMA), Global System for Mobile Communication (GSM) for communication purpose. Apart from above constraints quality of service and security are highly desirable. The proposed architecture implemented for convolutional encoder GSM-900 by using XOR free approach methodology with a required constraint length (K=5) and a data transmission code rate (R=1/2) using Xilinx 14.7 ISE software. The convolutional encoder for GSM-900 architecture verified on Nexys2 1200E Field Programmable Gate Array (FPGA).

***Index Terms*: Convolution Encoder, Error Control Codes, Field Programmable Devices (FPGA) and Global System for Mobile Communication (GSM), Linear Feedback Shift Register (LFSR) and XOR free approach.**

I. INTRODUCTION

In coding techniques, the message is increased due to encoding of symbols. In order to facilitate there are two basic demands at the receiver one is Error detection and other hand is error correction. Error detection and correction mechanisms are plays a major role and various techniques are involved in communication system. Current days, two major techniques are used such as Automatic Repeat Request (ARQ) and Forward Error Correction (FEC).The ARQ method only detects the errors introduced by the channel at the receiver side. Various ARQ techniques are available. It requires a return channel and it is not useful because delay cannot be considered or tolerated in communication purpose, whereas FEC does not requires a return channel and it is not affected by the propagation delay. In FEC, the encoded data can detect and correct the errors. This development mainly focus on FEC techniques. FEC codes are most significant for wireless communication standards which depend on various code families such as Reed– Solomon, convolution codes (counting Turbo codes), and low-density parity check (LDPC) codes. A few principles apply different codes, either in a fell/connected way or by determining a specific code family for various coherent channels [1].

FEC is an error control method for data transmission by adding redundant data to its messages to improve the capacity of a channel. This redundant data allows the receiver to detect and correct a certain number of errors without requesting the encoder to re-transmit more additional data. Channel coding is the process of adding this redundant information. There are two major types of channel coding: block codes and convolutional codes. Block codes have a fixed length of vectors. It consists of two integers (k, n) and generator polynomial. The most widely used block codes are hamming codes and cyclic redundancy check (CRC). Whereas convolutional codes are more efficient and easy than compare to block codes. The most widely used convolutional codes are convolutional encoder and turbo encoder. FEC techniques are involved in various communication applications such as deep space, satellite communication, broadcast, storage systems, wireless and tele communication applications. Data transmission reliability and quality of service are two main constraint requirements of modern third generation partnership projects such as 3GPP and 3GPP2 wireless standards such as CDMA and GSM [2].

To implement novelty and cost effective FEC codes are satisfy these requirements for the mobile devices. CDMA coordinate extremely well with channel coding utilizing FEC techniques. In fact, all CDMA systems using FEC method [3].

The convolutional codes are mostly preferred than compare block codes due to its decoding capability and higher coding gain. The convolutional codes mainly depends on its constraint length (K) and code rate (R=1/2). The basic convolution operation is multiplication, which is implemented by using shifting and addition operation. The multiple and addition operations can consumes a significant amount of power and increase the complexity. The main concentrate in the convolutional encoder design is to minimize the complexities by reducing the number of logical operators. To eliminate bit pattern for optimize the XOR gates count by using the Common subexpression elimination (CSE) method [4].

This paper presents the XOR free approach based convolutional encoder for GSM -900 architecture with constraint length K=5 and code rate R=1/2 is implemented using Xilinx ISE 14.7 software and verified on Nexys2 1200E FPGA technology.

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The rest of the paper is organized as follows. Section II provides Motivation of the Paper. Section III provides Literature Review. Section IV provides convolutional Codes. Section V provides convolutional Encoder. Section VI provides the Methodology for XOR free approach. Section VII provides Results and Discussion. Section VIII provides concludes the Paper.

II. MOTIVATION

Digital communications are used to transform the information (message) between sender to receiver during this process various errors can affect the transmitted signals. It is necessary to control the errors by using error control coding techniques. The cost effective and innovative FEC codes are developed for wireless communication applications. The errors can control by using convolutional technique. Convolutional codes can do both error detection and correction. Now a days, convolutional codes have turned out to be increasingly more essential in digital transmission. Convolutional codes with Viterbi decoding is utilized in various applications such as wireless communications, Telecommunications, remote and satellite communications. The different models of wireless standards such as GSM IS-54, IS-95 CDMA standards.

III. LITERATURE REVIEW

In 2008, John Dielissen et.al. [1] Proposed a work depend on the compression of the era of mobile terminal of real-time support of various transmission standards such as FEC and ARQ. The FEC has capability to decoding functionality is including in some of these standards. Due to the need of handy and fast processing area reduction and low power consuming devices are widely used in current days.

In 2016, G. Purohit, et.al. [2] Proposed a work on new algorithm to develop a XOR-Free approach of an effective convolutional encoder. Here main focus is optimization XOR gate operation while executing polynomials over GF (2) that consumes a lot of dynamic power. The proposed methodology totally eliminates of the XOR processing operation of a selected non-systematic, feed-forward generator polynomial and reduces the logical operators, thereby the encoding value. The Hardware co-simulation of the design is first approved and after that actualized with Xilinx Vertex-V FPGA. By using this methodology to reduces the standard polynomial into a ROM and ease to implement on FPGA. The architecture can be effectively tested for 3GPP and 3GPP2 wireless models such as CDMA and GSM.

In 1996, Joachim Hagenauer et.al. [3] Proposed work depend on the strategy or principle is Spread spectrum systems, (FEC) methods is applied in specially code division multiple access systems (CDMA). In fact, almost all CDMA systems utilize the other way of FEC. CDMA or FEC system viewed and schemes with inner and outer decoding. And how such a system can be improved by using a soft in or soft out decoder which passes a soft decision from the inner to the outer decoder. Further enhancement can be obtained by using another soft in or soft out decoder.

In 1999, R. Pasko et.al. [4] Proposed a method based on an effective hardware implementation of multiplications with one or more constant is faced in different digital signal-processing areas, such as reflection dispensation or digital filter optimization is a problem. The solution of this is to design the circuit with low power using common CSE method. Hence targeting on the parameters like area and power efficient of hardware implementation on FPGA.

In 1971, A.J. Viterbi et.al. [5] Proposed a work on, numerous applications such as telephonic conversations that require communication in which the messages are encoded into the communication channel and then decoding it at the receiver end. When message transferring, the data may get corrupted due to noise in the communication channel. Hence, the decoder have ability of correcting the error. Viterbi algorithm has got numerous applications because of its error detection and correction. Convolution encoding with Viterbi decoding is a best way for forward error correction. Because of the limited capacity of the communication channels. It has been broadly deployed in many wireless communication systems.

In 1999, Y.Yibin et.al. [6] Proposed a work is on XOR gates which has several advantages in modern circuit design such as small in size and good testability. The power consumption in XOR dominated circuits and evaluate such designs with general AND/OR logic. The suitability of using various delay models like fan-out delay, unit delay and random delay in XOR dominated logic. The internal node capacitances is also considered as the Power losses because of charging and discharging of capacitance.

IV. CONVOLUTIONAL CODES

In 1955, the convolutional codes were introduced by Elias. Convolution coding is a popular error correcting coding technique can be used to enhance reliability of communication system. These codes are vary from block codes, which can deal with fixed length blocks of code whereas convolutional codes can deal with data sequentially. In Block codes, the length of the block increases it become very complex and hence harder to implement. Convolutional codes are easy to implement and less complex then compare to block codes [5], [12].

The convolutional codes can map the information bits to code bits, sequentially convolve the sequence of information bit according to some standard rule. Convolutional codes are continuous data stream as well as to blocks of data whereas the block codes can be applied only for the block of data. Thus the convolutional codes requires very little buffering and storage hardware than compare to block codes. Convolutional codes are mostly used in digital communications hence it is popular error correcting method. Convolutional coding can be utilized to enhance the reliability of communication system. To decipher convolutional codes for Viterbi decoders are mostly utilized. It is very popular method and robust. For excellent error control performance the convolutional encoder and Viterbi decoder are mostly used in communication systems.

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V. CONVOLUTIONAL ENCODER

Convolutional encoder is one of the FEC coding method. It is a sequential circuit like mealy machine, where the output is obtained from the elements of present state and the present input information (such as past outputs). It can be formed one or more shift registers (DFF) and various XOR gates. Thus, it is called as Convolutional encoder [9], [10].

The XOR gates are combined with the shift registers and addition to the present input information then it results to produce the output polynomials. The convolutional encoder can be commonly specified by three parameters (x, y, K) which are as follow:

x= Number of input bits.
y= Number of output bits.
Constraint Length: K= (M + l) digits.
M = Number of stages of shift register.
l = Number of bits in a message sequence.
Code Rate: R = y/ x.
The important key terms can be defined here.

Code Rate (R): Code rate is defined as the Ratio of the number of input bits to the number of output bits. For example, code rate is 1/2 which means there are two output bits for each input bit.

Constraint length (K): It determines the length of the Encoder. The number of delay elements in the convolutional coding for example with K = 3, there are two delaying elements.

Generator polynomial (g): Wiring of the input sequence with the delay elements to form the output. For example, the generator polynomial is considered as g [3, 1]8 = [011,001]2.

The encoder maps information bits to be encoded sequentially and convolved depending on some rule. It is realized in Galois Field (GF) in which multiplication and addition is represented in modulo-2 (XOR) operation. The convolutional encoder with constraint length K=3 and code rate R=1/2 is as shown in Fig. 1.

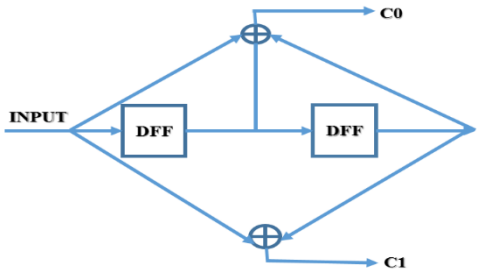

Fig. 1 Convolutional encoder with constraint length K=3 and code rate R=1/2

The Fig.1 shows the convolutional encoder with constraint length (K) =3 and code rate (l) =1/2 produces two bits of encoded output data for single bit of input data, so it is referred as a code rate (R=1/2). Generally the code rate is represented as y/x, here y is represented as a number of outputs of the encoder, x is number of inputs of the encoder, and M is number of shift registers. The number of input data values used to generate the code is called the constraint length. Here the input bit enters into the encoder at every clock cycle and previous value of the shift register stages sequentially. The encoded output is obtained from the generator polynomial and the denominator of the code rate. This coding method is mostly utilized in various fields like space communications, wireless, Tele communications and digital communications.

Convolutional encoder can be represented in various models in digital communications. The various convolutional encoder representations can be expressed as

i. State diagram
ii. Trellis diagram
iii. Tree diagram

A. Convolutional Encoder for GSM-900 Architecture

The convolutional encoder is a sequential circuit which can be represented as final state machines (FSM) like Mealy or Moore machine states [14].To optimize the sequential circuit use various approaches. It is realized in Galois Field (GF) in which multiplication and addition is represented in modulo-2 adder operation. The Fig. 2 shows the conventional convolutional encoder for GSM-900 architecture with constraint length K=5 and code rate R=1/2. To generate the output, the encoder uses 5 values of the input signal (1 present input bit and 4 previous input bits). The number of shift registers has memory elements utilizing four i.e. (K-1). The output of each set of is produced by XOR operation and shifted values of input data. In conventional convolutional encoder XOR (Modulo-2 adders) gates plays major gates. Various XOR-based synthesis styles have been introduced over the most recent couple of years, in this paper we examined the modeling of power consumption of XOR dominated circuits [6]. Due to various possible implementations styles for XOR gates, we consider XOR gates as basic gates as well as complex gates. For large circuits size can be significantly decreased by utilizing XOR-based synthesis techniques. Basically XOR gates are considered as basic gates, which are implemented as complex static CMOS gates, the power consumption is more. Power consumption due to charging and discharging of internal node capacitances in complex XOR gates is significant [7]. The conventional convolutional encoder for GSM-900 architecture having generator polynomials g0=31 and g1=33 can be realized with XOR gates (Modulo-2 adders) and shift registers with Constraint length K=5and code rate R=1/2 is shown in Fig. 2.

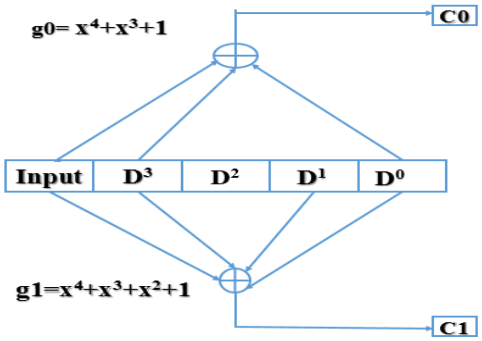

Fig. 2 Convolutional encoder for GSM-900 with Constraint length K=5and code rate R=1/2

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VI. XOR FREE APPROACH METHODOLOGY

XOR gates have more switching probability then compare to common logic gates like AND, OR gates. To overcome this problem, XOR free approach methodology is used. The XOR free approach based convolutional encoder for GSM-900 architecture with constraint length K=5 and code rate R=1/2 is consists of three building blocks such as

i. Selection of MUX logic
ii. XOR free MUX and
iii. ROM memory.

Verilog coding for MUX logic, XOR free MUX and ROM memory are written in Verilog and simulated using Xilinx ISE 14.7 software and implemented on Nexys2 1200E FPGA board.

The XOR free approach is better approach then compare to conventional approach of convolutional encoder. This approach reduces the hardware complexity and power consumption is also reduced. The flow chart for XOR Free Approach Methodology based convolutional encoder for GSM-900 architecture [2], [8].

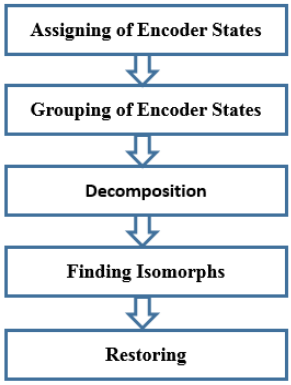

Fig. 3 The Flow chart for XOR free approach based convolutional encoder

The Fig. 3 shows the flow chart for XOR free approach methodology for convolutional encoder GSM-900 architecture. It follows five steps such as assigning of encoder states, grouping of encoder states, decomposition, finding isomorphs and restoring.

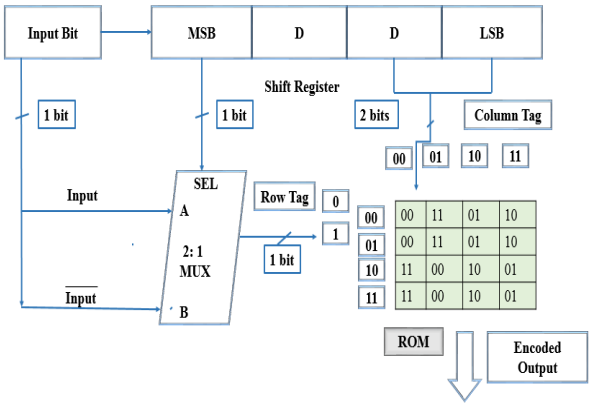

Fig. 4 XOR free approach based convolutional encoder for GSM-900 architecture

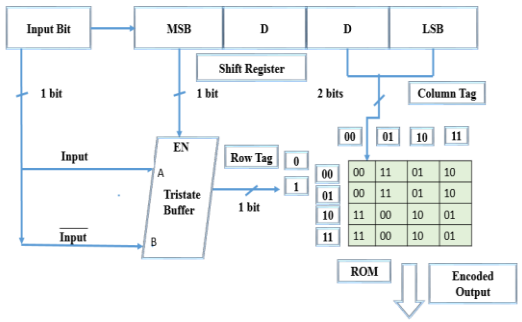

Fig. 5 The proposed XOR free approach based Convolutional encoder for GSM-900 architecture

The Fig.4 shows XOR free approach based convolutional encoder for GSM-900 architecture with constraint length K=5and code rate R=1/2. Here 2:1 mux is used. The proposed XOR free approach based convolutional encoder for GSM-900 architecture with constraint length K=5and code rate R=1/2 is designed using tristate buffer. The proposed architecture replace the multiplexer (2:1 Mux) with Tristate buffer is shown in Fig. 5. The process of XOR free approach based convolution encoder architecture consists of following the five steps. The steps are explained here.

i. Assigning of Encoder States
ii. Grouping of Encoder States
iii. Decomposition
iv. Finding Isomorphs
v. Restoring

Step 1: Assigning of Encoder States

To assign the input bit as logic "0" for all encoder states, the next encoder state can be obtained from the previous encoder state incremented by one. The output response can be computed by using normal convolutional encoder process is shown in Table. I.

Table. I Convolved output for input bit as Logic 0

Input Bit	D3	D2	D1	D0	C0	C1
0	0	0	0	0	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	1
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	0	0	0	1	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	1

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Step 2: Grouping of Encoder States

The encoder states can be grouped based on their same encoded output with all possible combination of values such as {00, 01, 10, and 11} is shown in Table. II.

Table. II Convolved output for grouping of encoder states

Input Bit	D3	D2	D1	D0	C0	C1
0	0	0	0	0	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	1
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	0	0	0	1	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	1

Step 3: Decomposition

The assignment of encoder state bits can be splits into two subparts for state representation. The first part as a row tag (RT) and second part as a column tag (CT) [15], [16].

To obtain the row tag (RT) and column tag (CT) using the formulas as follows

- Colum Tag (CT) = $k-1$
- Row Tag (RT) = $[K-\{CT+1\}]$

Here RT as most significant bits and CT as the least significant bits is shown in Table. III.

Table. III Decomposition of row tag and column tag

ROW TAG	COLUMN TAG			
	00	01	10	11
00	00	11	01	10
01	00	11	01	10
10	11	00	10	01
11	11	00	10	01

Step 4: Finding Isomorphs

To find the isomorph RT pairs which have same encoded output bits with respect to the CT and connected them and result in similar parity bits is shown in Table IV. To create an array like ROM function. Simply it can be obtained by similar encoder states and outputs is said to be Isomorphs.

Table. IV Finding Isomorphs

S.NO	ROW TAG	COLUMN TAG
1	0	000,001,110,111
2	1	010,011,100,101

Step 5: Register Allocation

The overall functionality can be obtained by applying input bit as Logic "0" as well as Logic "1," the even and odd parity concepts are utilized and then the output is flipped is shown in Table. V. Registers can be used to store the data and accumulated for each clock cycle. The outputs can be stored in corresponding memory shift registers.

Table. V Formation of ROM Array Function

RT	CT			
	00	01	10	11
0	00	11	01	10
1	11	00	10	01

VII. RESULTS AND DISSCUSIONS

The XOR free approach based convolutional encoder is implemented using D-FF, T-FF and LFSR. The proposed design reduces the hardware complexity. The individual modules designed in Verilog HDL. The design is synthesized in Xilinx ISE 14.7 and verified on Nexys2 1200E FPGA. The synthesis and simulation results reports are presented.

A. Implementation of Convolutional Encoder GSM-900 Architecture Using D-FF

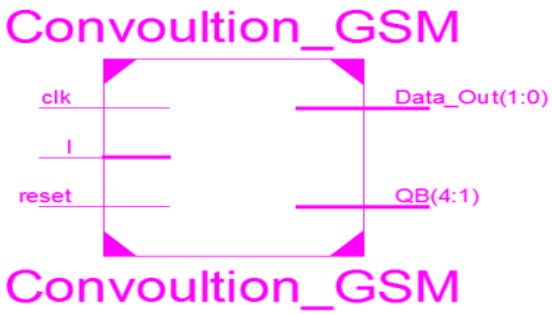

Fig. 6 Block diagram of convolutional encoder for GSM-900 using D- FF

Here Fig.6 shows block diagram of convolutional encoder for GSM-900 architecture. It produces the outputs based on given inputs such as clk, reset along with input (I) to obtain the convolutional encoder output. Here the input bit is always 0. The simulation results of convolutional encoder for GSM-900 using D- FF is shown in Fig. 8.

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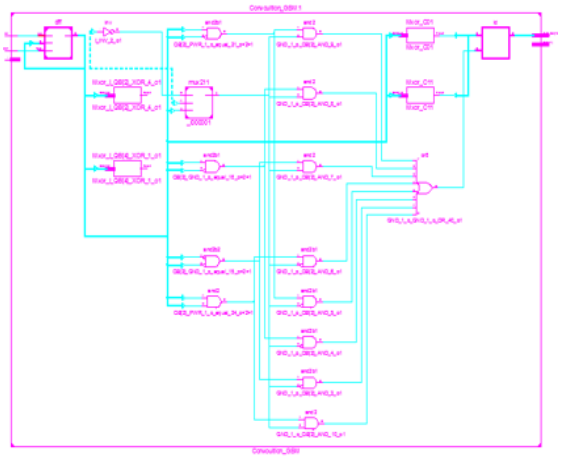

Fig. 7 Implementation of Convolutional encoder for GSM-900 using D- FF

The Fig.7 shows the implementation of convolutional encoder for GSM-900 architecture using D-FF. The internal circuit diagram consists of input, shift registers, tristate buffer and ROM.

The Fig.8 shows the simulation results of XOR free approach based convolutional encoder using D-FF with constraint length K=5, code rate R=1/2 and generator polynomial is g0=31 ,g1=33. In this the encoded states are generated from 0000 to 1111 and produces the output as c0 and c1 when input bit is 0 .The for example the encoding state q= 0100 and input=0 then it produces the output c0 =0 and c1=0 i.e. 00 is as shown in above Fig.. Similarly for all possible states from 0000 to 1111 it produce the outputs.

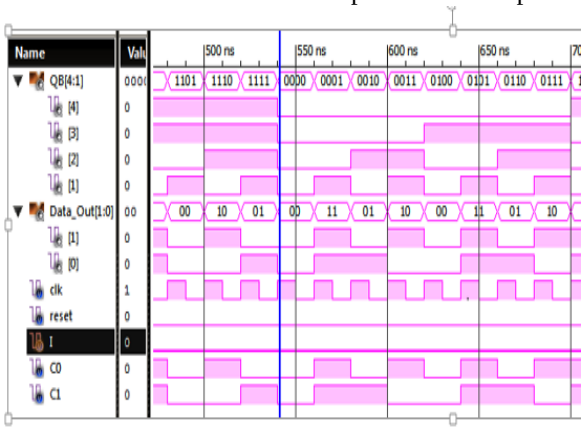

Fig.8 Simulation results of convolutional encoder for GSM-900 using D- FF

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	2	53200	0%
Number of fully used LUT-FF pairs	0	2	0%
Number of bonded IOBs	13	200	6%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig.9 Utilization summary for D- FF

The Fig.9 shows the device utilization summary for D-FF for using XOR free approach based convolutional encoder with constraint length K=5, code rate R=1/2.
LUT (Look up Table) =2/53200 are used
Number of Fully LUT-FF pairs=0/1 used
Number of IOBs =13/200 are consumed.

B. Implementation of Convolutional Encoder GSM-900 Architecture Using T-FF

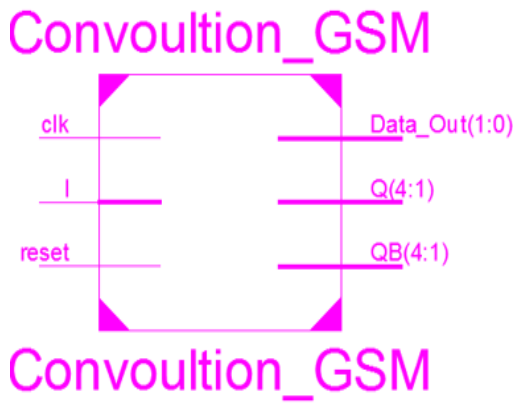

Fig.10 Block diagram of Convolutional encoder for GSM-900 using T- FF

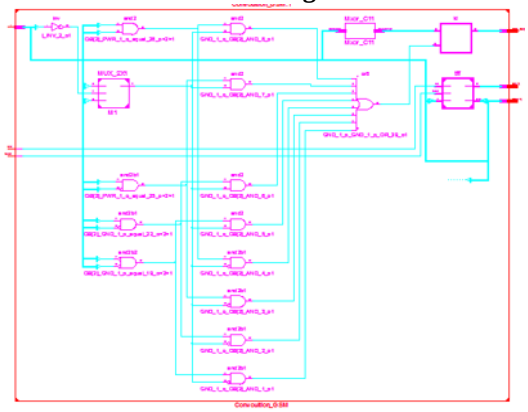

Fig.11 Implementation of convolutional encoder for GSM-900 using T- FF

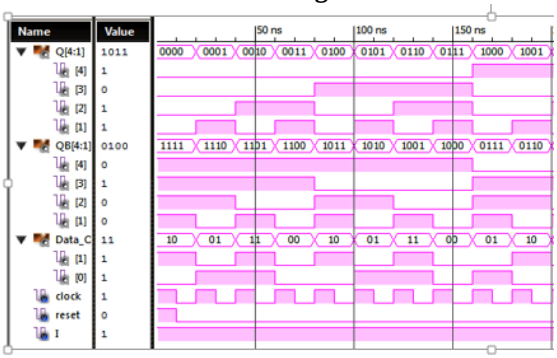

Fig.12 Simulation results of convolutional encoder for GSM-900 using T- FF

The Fig.12 shows the simulation results of XOR free approach based convolutional encoder using T-FF with constraint length K=5, code rate R=1/2 and generator polynomial is g0=31 ,g1=33. In this the encoded states are generated from 0000 to 1111 and produces the output as c0 and c1 when input bit is 1.The encoding state q= 1111 then it produces the output c0 =1 and c1=0 i.e. 10 is as shown in above Fig.12 .Similarly for all possible states from 0000 to 1111 it produce the outputs.

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In this the encoded states are generated when input bit is 1. It is implemented on hardware there is no need for initialization. Thus it will reduces some hardware resources than compare to using D-FF. The Device utilization summary is also shown in Fig.13.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1	53200	0%
Number of fully used LUT-FF pairs	0	1	0%
Number of bonded IOBs	11	200	5%

Fig.13 Utilization summary for T- FF

The Fig.13 shows the device utilization summary using T-FF for implementing the XOR free approach based convolutional encoder with constraint length K=5, code rate R=1/2 and generator polynomial is g0=31 ,g1=33.
LUT (Look up Table) =1/53200 are used
Number of Fully LUT-FF pairs=0/1 used
Number of IOBs =11/200 are used

C. Implementation of Convolutional Encoder GSM-900 Architecture Using LFSR

Linear feedback shift register (LFSR) is a shift register which generates the sequence of binary values. The sequences are repeated after specific elements and it regains the original value, it is known as pseudo random sequence. LFSR structure consists of shift registers and exclusive –or/ exclusive nor gates. Shift registers are cascade of flip flops. Flip flops are basic building blocks of LFSR.
Generally LFSR structure can be realization in two methods, one is Fibonacci LFSR configuration and Galois LFSR configuration. The convolutional encoder for GSM-900 architecture is realized in Galois Filed (GF). The design implementation of convolutional encoder for GSM-900 architecture is shown in Fig.14.

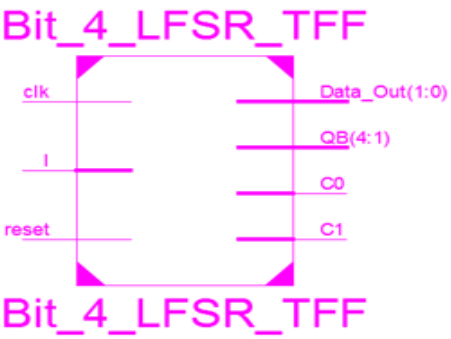

Fig.14 Block diagram of Convolutional encoder for GSM-900 using LFSR

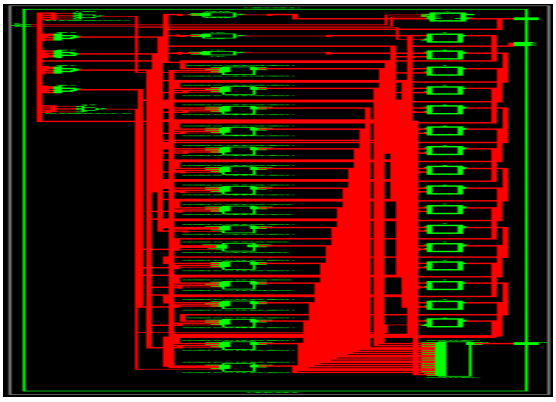

Fig.15 Implementation of convolutional encoder for GSM-900 using LFSR

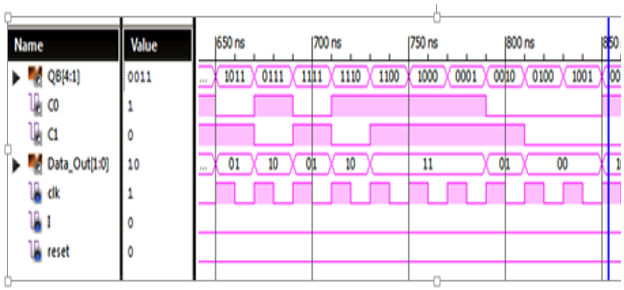

Fig.16 Simulation results of convolutional encoder for GSM-900 using LFSR

The Fig.16 shows the simulation results of XOR free approach based convolutional encoder using T-FF with constraint length K=5, code rate R=1/2 and generator polynomial is g0=31 ,g1=33. The Device utilization summary is also shown in Fig.17.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1	53200	0%
Number of fully used LUT-FF pairs	0	1	0%
Number of bonded IOBs	7	200	3%

Fig.17 Utilization summary for LFSR

The Fig. 17 shows the device utilization summary using T-FF for implementing the XOR free approach based convolutional encoder with constraint length K=5, code rate R=1/2 and generator polynomial is g0=31 ,g1=33.
LUT (Look up Table) =1/53200 are used
Number of Fully LUT-FF pairs=0/1 used
Number of IOBs =7/200 are used.

Logic Utilization	**D-FF**	**T-FF**	**LFSR**
Number of Slice LUTs	**2**	**1**	**1**
Number of LUT-FF pairs	**0**	**0**	**0**
Number of IOBs	**9**	**11**	**7**

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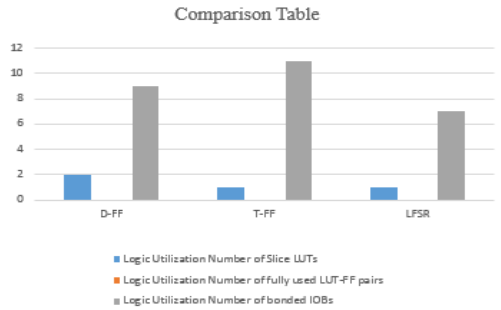

Fig.18 Comparison table for D-FF, T- FF and LFSR

D. Field Programmable Gate Array

Current FPGA has abilities in the zone of run-time reconfiguration to meet the needs of wireless communications applications, telecommunication and satellite communication applications. Generally FPGAs are pre-manufactured silicon devices that can be electrically customized to become almost any kind of digital circuit or system. FPGAs has programmable logic components called "logic blocks", and a hierarchy order of reconfigurable interconnects that enable the blocks to be "wired together" to seems like a one-chip programmable breadboard. Logic blocks can be designed to perform complex combinational functions, simple logic gates like AND, OR and XOR. The implementation of Convolutional Encoder GSM-900 Architecture on FPGA is as shown in Fig.19.

Fig.19 FPGA implementation of convolutional encoder for GSM-900 Architecture

The the XOR free approach based convolutional encoder with constraint length K=5, code rate R=1/2 and generator polynomial (g0=31, g1=33) is implemented.

Fig. 20 FPGA implementation of convolutional encoder for GSM-900 architecture

The the Fig.20 shows implementation of convolutional encoder for GSM-900 architecture on reconfigurable hardware i.e, FPGA. Here , the input bit as 0 and encoded state is 1000 (8) then the output is produced as c0=1 and c1=1 i.e. is 11 for a given polynomial is g0=33 and g1=33 using XOR free approach. Similarly it will produces the outputs for all the encoded states (0000 to 1111). Hence, based on polynomial it will produces outputs.FPGA has ability to configure the polynomial and produce the outputs.

VIII. CONCLUSION AND FUTURE WORK

In this paper, the proposed approach is implemented on Nexys2 1200E FPGA for XOR free approach based convolutional encoder GSM-900 architecture with constraint length K=5 and code rate R=1/2. It is implemented with D-FF, T-FF and LFSR.

In this XOR free approach method the mux replaces with tristate buffer, thus it reduces some hardware resources for T-FF when compare to D-FF. The entire architecture has been designed by XILINX ISE 14.7 synthesis and simulation with Verilog HDL for the constraint length of K=5 and code rate R=½ implemented and verified on FPGA. Communications are widely used in huge no of various applications such as Radar, aerospace, under water maritime or naval communication and mobile communication. Convolutional encoder plays a major role in the field of telecommunication and wireless communication applications. Convolutional codes are mostly used in deep space communications and wireless communications applications. In future the convolutional encoder can be implemented for high constraint length and configure the polynomial in runtime.

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