International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-8 Issue-4, February 2019

T-NOT Gate : A Novel Circuit based on Ternary Logic

Amit Verma, Manish Prateek

Abstract: ***In this paper a novel circuit for the t-NOT gate is proposed using op-amp 741 IC and the basis AND and OR binary gate. Proposed circuit is based on the concept of ternary logic, where the term ternary means three logic that is 0, 1 and 2 instead of traditional two logic 0,1 (binary). As the ternary logic can be the altenate for the radix 2 that is binary logic to reduce the transition delay, enhance the processing speed, reduce the memory requirement, reduce circuit complexity and number of electronic components The truth table, symbol and state transition diagram is also presented in the paper. Which show that t-NOT gate is a unary gate that takes single input and provide the next immediate logic in clockwise cyclic direction as the output as shown in the state transition diagram mention in the paper. Further the standard working of op-amp 741 IC is discussed, the actual voltmeter reading for various input voltages greater than the upper limit +V_{CC} is presented in tabular format. Simulation of the binary AND and OR gate is carried out using proteus to prove that the current binary AND, OR gate can be used as MIN and MAX gate for logic circuits of higher radix. Here the MIN and MAX logic means the gate giving the minimum and maximum voltage as the output voltage among the various input voltages.***

Index Terms: op-amp 741 IC, ternary, multi-valued logic.

I. INTRODUCTION

Now a day MVL is attracting the interest of many researchers as MVL is having considerable advantages over current binary system. Current binary circuitry require large number(plentiful) of electronic components [1], interconnection overhead [2], [3], [4], [5], [6], [7] and large chip area[8], [7], [9]. MVL can be considered as increasing number of states in the current logic, which can be ternary or fuzzy. Here ternary means having three state machine instead of two (0/1) and according to multiple research references fuzzy [10], [11], [12], [13] is considered as infinite states logic. However, fuzzy logic should be consider as a machine working with decimal logic or base 10. As base 10 machine can be considered as the saturated machine in terms of computational speed, as all the computations can be done in base 10 that is set of numbers from 0 9. So increasing base/radix further will be repetitive and useless. And the term ternary can be defined as adding one more state to the current binary logic that is to increase radix to 3, third state considered as unknown or uncertain state [14], [15], [16], [17], [5], [18]. And third state is also consider as suitable for treating the ambiguity, sometimes it is difficult to find the logical state like transition state or initial state of circuit [19], [5]. As in some cases, it become impossible to define the state of machine in two logic that is YES/NO or 0/1, in that case it is uncertain to find the state of machine. So, this uncertain state is considered as third state [19].

Many efforts has been made my numerous researchers to provide the circuits based on MVL when the advantages of MVL over 2-state logic appears. Still there has not been developed any widely used system based on even ternary logic. MVL circuit can be categorized into two type that is v-MVL or i-MVL, here v-MVL and i-MVL representing voltage and current mode Multi-valued Logical circuits [20], [21], [8], [4]. Multiple current and voltage based circuits have been given in past 20 years for the implementation of ternary logic using complementary metal-oxide semiconductor (CMOS) transistors and carbon nanotube FETs. Almost every author, who proposed any arithmetic circuit based ternary logic has discussed about the circuit of ternary inverter and consider it as basic building block of any circuit based on ternary logic [22], [23], [7], [24]. And ternary inverter broadly classify into three unary inverters that are simple ternary inverter (STI), positive ternary inverter (PTI) and negative ternary inverter (NTI) based on MOS transistors. Multiple designs of ternary adders has been proposed based on CMOS [22], [24], [25], MOSFETs[7] and CNTFETs[20], [26] in last three decades. In this paper, a circuitry of ternary NOT gate (t-NOT) is proposed using op-amp 741 IC and basic binary to remove the overhead of three different inverter circuits namely simple ternary inverter (STI), positive ternary inverter (PTI) and negative ternary inverter (NTI). The proposed circuitry of t-NOT gate can be use as a basic building block of many circuits based on ternary logic or even higher radix. The use of higher resistance and variable resistance circuits is avoided. Working of op-amp 741 IC is described and checked using real time data in laboratory with different voltages in different condition, other than the standard working of op-amp 741 IC. Simulation of binary AND and OR gate is done using proteus to prove the functionality of gates is to return the minimum and the maximum of the supplied voltages respectively. The rest of the paper is organized as follows: Related work is discussed in Section II. Section III describes the circuitry of proposed t-NOT gate and the working of op-amp 741 IC in different conditions other then there standard working. Section IV presents the results. Finally, we conclude in Section V.

Manuscript published on 28 February 2019.
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II. RELATED WORK

In this section, we discuss major application of ternary logic proposed so far. Mainly the use of ternary logic in treating ambiguity, proposed circuits of basic logic gates and arithmetic using MOS, CMOS and CNTFETs.

Ternary Invertor Circuits

In [27] simple ternary inverter (STI) , positive ternary inverter (PTI), negative ternary inverter (NTI), forward diode (FD)and reverse diode (RD) considered as basic unary op-erators. Ternary inverters are considered as the basic circuit for building other ternary logic gates. Ternary inverter circuit is presented using COS/MOS by inserting resistors between the two complementary type transistors with common drain, one input and three output representing three level of voltage (negative, zero and positive). The ternary inverter circuit realized as combination of three types of ternary inverters. FD and RD, simple diode with shunt resistance. Mouftah et al. [28] proposed the circuit for simple ternary inverter (STI) , positive ternary inverter (PTI) and negative ternary inverter (NTI) using two opposite MOS transistors (p-type and n-type) with common drain and one resistor. The load resistor is connected at the output with the fixed voltage and according to the voltage circuit behave either STI, PTI or NTI. Balla et al. [7] have proposed general ternary inverter (GTI) based on the same concept of three different inverter circuits namely simple ternary inverter (STI) , positive ternary inverter (PTI) and negative ternary inverter (NTI) using MOS transistors. And compared with proposed inverter circuits [29], [30], [28] showing the advantage of reduction in power dissipation with proposed alternative circuit of simple ternary inverter (STI). Heung et al. [22] have proposed circuit for STI, NTI and PTI to further reduce the power consumption and increase the speed of circuit using both enhancement and depletion MOS transistor (DECMOS [31]) without using any resister. The work has been compared for power consumption with the inverter circuits [28], [32]. Mouftah et al. [30], [29], [33] have taken +4V, 0V and -4V as high, middle and low level to represent three different levels of voltage to represent 3-states of ternary logic. Proposed the design on ternary operators (inverter, NAND ad NOR) based on MOS transistors. Inverter circuits is considered as the build-ing block of other ternary logic gates, which actually consist of three different inverter namely simple ternary inverter (STI), negative ternary inverter (NTI) and positive ternary inverter (PTI). On the basis of ternary inverter proposed the cheaper circuit of already proposed [34] Jk arithmetic and T-gate. In [4] discuss the benefits of higher radix that is MVL over binary logic. Mention that the circuit based on the MVL require less wiring complexity and large reduction in the inter-connections [35]. MVL based circuits needed approximately 20% of less logic gates compare to the binary logic. Dynamic STI, PTI and NTI is proposed in [36].

Srivastava et al. [24] have proposed the circuit of ternary inverter based on the same concept of three different in-verters that is simple ternary inverter (STI), negative ternary inverter (NTI) and positive ternary inverter (PTI). Claims the implementation of inverter circuits without using as external resistance, but use the concept of length-to-width ratio [37] to provide the internal resistance to the circuit.

In [20] the author have proposed the circuit of inverter (STI, PTI and NTI) using carbon nanotubes FETs instead of CMOS without any external resistor. The author use the concept of changing threshold voltage of the transistor according to the diameter of CNT [38]. External resistor is actually replaced by varying the internal threshold voltage of the transistors. It has been observed that many researches proposes the circuit of inverter based on the concept of simple ternary inverter (STI), negative ternary inverter (NTI) and positive ternary inverter (PTI). Which are actually three different structure for inverter circuit. Moreover, the authors in multiple research papers claims the removal of external resistance in the circuit, but they have used the variable resistance transistors instead of external resistance. Still the circuit is having the overhead of variable threshold based transistors. The proposed circuit of t-NOT gate can be consider as the replacement of three different invertor circuits (STI, NTI, and PTI) for creating various circuits based on ternary logic. The proposed circuit don't need any overhead of external resistance, variable internal resistance or variable threshold transistors.

III. PROPOSED WORK

In this section, the working of op-amp is shown when the input voltage supply is greater than the upper limit of the voltage +VCC. The circuitry for t-NOT gate is proposed using current binary gates and operational amplifier (op-amp 741 IC). Simulation of the AND and OR gate is carried out over proteus as MAX and MIN gate.

A. Operational Amplifier (op-amp 741 IC)

Op-amp is an analog electronic device that is considered as the basic building block of many electronic circuits. It can be used for various purpose but here we have use the op-amp 741 as a comparator. Basic diagram of op-amp 741 is shown in the Fig 1 with pin configuration.

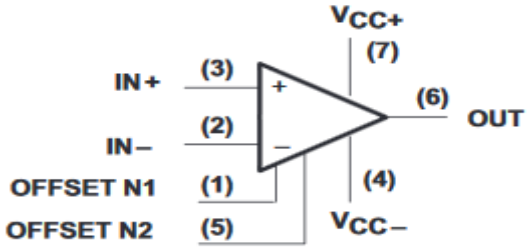

Fig 1. op-amp 741 IC

When we use op-amp as comparator then pin number 3(non-inverting voltage) is connected with input voltage VIN, pin number 2 (inverting voltage) with the reference voltage VR, pin number 7 and 4 with + and – VCC which represent the upper and lower voltage limit and from pin number 6 we get the output voltage VOUT. The standard functionality of the op-amp is shown in the Table 1. According to which is the input voltage is greater than the reference voltage then at pin 6 we get upper limit + VCC as the output voltage.

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Else, if the input voltage is less than the reference voltage we get lower limit -VCC as the output at pin 6. Now we will see the results of the op-amp when we supply the input voltage greater than the upper limit of the op-amp that is +VCC. For that we have conducted the set up in the lab and supply input voltage greater than the + VCC, in this case we observe that the op-amp give the upper limit + VCC as the output voltage as shown in the Table 2. The actual reading of the voltmeter incase when the input voltage of the op-amp is greater than the upper limit of the voltage of op-amp that is +VCC is shown in Table 3.

V_{IN}	V_{OUT}
$> V_R$	$+ V_{CC}$
$< V_R$	$- V_{CC}$

Table 1. Standard working of op-amp

V_{IN}	V_{OUT}
$> +V_{CC}$	$+ V_{CC}$

Table 2. When input voltage is greater than upper limit of op-amp

V_{IN}	V_{OUT}
+7.54V	+4.33V
+6.37V	+4.26V

Table 3. Actual result of op-amp when the input voltage is greater than the upper limit voltage (+VCC = 5V) of op-amp.

Considering this concept, we have proposed the circuit of t-NOT gate for ternary logic that is logic 0, 1 and 2. Where the actual range of the voltage representing the logic 0, 1 and 2 is shown in Table 4.

Logic	Voltage Range
0	0 to < 3
1	3 to < 5
2	≥ 5

Table 4. Voltage representation of the states of ternary logic

B. Circuitry and Functionality of t-NOT gate

A novel circuit is proposed for the implementation of the t-NOT gate based on the concept of ternary logic. The basic concept of the t-NOT gate is same as the concept of the binary NOT gate (inverter circuit). As in case of binary NOT gate, the low input (0V) is inverted into high (5V) and vice-versa. Similarly, in t-NOT gate a third state is introduced with logic 2 as shown in the Fig 2 and the truth table of the t-NOT gate is shown in Table 5.

a	*a'*	*a''*
0	1	2
1	2	0
2	0	1

Table 5. Truth Table t-NOT Gate

As shown in the Table 5 a' represent the partial transition of one logical state to another and a'' shown the complete transition of one logical state to another. Here by the term partial transition we mean that taking logic to immediate next state in clockwise direction as shown in Fig 2 for example if the input is logic 0 then the output of partial transition a' will be 1. In the same manner complete transition take the logic to the next to the immediate next state in clockwise direction for example if the input logic is 2 then the complete transition that is a'' will be 1.The t-NOT is unary gate same the binary NOT gate, it takes one input and provide one output. Single t-NOT gate provide the partial transition of one logical state to another. The proposed symbol for the t-NOT gate is shown in the Fig. 3 where a represent the input and a' represent the output after performing the partial transition of the input logic according to the truth table of t-NOT gate shown in Table. 5.

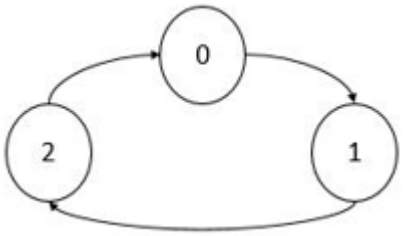

Fig 2. State Transition according to t-NOT gate

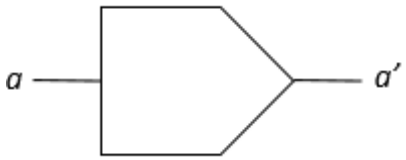

Fig 3. Symbol for t-NOT gate

Actual internal circuit of the t-NOT gate is shown in Fig 4 which consist of three op-amp 741 IC, one binary AND and binary OR gate. We have done the simulation of binary AND and OR gate on proteus to show that the binary AND and OR gate act as MAX and MIN gate. That mean the working of the binary AND and OR gate is to return the minimum and the maximum among the input voltages as the output voltage. The screenshot of simulation result for binary AND and OR gate, carried out on proteus is shown in Fig 5.

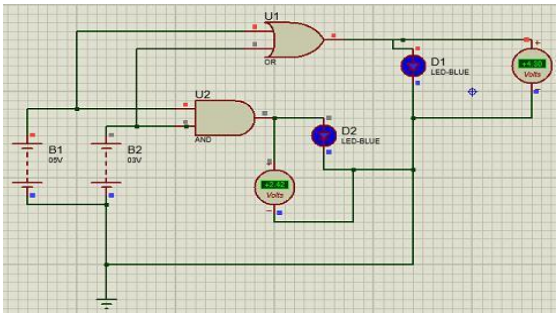

Fig 5. Simulation of binary AND and OR gate on proteus.

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As we can see in Fig 4 the connected B1 and B2 are 5V and 3V respectively, the output in the voltmeter connected diode D1 of OR gate is showing the reading +4.30V where as the voltmeter connected across the diode D2 of binary AND gate is showing the reading +2.42V. So, it mean that the AND gate is giving the resultant voltage near to +3V that is minimum among supplied voltages. And the OR gate is giving the output voltage as +4.30V which is near to 5V that is maximum among the supplied voltages. It prove that even in the case of ternary logic no separate MAX or MIN gate is needed, instead we can use binary OR and AND gate for the same. According to circuit diagram of t-NOT gate as shown in Fig 4 the first op-amp 741 IC is having +VCC = +5V, –VCC = 0V, VR is the variable voltage as it is connected with the input of the gate. Therefore, VR will always be equal to the supply input voltage to the t-NOT gate, VIN is 2V (constant). Similarly second op-amp 741 IC is having +VCC is variable voltage as connected with the input of the gate. So, that value +VCC will be always equal to the input voltage of the t-NOT gate, –VCC = 0V, VR is also variable voltage and connected to the input of the gate, VIN is 4V (constant). Finally third op-amp 741 IC is having +VCC = +5V, –VCC = 0V, VR is 2V (constant). Moreover, VIN is the variable voltage as it is connected with the VOUT of the second op-amp 741 IC. The VOUT of the first op-amp 741 IC is connected to the binary AND gate and the other input of the AND gate is 3V (constant). In addition, the input of the binary OR gate is the output voltage of the AND gate and the output voltage VOUT of the third op-amp 741 IC. The output voltage of the OR gate is the result.

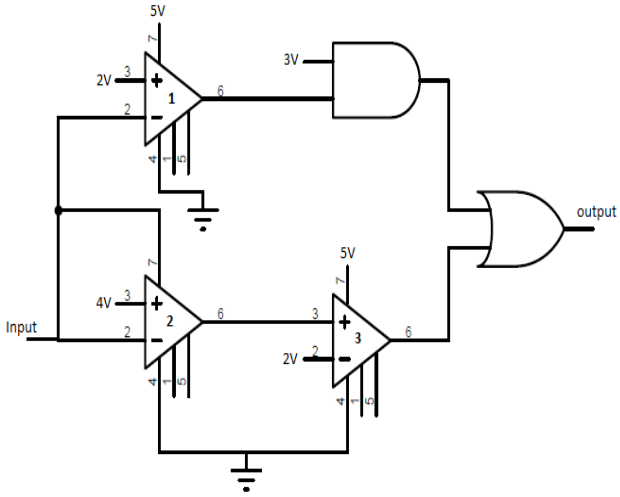

Fig. 4. Circuitry of t-NOT gate

IV. RESULTS AND DISCUSSION

Here, in this section we will discuss about the working of the proposed inverting circuit that is t-NOT gate as shown in Fig 4. In which when the 0V is supply to the t-NOT gate then the first op-amp gives the output as 5V (+VCC) because VIN = 2V which is greater than the VR = 0V. The VOUT of the first op-amp is supplied as one of the input voltage to AND gate with another input voltage is 3V so the output voltage of the AND gate will be equal to the minimum among 3V and 5V which will be 3V. And the 3V will be pass to OR gate as one of the input voltage. Similarly second op-amp will give VOUT = 0V as its VIN is greater than the +VCC (0V in this case). So, the output voltage of the op-amp that is VOUT = +VCC. This VOUT of the second op-amp pass as VIN to the third Op-amp whose VR = 2V (constant), so VOUT of the third op-amp will be equal to 0V which will act as the second input voltage to the OR gate. Finally, OR gate give the maximum among the input voltages (3V and 0V in this case) that is 3V. Now if 3V is the input to t-NOT gate then the first op-amp gives the output as 0V because VIN = 2V which is less than the VR = 3V. The VOUT of the first op-amp is supplied as one of the input voltage to AND gate with another input voltage is 3V so the output voltage of the AND gate will be equal to the minimum among 3V and 0V which will be 0V. And the 0V will be pass to OR gate as one of the input voltage. Similarly second op-amp will give VOUT = 3V as its VIN is greater than the +VCC (3V in this case). So, the output voltage of the op-amp that is VOUT = +VCC (3V in this case). This VOUT of the second op-amp pass as VIN to the third op-amp whose VR = 2V (constant), so VOUT of the third op-amp will be equal to 5V (+VCC) which will act as the second input voltage to the OR gate. Finally, OR gate give the maximum among the input voltages (0V and 5V in this case) that is 5V. Finally if 5V is input to the t-NOT gate then the first op-amp gives the output as 0V as VIN = 2V(constant) which is less than the VR = 5V. The VOUT of the first op-amp is act as one of the input voltage to AND gate with another input voltage is 3V(constant) so the output voltage of the AND gate will be equal to the minimum among 3V and 0V which will be 0V. This 0V will be pass to OR gate as one of the input voltage. Similarly second op-amp will give VOUT = 0V as its VIN is less than the VR (5V in this case). So, the output voltage of the op-amp that is VOUT = -VCC (0V in this case). This VOUT of the second op-amp pass as VIN to the third op-amp whose VR = 2V (constant), so VOUT of the third op-amp will be equal to 0V (-VCC) which will act as the second input voltage to the OR gate. Now, OR gate give the maximum among the input voltages (0V and 0V in this case) that is 0V. Final results of the circuit is shown in Table 6.

INPUT	OUTPUT
0	3
3	5
5	0

Table 6. Input and output voltage of t-NOT gate.

The proposed circuit of t-NOT gate based on ternary logic can be consider as the replacement of three different inverter circuits that is simple ternary inverter (STI), positive ternary inverter (PTI) and negative ternary inverter (NTI). The t-NOT gate can be used as a bulding block of various different circuits based on ternary logic and for higher radix as well.

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V. CONCLUSION

A novel circuit for inverting logic t-NOT gate is proposed which work on the ternary logic. Which take the input at 0V, 3V and 5V and give the out as 3V, 5V and 0V respectively. The working of op-amp 741 IC is presented for the standard condition that is when the input voltage is greater and less than the reference voltage. Experimental results are shown for the output voltage of the op-amp 741 IC when the input voltage is greater than the upper limit voltage +VCC. The simulation of AND and OR is done over proteus to show that binary AND and OR gate return the minimum and the maximum voltage as the output voltage among the supplied voltages.

REFERENCES

1. Charles M Allen and Donald D Givone. A minimization technique for multiple-valued logic systems. IEEE Transactions on Computers, (2):182–184, 1968. 1
2. Robert W Keyes. The evolution of digital electronics towards vlsi. IEEE Journal of Solid-State Circuits, 14(2):193–201, 1979. 1
3. Shweta S Dawley and Pradnya A Gajbhiye. Design and comparative analysis of binary and quaternary logic circuits. In Futuristic Trends in Research and Innovation for Social Welfare (Startup Conclave), World Conference on, pages 1–6. IEEE, 2016. 1
4. Zvonko G Vranesic and Kenneth C Smith. Engineering aspects of multi-valued logic systems. Computer, 7(9):34–41, 1974. 1, 2
5. Noboru Takagi and Kyoichi Nakashima. Discrete interval truth values logic and its application. IEEE Transactions on Computers, 49(3):219–229, 2000. 1
6. Daniel Etiemble. On the performance of multivalued integrated circuits: past, present and future. IEICE Transactions on Electronics, 76(3):364– 371, 1993. 1
7. Prabhakara C Balla and Andreas Antoniou. Low power dissipation mos ternary logic family. IEEE Journal of Solid-State Circuits, 19(5):739– 749, 1984. 1, 2
8. Kenneth C Smith. The prospects for multivalued logic: A technology and applications view. IEEE Transactions on Computers, (9):619–634, 1981. 1
9. Brian Hayes. Computing science: Third base. American scientist, 89(6):490–494, 2001. 1
10. Ben Choi. Advancing from two to four valued logic circuits. In Industrial Technology (ICIT), 2013 IEEE International Conference on, pages 1057–1062. IEEE, 2013. 1
11. Peter N Marinos. Fuzzy logic and its application to switching systems. IEEE Transactions on Computers, 100(4):343–348, 1969. 1
12. Tomoyuki Araki, Hisayuki Tatsumi, Masao Mukaidono, and Fujio Yamamoto. Minimization of incompletely specified regular ternary logic functions and its application to fuzzy switching functions. In ismvl, page 289. IEEE, 1998. 1
13. Joel Berman and Masao Mukaidono. Enumerating fuzzy switching functions and free kleene algebras. Computers & mathematics with applications, 10(1):25–35, 1984. 1
14. Tsutomu Sasao. Ternary decision diagrams. survey. In Multiple-Valued Logic, 1997. Proceedings., 1997 27th International Symposium on, pages 241–250. IEEE, 1997. 1
15. Melvin A Breuer. A note on three-valued logic simulation. IEEE Transactions on Computers, 100(4):399–402, 1972. 1
16. Miron Abramovici, Melvin A Breuer, and Arthur D Friedman. Digital systems testing and testable design, volume 2. Computer science press New York, 1990. 1
17. Yukihiro Iguchi, Tsutomu Sasao, and Munehiro Matsuura. A method to evaluate logic functions in the presence of unknown inputs using lut cas-cades. In Multiple-Valued Logic, 2004. Proceedings. 34th International Symposium on, pages 302–308. IEEE, 2004. 1
18. Petr Hajek,´ Kamila Bendova,´ and Zdenek˘ Renc. The guha method and the three-valued logic. Kybernetika, 7(6):421–435, 1971. 1
19. Masao Mukaidono. Regular ternary logic functions? ternary logic func-tions suitable for treating ambiguity. IEEE transactions on computers,

20.(2):179–183, 1986. 1, 2

21. Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi. Cntfet-based design of ternary logic gates and arithmetic circuits. IEEE transactions on nanotechnology, 10(2):217–225, 2011. 1, 2
22. CR Mingoto. A quaternary half-adder using current-mode operation with bipolar transistors. In Multiple-Valued Logic, 2006. ISMVL 2006. 36th International Symposium on, pages 15–15. IEEE, 2006. 1
23. Alex Heung and HT Mouftah. Depletion/enhancement cmos for a lower power family of three-valued logic circuits. IEEE Journal of Solid-State Circuits, 20(2):609–616, 1985. 1, 2
24. Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi. A novel cntfet-based ternary logic gate design. In Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on, pages 435–438. IEEE, 2009. 1
25. A Srivastava and K Venkatapathy. Design and implementation of a low power ternary full adder. VLSI Design, 4(1):75–81, 1996. 1, 2
26. TN Rajashekhara and I-SE Chen. A fast adder design using signed-digit numbers and ternary logic. In Southern Tier Technical Conference, 1990., Proceedings of the 1990 IEEE, pages 187–194. IEEE, 1990. 1
27. LS Phanindra, MN Rajath, V Rakesh, and KS Vasundara Patel. A novel design and implementation of multi-valued logic arithmetic full adder circuit using cntfet. In Recent Trends in Electronics, Information & Communication Technology (RTEICT), IEEE International Conference on, pages 563–568. IEEE, 2016. 1
28. HT Mouftah. A study on the implementation of three-valued logic. In Proceedings of the sixth international symposium on Multiple-valued logic, pages 123–126. IEEE Computer Society Press, 1976. 1
29. HT Mouftah and KC Smith. Injected voltage low-power cmos for 3-valued logic. In IEE Proceedings G-Electronic Circuits and Systems, volume 129, pages 270–272. IET, 1982. 2
30. HT Mouftah and IB Jordan. Integrated circuits for ternary logic. In Proc. 1974 Int. Symp. Multiple-Valued Logic, pages 285–302, 1974. 2
31. HT Mouftah and KC Smith. Design and implementation of three-valued logic systems with mos integrated circuits. In IEE Proceedings G-Electronic Circuits and Systems, volume 127, pages 165–168. IET, 1980. 2
32. Alex Heung and HT Mouftah. Decmos—a low power family of three-valued logic circuits for vlsi implementation. In Proc. ISMVL-84, pages 120–124, 1984. 2
33. HT Mouftah, ANC Heung, and LMC Wong. Qtc-1 a cmos ternary computer. In Proc. ISMVL-84, pages 125–132, 1984. 2
34. HT Mouftah and IB Jordan. Design of ternary cos/mos memory and sequential circuits. IEEE transactions on computers, (3):281–288, 1977. 2
35. John Barkley Rosser and Atwell R Turquette. Many-valued logics. 1954. 2
36. Zvonko G Vranesic and V Carl Hamacher. Ternary logic in parallel multipliers. The Computer Journal, 15(3):254–258, 1972. 2
37. C-Y Wu and H-Y Huang. Design and application of pipelined dynamic cmos ternary logic and simple ternary differential logic. IEEE journal of solid-state circuits, 28(8):895–906, 1993. 2
38. HT Mouftah and AI Garba. Vlsi implementation of a 5-trit full adder. In IEEE Proceedings G-Electronic Circuits and Systems, volume 131, pages 214–220. IET, 1984. 2
39. Jie Deng and H-S Philip Wong. A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its applica-tion—part i: Model of the intrinsic channel region. IEEE Transactions on Electron Devices, 54(12):3186–3194, 2007. 2
40. Stephen Cole Kleene, NG de Bruijn, J de Groot, and Adriaan Cornelis Zaanen. Introduction to metamathematics, volume 483. van Nostrand New York, 1952. 2
41. Yoshinori Yamamoto and Masao Mukaidono. Meaningful special classes of ternary logic functions-regular ternary logic functions and ternary majority functions. IEEE transactions on computers, 37(7):799–806, 1988. 2
42. Masao Mukaidono. On the mathematical structure of the c-type fail safe logic. IEICE Trans. Electron., 52(12):812–819, 1969. 2
43. Michael Yoeli and Shlomo Rinon. Application of ternary algebra to the study of static hazards. Journal of the ACM (JACM), 11(1):84–97, 1964. 2

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Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)
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