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Fractional Order-PID Controlled Closed-loop MLI based DP-FC for Fourteen-Bus System

D Narasimha Rao, P Srinivasa Varma

Abstract*: This work manages improvement of time response in fourteen- bus-framework utilizing MLI based Distributed Power Flow Controller (DP-FC)with PI and FOPID which is made out of a Distributed Power Flow, new gadget inside the group of FACTS. The DP-FC has a similar control capacity as the UP-FC, however with much lower cost and higher unwavering quality. This effort tends to one of the utilizations of the DP-FC to Compensate Voltage list in Transmissions Systems. Fourteen-bus-framework with ordinary VSI and with nine-level-MLI based DP-FC is mimicked and their outcomes are exhibited. Closed-loop-fourteen bus-framework With PI &FOPID-controllers are mimicked and the dynamic reaction shows that FOPID-controlled-DP-FC produces better reaction when-make-out with-PI-controlled-DP-FC.

***Index Terms*: About four key words or phrases in alphabetical order, separated by commas.**

I. INTRODUCTION

The Power quality issues like voltage varieties &flow varieties exhibited in the electrical systems are because of the customer's utilities.Voltage sag occurs due to addition of heavy loads. Voltage distortion occurs due to non—linear loads like cell-charger ,furnaces, laptops etc.. Guda Priyanka[1] introduced another part inside the 'Flexible-AC-Transmission-Framework(FACTS)family', called 'Distributed-Power-Flow-Controller(DP-FC)'. The DP-FC is obtained from the 'unified-power-flow-controller (UPFC)'. The DP-FC can be considered as an UP-FC with a wiped out normal dc-connect. The 'dynamic power-exchange' between the shunt &series-converters, which is through the regular dc-interface in the UP-FC, is presently through the transmission-lines at the '3rd-harmonic-recurrence'.

'Double-changes are done in DP-FC' by Rashmi[2]i.e., the basic dc-interface through which dynamic-power is traded between 'the-shunt&series-converters in UP-FC' is currently through the transmission lines at the third-harmonic-recurrence in DP-FC &TPSC(three-phase-series-converter) is isolated to a few SPSDC(single-phase-series-distributed-converters) which gives repetition, subsequently makes the framework increasingly dependable.

The connection and elements of the series-inverters of the DP-FC, the structure and the control standard of the series-inverters were proposed by Menglu Gao[3]. 'DP-FC-utilizing single-stage-DS-SC to acknowledge dynamic-power stream control through transmission-line' was proposed by Sandeep[4]. Breaking down the execution of DP-FC in transmission framework was exhibited by A.Gayathri Reddy[5]. Plan of a neural system based DP-FC for power-framework-stability was exhibited by G.Madhusudhana Rao[6].

To defeat this issue, an appropriated power stream controller was proposed by Anantha lakshmi [7] to moderate the voltage and current varieties because of three-phase-fault in a solitary machine framework. 'Oscillation-damping with DP-FC utilizing improvement procedures' was exhibited by Monika Sharma[8].In this, ideal plan issue is understood utilizing'Genetic-Algorithm(GA)&Differential-Evolution(DE)' calculation to optimize the damping controller-parameters.

DP-FC to enhance the power nature of 'thirty-three-bus-radial framework' was proposed by S. Vadivel[9]. 'Effect of DP-FC to enhance power-quality dependent on synchronous reference outline technique' was displayed by Ahmad Jamshidi[10].

K. S. Srikanth[11] displayed 'structure&usage of new DP-FC to control power-quality'. This DP-FC strategy is same as the UP-FC used to repay the voltage sag &the current-swell. In DP-FC, it wipe out the basic dc-connect capacitor and rather than single three stage-series-converter it has three individual single-phase-converters. Kuldeep[12] proposed examination of DP-FC in power framework for enhancing power steam control. 'DP-FC-application in power framework' to alleviate voltage-sag &swell was proposed by Meghana[13]. A near report on power quality enhancement in a hybrid-framework utilizing DVR &STATCOM versus DP-FC was exhibited by Anju Antony[14]. Gaurav proposed 'usage of DP-FC to enhance PQ(power-quality)for 220KV transmission-line'[15].

Correlation of execution of DP-FC& UPFC was proposed by Nikita[16]. Upgrade of DP-FC amid series converter-failures was proposed by V. Sudheer Kumar[17]. Displaying and reenactment of DP-FC framework for power quality enhancement was proposed by Ranga rao[18]. The control ability of DP-FC is to control the transmission impedance, the load-edge, and the greatness of the bus-voltage. M. Bindu[19] introduced power-quality upgrade &moderation of voltage -sag utilizing DP-FC."The-DP-FC can control the transmission-line-parameters, for-ex..,, line-impedance(Z), transmission-point(Θ), &bus-voltage size".

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The issues got with power-quality issues, for example, voltage-droop and swell can be moderated by utilizing DP-FC. Ideal arrangement of DP-FC for misfortune decrease utilizing firefly &genetic-calculation was displayed by P.Ramesh[20].

The organization of this paper is as follows:

Section-I deals with introduction and literature-survey. Section-II deals with research-gap.Section-III deals with system-description. Section-IV deals with simulation-results of DP-FC system. The present-work is concluded in section-V.

II. RESEARCH - GAP

The exceeding-writing does not pact with FOPID-controlled-DP-FC-system. This investigation recommends with FOPID-controller for DP-FC-system. The exceeding-writing do not report the evaluation of PI &FOPID controlled DP-FC-systems. This effort evaluates the results of PI & FOPID - controlled- DP-FC-systems in Fourteen – Bus - System (F-B-S).

III. SYTEM DESCRIPTION

"Block-diagram of basic – Distributed – Power – Flow – Controller (DP-FC)" is appeared in Fig-1. In the multi-bus system, DPFC is inserted between bus-i and bus -j. The control circuit generates pulses required for DP-FC. The 'proposed-block-diagram of DP-FC' is appeared in Fig-2.

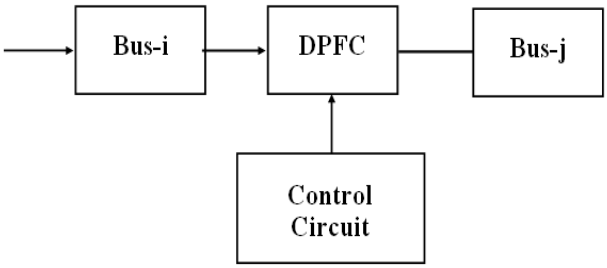

Fig-1. 'Block-Diagram of Basic-DP-FC-system'

Block-diagram of closed-loop- Distributed – Power - Flow-Controller (DP-FC) system" is appeared in Fig-2. In the multi-bus system, DPFC is inserted between bus-i and bus –j. Load-voltage is sensed and it is compared with reference-voltage. The voltage error is applied to the FOPID-controller. The out-put of FOPID is used to updatethe pulse-width of DPFC.

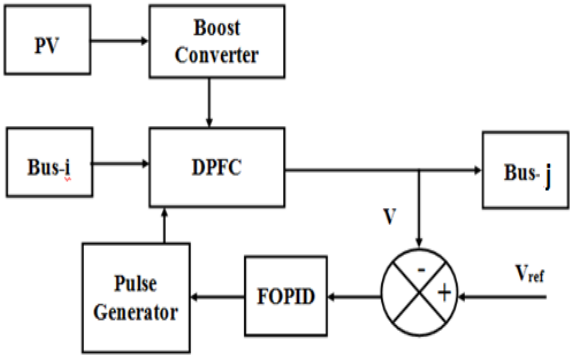

Fig-2.'Block-diagram of proposed-DP-FC-system'

IV. SIMULATION RESULTS

'Circuit-diagram of Open-loop-14-bus DP-FC-system with Disturbance' is delineated in Fig.3.An additional-load is associated at bus-9 produces a 'fall in voltage of bus-9'. There are five-generator buses &nine-load buses.Each-generator is represented as series-R.L-branch. Each- load is represented as a shunt-R.L-branch.

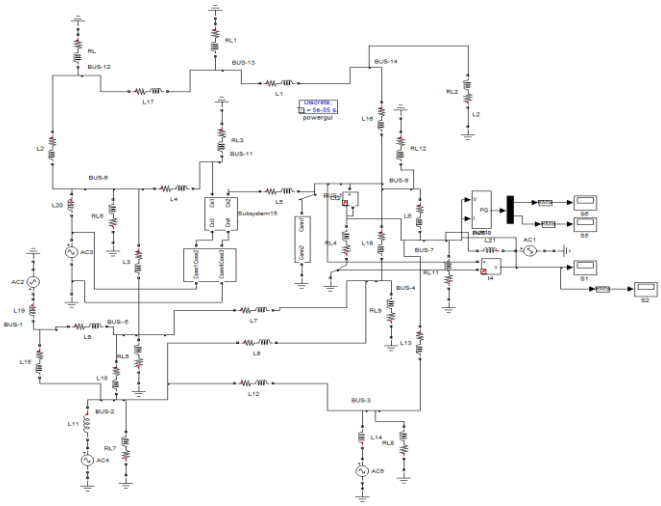

Fig-3. 'Circuit-diagram of Open-loop-FBS-DP-FC-system with Disturbance'

'Voltage at bus-10' is delineated in Fig-4 &the-value is 0.78* 10 4V. The 'voltage-decreases at Bus-10' due to increase in load by 0.3 sec.

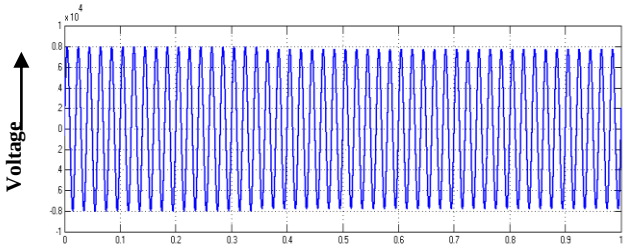

Fig-4.'Voltage at bus-10'of Open-loop-FBS-DP-FC-system

'Circuit-diagram of boost with Multilevel-inverter' is delineated in Fig-5.'Re-boost converter' is introduced between DC-source and M-L-I.

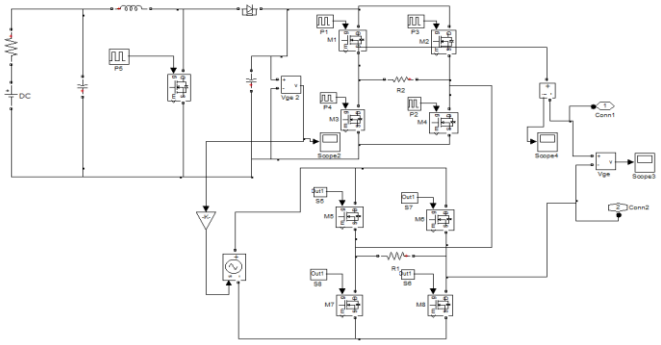

Fig-5. 'Circuit-diagram of Boost with multilevel-inverter'

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'Voltage-across multilevel-inverter' is delineated in Fig-6 and the-value is 180V.'RMS-voltage at bus-10'is delineated in Fig-7 and the-value is 5500V.

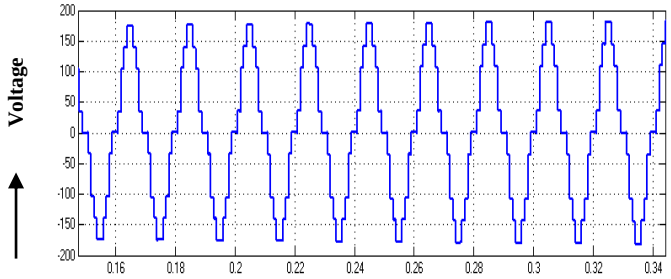

Fig-6.'Voltage-across multilevel-inverter'of Open-loop-FBS-DP-FC-system

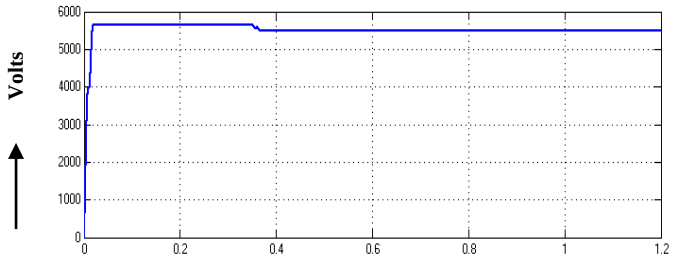

Fig-7.'RMS-voltage at bus-10 of Open-loop-FBS-DP-FC-system'

'Real-power at bus-10'is delineated in Fig-8 and the-value is5.7 * 10 5W. 'Reactive-power at bus-10'is delineated in Fig-9 and the-value is 3.4 * 10 4VAR.The 'fall in real-power is due to fall in voltage'.

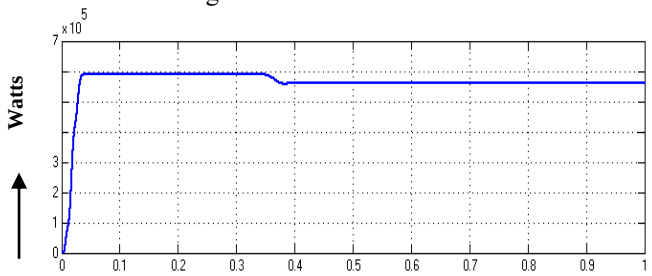

Fig-8.'Real-power at bus-10of Open-loop-FBS-DP-FC-system'

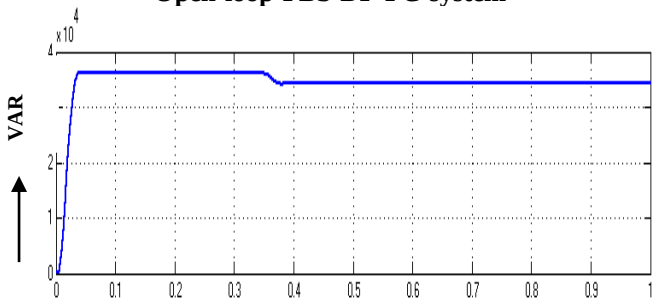

Fig-9.'Reactive power at bus-10of Open-loop-FBS-DP-FC-system'

'Circuit-diagram of Closed-loop-14-bus DP-FC-system with PI-controller' is delineated in Fig.10.'Voltage at bus-10' is delineated in Fig-11 and the-value is 0.8 * 10 4 V.'Voltage at Bus-9 'is sensed and it is evaluated with the reference-voltage to get Voltage-Error (VE). The'VE is directed to a PI-controller'. The 'yield of PI' is used to adjust the Pulse-Width(PW) of boost-converter.

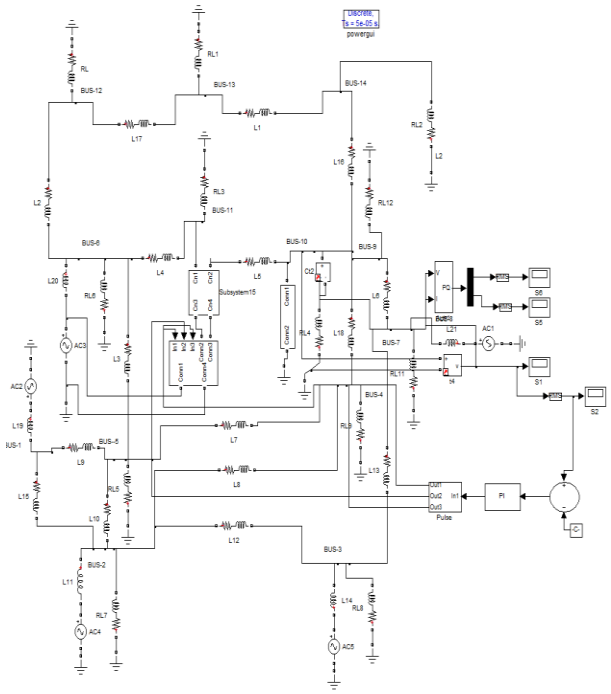

Fig-10.'Circuit-diagram of Closed-loop-FBS-DP-FC-system with PI-controller'

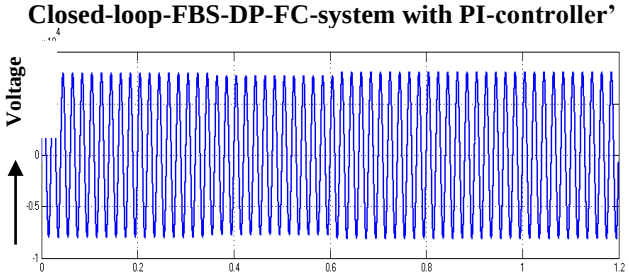

Fig-11.'Voltage at bus-10 of FBS-DP-FC-system with PI-controller''

'Circuit-diagram of Boost with multilevel-inverter' is delineated in Fig-12.

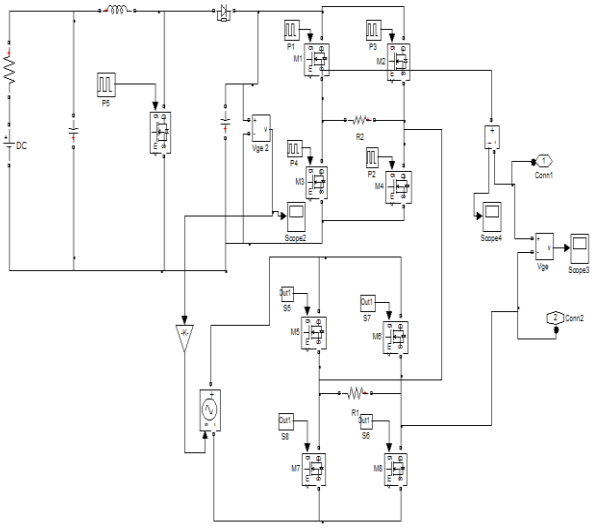

Fig-12.'Circuit-diagram of Boost with multilevel-inverter'

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'Voltage across multilevel-inverterof FBS DP-FC-system with PI-controller' is delineated in Fig-13 and the peak-value is 180 V.

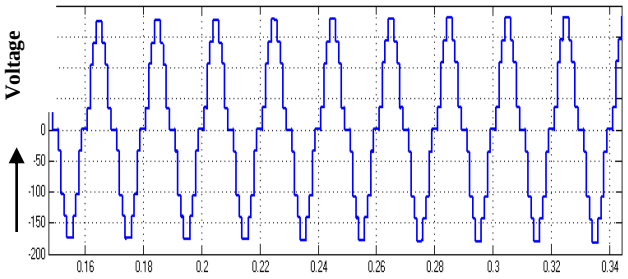

Fig-13.'Voltage-across multilevel-inverter of FBS-DP-FC-system with PI-controller''

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'RMS-voltage at bus-10of FBS-DP-FC-system with PI-controller'is delineated in Fig-14 and the-value is 5800V.'Real-power at bus-10of FBS DP-FC-system with PI-controller'is delineated in Fig-15 and the-value is6.2 * 10 5Watts. 'Reactive-power at bus-10of FBS-DP-FC-system with PI-controller'is delineated in Fig-16 and the-value is 3.8 * 104VAR.

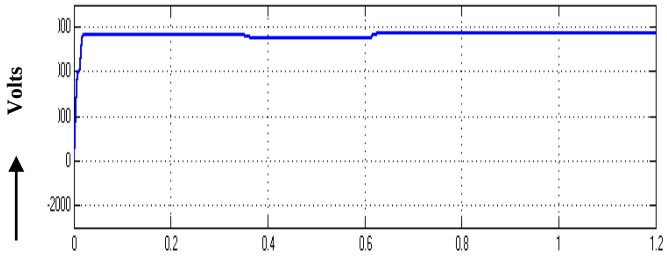

Fig-14.'RMS-voltage at bus-10 of FBS-DP-FC-system with PI-controller''

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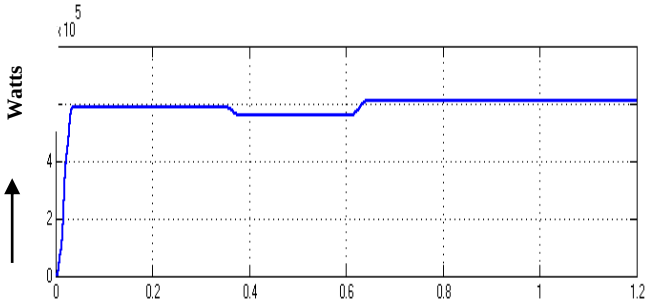

Fig-15.'Real-power at bus-10 of FBS-DP-FC-system with PI-controller''

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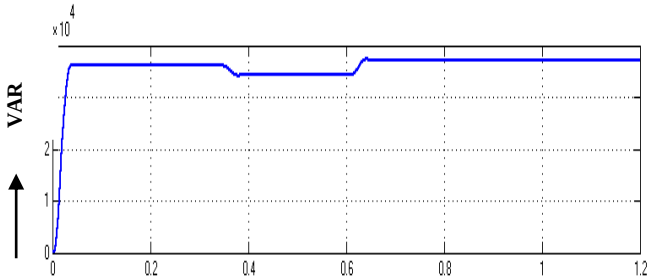

Fig-16.'Reactive-power at bus-10 of FBS-DP-FC-system with PI-controller''

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'Circuit-diagram of closed-loop-14-bus DP-FC system with FOPID-controller' is delineated in Fig-17. 'Voltage at bus-10of FBS-DP-FC-system with FOPID-controller' is delineated in Fig-18 and the-value is 0.8 *104V.VE is given to FOPID-controller. The 'yield of FOPID' is used to update the Pulse Width (PW)of BC to bring the bus-voltage to normal-value.

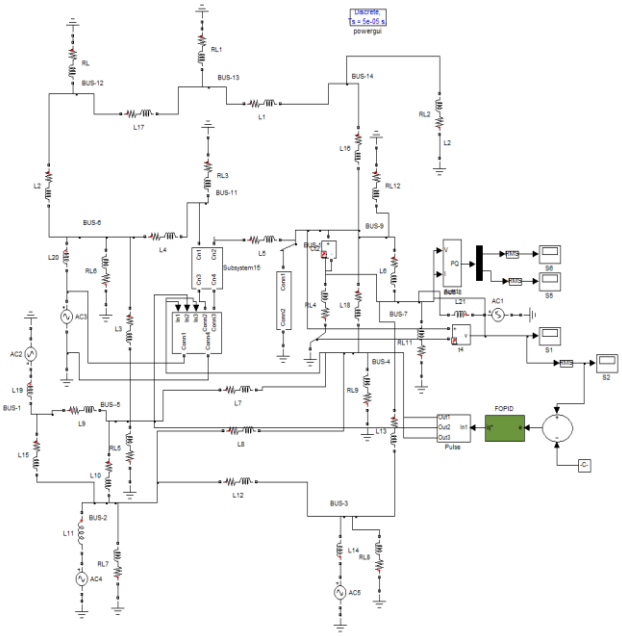

Fig-17.'Circuit-diagram of closed-loop-FBS-DP-FC-system with FOPID-controller'

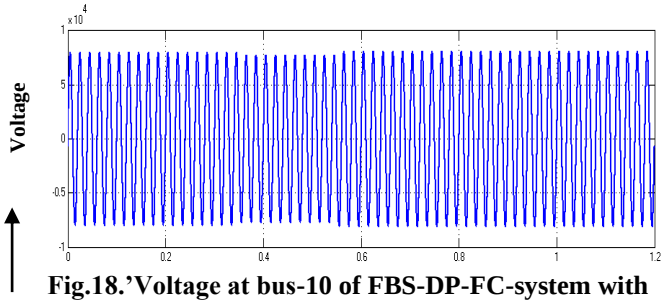

Fig.18.'Voltage at bus-10 of FBS-DP-FC-system with FOPID-controller''

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'Circuit-diagram of Re-boost with multilevel-inverter' is delineated in Fig-19. DC-voltage of boost converter is stepped-up using Re-boost converter and it is applied to the M-L-I.

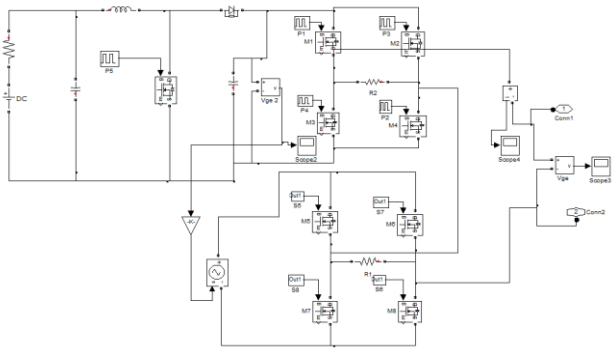

Fig.19.'Circuit-diagram of Re-Boost with multilevel-inverter'

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'Voltage-across-multilevel-inverterof FBS-DP-FC-system with FOPID-controller' is delineated in Fig-20 and the-value is 180V.RMS- voltage at bus-10of FBS-DP-FC-system with FOPID-controlleris delineated in Fig-21 and the-value is 5800V.'Real-power at bus-10of FBS-DP-FC-system with FOPID-controller'is delineated in Fig-22 and the-value is6.1 * 10 5Watts. 'Reactive-power at bus-10of FBS-DP-FC-system with FOPID-controller'is delineated in Fig-23 and the-value is 3.8 * 10 4VAR.

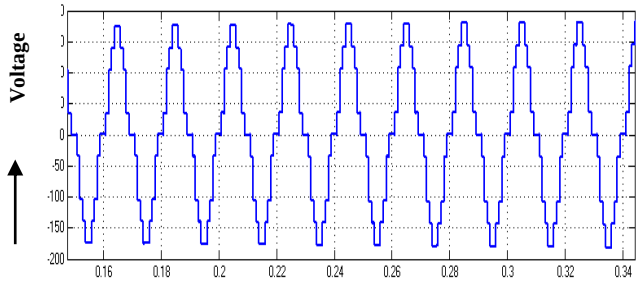

Fig-20.'Voltage-across-multilevel-inverter of FBS-DP-FC-system with FOPID-controller'

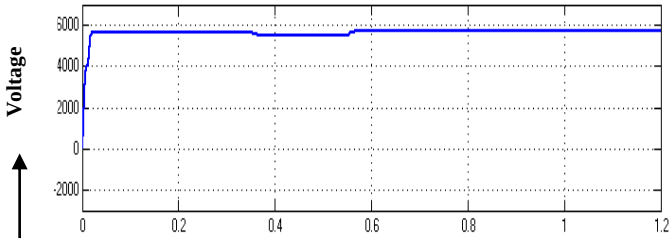

Fig-21.'RMS-voltage at bus-10 of FBS-DP-FC-system with FOPID-controller'

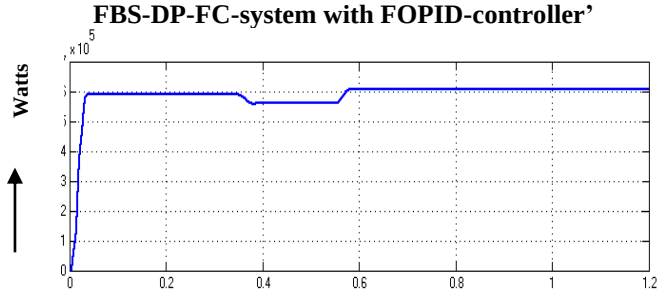

Fig-22.'Real-power at bus-10 of FBS-DP-FC-system with FOPID-controller'

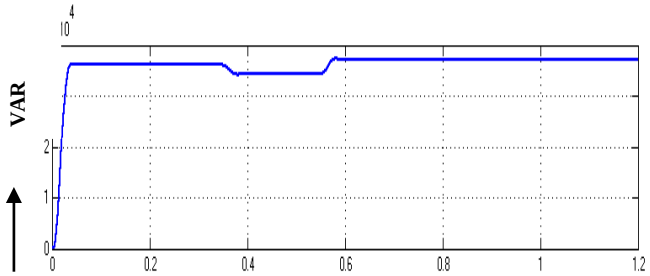

Fig-23.'Reactive-power at bus-10 of FBS-DP-FC-system with FOPID-controller'

Comparison of time-domain-parameters with PI and FOPID-controller for a reference value of 5800V is given in Table-1.By using FOPID-controller, the 'rise-time' is reduced from 0.36 Sec to 0.35 Sec; 'peak-time' is reduced from 0.58 Sec to 0.45 Sec; 'Settling-time' is reduced from 0.63Sec to 0.56Sec&'steady-state-error' is reduced from 0.09V to 0.05 V.

Table-1'Comparison of time-domain-parameters with PI& FOPID-controllers for a reference-value of 5800 V'

Controllers	Rise-time (s)	Peak-time (s)	Settling-time (s)	Steady-state-error (V)
PI	0.36	0.58	0.63	0.09
FOPID	0.35	0.45	0.56	0.05

'Comparison of time-domain-parameters with PI and FOPID-controller for a reference value of 5850 V' is given in Table-2.By using FOPID-controller, the 'rise-time'is reduced from 0.37 Sec to 0.36 Sec; 'peak-time'is reduced from 0.59 Sec to 0.47 Sec; 'Settling- time' is reduced from 0.65Sec to 0.57Sec and 'steady-state-error' is reduced from 0.11V to 0.06 V.

Table-2
'Comparison of time-domain-parameters with PI &FOPID (Vref = 5850V)'

Controllers	Rise-time (s)	Peak-time (s)	Settling-time (s)	Steady-state-error (V)
PI	0.37	0.59	0.65	0.11
FOPID	0.36	0.47	0.57	0.06

V. CONCLUSION

Re-boost-converter MLIbased DPFC is proposed for FBS.Closed loop DP-FC based FBS systems with PI and FOPID-controllers are simulated using MABLAB-SIMULINK. The setteling-time is as low as 0.56 Sec. &steady state error is 0.05 V with FOPID controller. The outcome represents that the 'settling time &steady state error' are diminished using FOPID-controller.Hence, Closed loop 14 bus DP-FC-system with FOPID- controller is superior to Closed loop 14 bus DP-FC system with PI-controller. The benefits of DP-FC is that the bus voltage profile is improved and the drawback of DP-FC is that it needs multiple-series-converters The present-work deals with 'Closed loop 14 bus DP FC system with FOPID controller'.'Closed loop 14 bus DP-FC system with PR controller' will be done in future.

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