Design and Comparison of Different 4:2 Compressors Based on 180nm Technology

Sri Laxmi.P, B. Kumar Sanjiv, Vandana Khare

Abstract --- Many of the circuits such as portable devices, digital signal processing filters, compressors are basic building block for high performance. Different logic types of 4:2 compressors are designed and their performance is computed. The new design uses, different logic style which cut down power consumption and delay. For getting high speed and consuming less power, the new compressor are proposed which consists of eight transistors (8T) XOR-XNOR unit. Different models get designed and simulated using Cadence Virtuoso tool (180nm). From simulation results we reached the improvement of less power consumption, speed of proposed 4:2 compressors.

Keywords: 4:2 compressor, eight transistors(8T),logic styles, Virtuso Cadence tool, power consumed..

1. INTRODUCTION

Today's scenario portable devices have a prominent role in semiconductor industry which in turns to lot of demand for multimedia based applications. Most of digital systems like (digital signal processors, filters, µ processors etc) are using efficient compressors (High speed). The project aim is to design a 4:2 compressor which takes less power consumption and perform with less delay. And the capital Objective of the paper is to explain about different styles of compressor designs and their simulation results.

To reducing the operands, while adding partial products the compressors are introduced in multiplication process. Three main stages in multiplication are first stage is to generating the partial product, second stage is to reduce the partial product and the last stage is computation of product. The input for 4:2 compressors as four partial products and the output as reduced to two partial products and critical path delay is also deducted. The proposed designofa4:2compressor has four multiplexers on transmission logic gate and eight transistors.

2. DIFFERENT STYLES OF 4:2 COMPRESSORS

a. Compressor using 2 full adders

The module has input signals (x1, x2, x3, x4 and C_{in}) and output as Sum and Carry as shown in fig 1(a). The C_{in}signal is doesn't affect the

C_{out}.Sum=x1⊕x2⊕x3⊕x4(1)

Carry= Majority [{x1⊕ x2 ⊕x3}, x4, C_{in}] (2)

C_{out}= Majority(x1, x2, x3) (3)

The full adders are constituent of XOR blocks and multiplexers and also from the above equations we can calculate delay from the equation 4*Δ-XOR gates as shown in Fig .1(b)

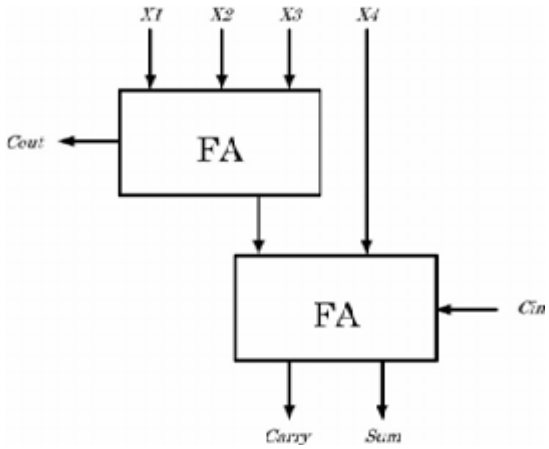

Fig1. (a) Conventional method of 4:2 compressor

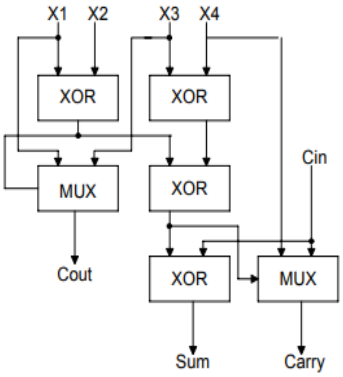

Fig1. (b) 4:2 compressor internal structure of two full adders

b. 4:2 compressor using full adder, OR, NAND, & XNOR gates

The second style of compressor consists of adder units and gate units such as (NAND, XNOR, ORgates and Full Adder Unit) as shown in figure 2. In this module twofull adders are connected serially. Where C_{in} , x1, x2, x3 and x4 are inputs, whereas Sum and carry as outputs.

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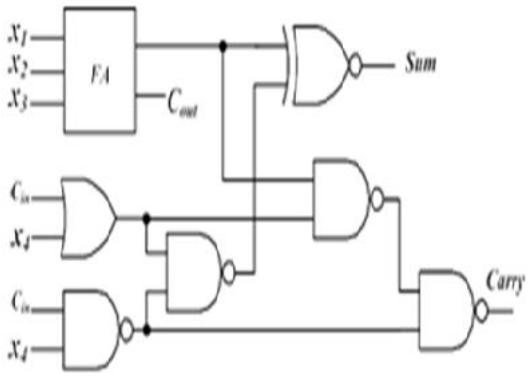


Fig 2. 4:2 compressor using NAND, XNOR, OR and two full adders.

In most of the platforms this gate level module design are process. One of the important criteria for any market is time to facilitated hardware but drawback it is to limited optimization capability.

c. Compressor using Majority & XOR gates

The compressor using Majority & XOR gates are presented in figure3. To form a three input XOR gate we are cascading 2 input XOR gates.

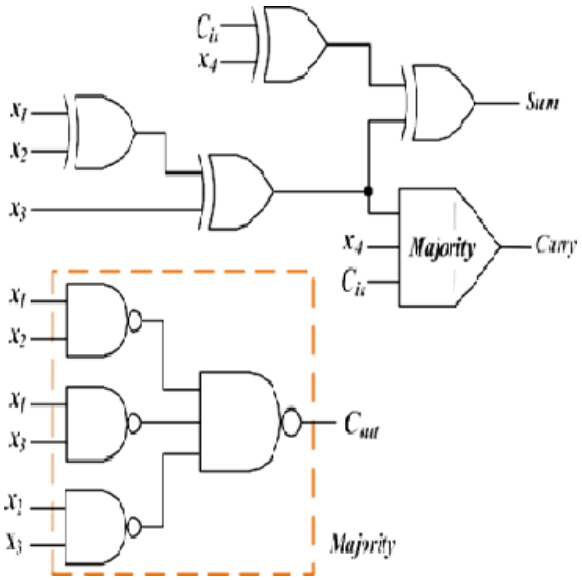


Fig3. Compressor using Majority and XOR gates

By the simulations we come to know that it is good energy efficient structure.

3. IMPLEMENTATION

Proposed compressor

A new layout comprises of transmission logic (four Multiplexers), six transistor (6T) XNOR inverter and two 8T (eight transistors)XOR-XNORunits. For getting good result in speed, full potential swing we have to use XNOR gate operation in this layout and also it consumes less power.

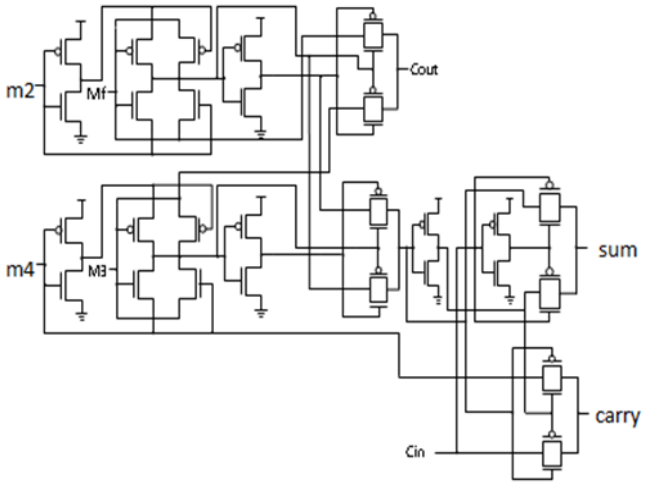


Fig4.Proposed Compressor diagram

The transistors mp1 and mn1 are generates the output which is complement of Y input. The transistors mn2 and mp2 are controlled by the output of (mn1&mp1 transistors). The output of second inverter will produce voltage degradation problem for two combinations (x=0, y=1 and x=1, y=1) to avert fault we are introducing two more transistors mp3 and mn3.

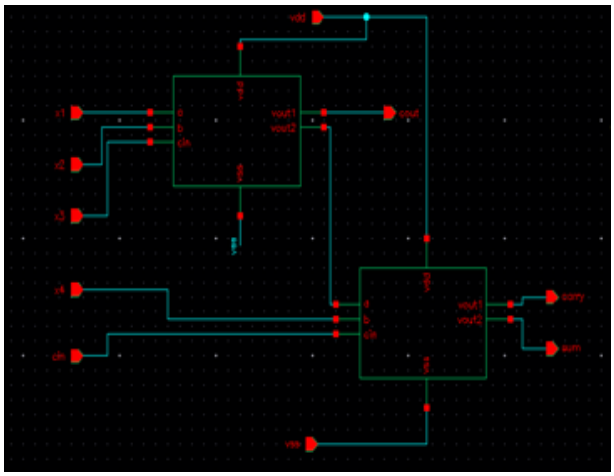
1. X=0, Y=0: mp1 and mp2 are ON, logic output is high
2. X=0, Y=1: mp2, mp3, mn1 and mn3 are ON logic output is low.
3. X=1, Y=0: mp1 and mn2 are ON logic output is low.
4. X=1, Y=1: mp3, mn1, mn2 and mn3 are ON logic output is high.

In this layout multiplexer3 generates an inverted output for given in input. Input for multiplexer1 and multiplexer2 are the XOR-XNOR cell output. The multiplexer2 and its complement are given to multiplexer4 (Carry generator).

4. RESULTS

Following are different styles of 4:2 compressors schematics and results. Fig 5.a is about conventional model of compressor result and schematic and result.

Conventional method of 4:2 compressor



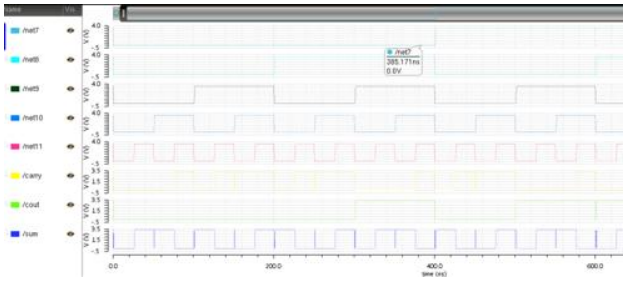
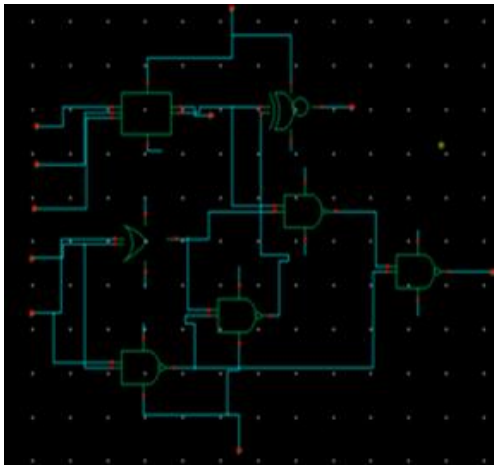


Fig 5.a Conventional Compressor Schematic and Output

Compressor using two full adders, NAND, OR and XNOR gates

Fig 5.b is about Compressor using two full adders, NAND, OR and XNOR gates of result and schematic and result.



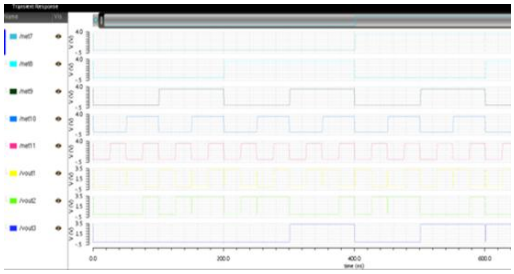
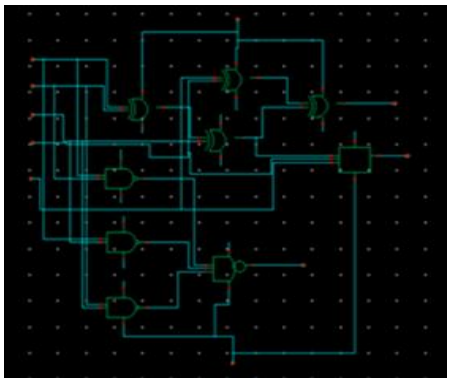


Fig 5.b 4:2 Compressor Schematic and Output Compressor using Majority and XOR gates

Fig 5.c is about Compressor using Majority and XOR gates of result and schematic and result.



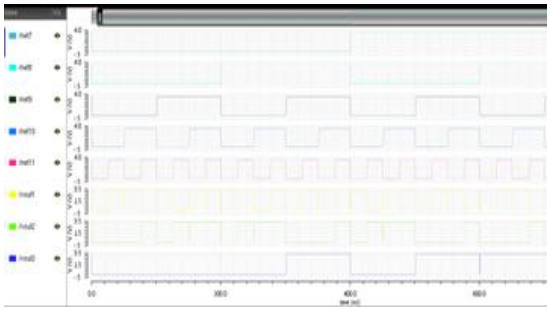
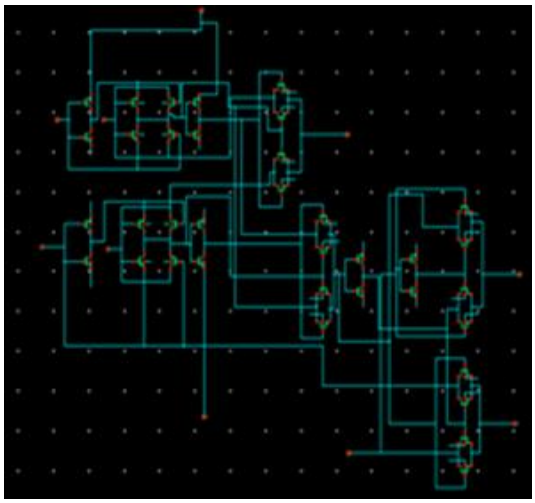


Fig 5.c Schematic and Output of 4:2 Compressor

Proposed Compressor

Fig 5.d is about proposed compressor of result and schematic and result.



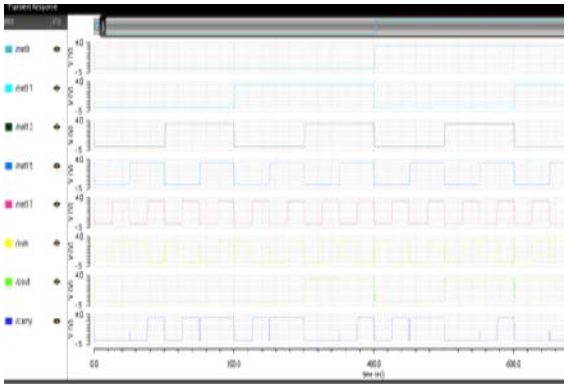


Fig 5.1.d 4:2 Compressor Schematic and Output

Table 1. Different styles of power consumption of 4:2 compressors in µW and delay in Nano seconds are compared

Different styles of 4:2 Compressors	POWER (Micro Watts)	DELAY (Nano sec)
Conventional method Compressor	74.96	400.5
Compressor using Full adder, NAND, OR and XNOR gates	98.51	400.6

Compressor using Majority & XOR gates	142.4	400.5
Proposed Compressor	23.26	400.2

The result for above proposed module with givenvoltageof3.3V, an averagepowercut down by the newcompressoris23.26µWandthesuperlative delay is 400.2ns

5. CONCLUSION

The proposed layout consequently attains the reduced power consumption and less delay using 36 transistors. For achieving the good energy-efficient compressor reduced transistor area is proposed. Comparing with previous designs the proposed module achieved less no. of transistors, cut down area and high energy efficiency. As result for above modules with givenvoltageof3.3V, anaveragepowercut down by theproposedcompressoris23.26µWandthesuperlative delay is 400.2ns.

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