

# Modified Multicast Routing Algorithm for Network-on-Chip

K.Shoukath Ali, P.Samapth, S.Elango, Sajan P Philip

**Abstract:** In this paper, the Multicast Routing (MR) algorithm problem for Networks-on-Chip (NOC) is studied and an efficient routing algorithm is proposed. Here each and every MR step is designed as a Minimum Directed Spanning Tree (MDST) Problem. The MDST capably finds the best routing solutions for multicast flows. Power consumption is one of the major evaluation parameter for routing inside Network-on-Chip (NOC). The power consumption mentioned here includes both leakage power and dynamic switching power. Simulation is performed over several randomized network layouts and the results are compared with conventional PIM-DM. In particular, the proposed algorithm achieves a 24% reduction in power consumption over conventional PIM-DM when the number of computational cores inside a chip is nearly hundred.

**Key words:** minimum spanning tree, shortest arborescence, leakage power, dynamic switching power, computational cores.

## I. INTRODUCTION

NoC architectures are design and proposed in nanoscale systems-on-chip (SoC) to the worldwide communication challenges [1, 2]. Besides design and verification benefits, the design and verification of NoCs increases the daunt clock and signal integrity.

NoC can be designed as custom network regular or regular network topologies [3-5]. There are number of challenges discussed for NoC routing problem.

In broad, node can be formed mutually and connect to the same node routers still even if they are not same sources (S) or destinations (D) of the same node group of flows because they may be able to beneficially share the common intermediate network resources. Also it is tough to take decision of sizes of partitions earlier, namely whether a design with a small number of larger routers would be extra cost efficient than a design with smaller routers. In this paper, a power minimisation problem is considered for efficient routing algorithm. Leakage power is good technique and it shows the increasing and dominating factor [6-7]. Hence it is most important to accounting the leakage power when summing the routers and network nodes to the synthesised designed architecture.

The rest of the paper is organised as follows. The proposed algorithm is discussed in section II. The ns2 implementation is shown in section III. Finally, simulation results and conclusions are presented in sections IV and V, respectively.

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## II. PROPOSED ALGORITHM

In this paper, the problem of MR for NoC is discussed and designed an efficient routing algorithm is proposed for MR. Here each MR step is formulated as a MDST problem. In this literature [13, 14] discuss the algorithm, which is used to calculate the RMDST of MRG with the S router as root.

$$c(i, k) = c(i, j) - c(x(j), j) \quad (1)$$

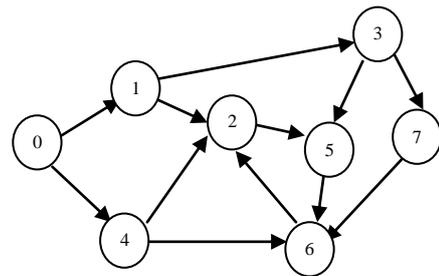


Fig. 1. Initial (Available Network connections)

The figure 1 shows a sample network connection point. It is treated as a strongly connected graph since there is a path from every node to every other node. In this example, node 0 is kept as the root (source) node.

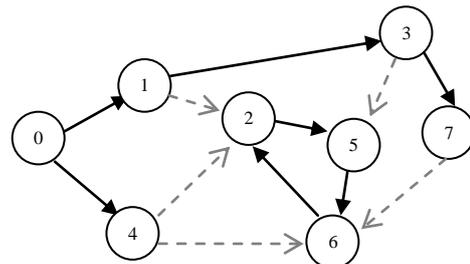


Fig. 2. Connectivity after step 1

Nodes 2, 5 and 6 form a cycle. There is no tree formation. Nodes in the cycle cannot be reached from the root(source) node.

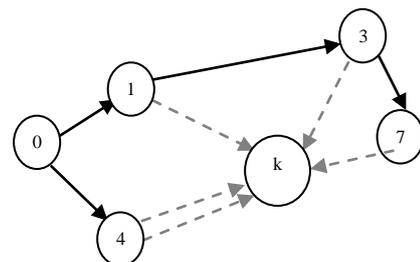


Fig.3. Contract into Pseudo-node for finding minimum extra cost



Nodes 2, 5 and 6 are contracted to form a pseudo-node (k). This approach leads to find the minimum extra cost needed to avoid the formation of cycles.

Arc (7, 6) is chosen since it has the minimum extra cost to clear the cycle. The final graph gives the rooted directed minimum spanning tree.

For a graph with |N| nodes and |E| edges, the complexity of the algorithm is  $O(|V|^2)$ . The above algorithm is proven to give optimum result for a given topology. The mathematical proof of the above statement is given in [12, 13].

In context of Network-On-Chip, the nodes correspond to IP cores and the edges correspond to connectivity flows.

### III. IMPLEMENTATION

The proposed algorithm is implemented using C++. Then it is integrated with ns2 to carry out packet level simulation. Various randomized scenarios (graphs) are created to analyze the performance of the proposed algorithm.

For comparison purpose, a standard multicast algorithm PIM – DM used in Internet routing is chosen. This protocol is chosen because PIM – DM is normally deployed in situations where multicast nodes are densely spread over a Large number of nodes. This kind of connectivity typically resembles the same kind of connectivity in NoC. Power consumption is used as the evaluation criteria. Various randomized scenarios (graphs) are generated and simulated in ns2. Some of them are shown below. The layout of the scenario is arbitrary and doesn't have any significance.

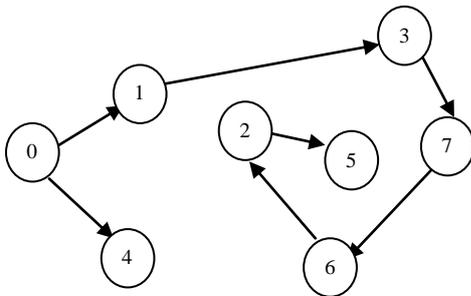


Fig.4. Final graph (rooted directed minimum spanning tree)

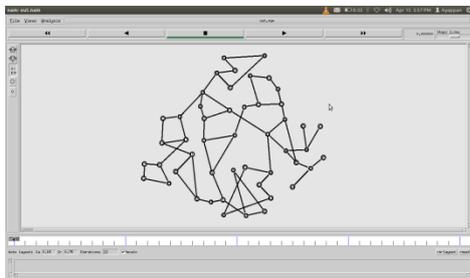


Fig. 5. Random Scenario with 50 nodes & 60 links

Fig.5 shows a randomized graph with a random node chosen as the root node. Each link was also given a random cost. In ns2, randomness is obtained through the use of declaring a random variable.

Appropriately uniform random variable is chosen since for a given interval, uniform random variable is meant to give ultimate randomness than any other random variable. Routes are formed when routing functionalities are enabled in each node.

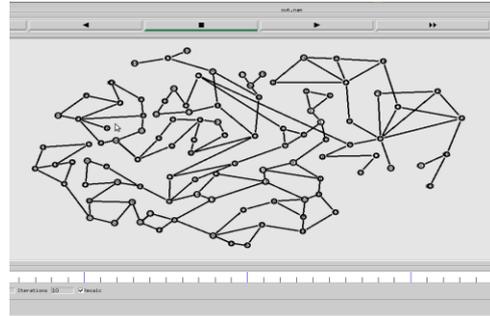


Fig. 6. Random Scenario with 104 nodes & 138 links

Fig.6 shows another graph with the nodes increased to 104. All scenarios are made to run over a time period of 4 minutes. For calculation of leakage power, standard values are taken from Table I. And for dynamic switching power calculation, switching bit energy values are also taken from Table I and a data rate of 2 Gbps is chosen which is the maximum rate possible given a frequency constraint of 1 GHz under binary signaling.

### IV. RESULTS & DISCUSSIONS

Various randomized networks are created with increasing number of nodes and links. As mentioned earlier, leakage power is increasingly dominating over dynamic switching power when the number of computational cores ( or nodes) approaches 100.

Tables II shows the comparison of leakage power of the proposed algorithm with PIM-DM. Table III shows the comparison of dynamic switching power.

TABLE II. COMPARISON OF LEAKAGE POWER

Nodes	Links	Leakage Power (W)	
		PIM- DM	Proposed Algorithm
20	25	0.108	0.075
34	42	0.194	0.118
50	60	0.291	0.183
66	81	0.378	0.248
82	104	0.496	0.313
104	138	0.668	0.441

TABLE III. COMPARISON OF DYNAMIC SWITCHING POWER

Nodes	Links	Dynamic Switching Power (W)	
		PIM - DM	Proposed Algorithm
20	25	0.0086	0.0059
34	42	0.0155	0.0093
50	60	0.0232	0.0145
66	81	0.0301	0.0197
82	104	0.0394	0.0249
104	138	0.0505	0.0350

From Table II, it is clear that the proposed algorithm significantly outperforms PIM-DM. For large number of nodes (or routers, in one case we can say that as computational cores), the reduction in leakage power is tremendous. This is due to the fact that the proposed

algorithm utilizes more routers with less number of input and output ports rather than utilizing fewer routers with more number of input and output ports.

For example, consider the random scenario with 104 nodes and 138 links. On applying the proposed algorithm, a spanning tree structure is formed with 16 routers requiring 4 x 4 (in x out) ports and 3 routers requiring 5 x 5 (in x out) ports whereas PIM-DM finds a structure with 25 (4 x 4) routers and 3 (5 x 5) routers.

The proposed algorithm also achieves a good reduction in dynamic switching power when compared with PIM-DM. The problem with PIM-DM and other such algorithms is that they are developed for routing packets in internet where reliability and speed is of utmost importance. Typically the strategy of every routing protocols deployed over the internet is to reduce the number of hops a packet makes as it traverses to reach the destination. But when comes to network-on-chip, any reduction in hop counts leads to an increase in the router links which in turn increases the overall power consumption. The total power consumption (sum of leakage power & dynamic switching power) is calculated and a comparison is made.

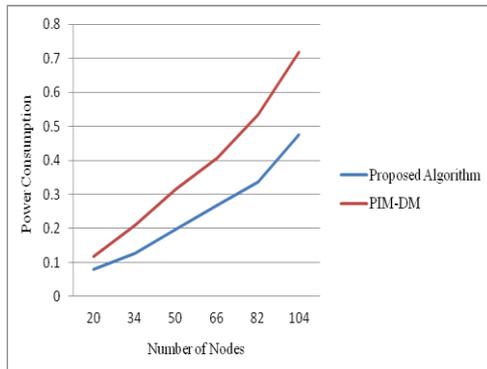


Fig.7. Comparison of Total Power Consumption

Figure 7 shows the total power consumption in the case of PIM-DM and the proposed algorithm. As we increase the number of nodes to 104, there is significant improvement in power savings for the proposed algorithm. In particular, the proposed algorithm achieves a 24% power reduction over PIM-DM when the number of nodes reaches 100 or above.

## V. CONCLUSION & FUTURE WORK

In this paper, the problem of multicast routing is studied and an efficient multicast routing algorithm is proposed. Since power consumption is a major bottleneck in Network-on-Chip, it is taken as the evaluation parameter. The dynamic switching power and leakage power is considered for simulation. Experimental results show that the proposed algorithm consumes less power when compared to PIM-DM. The power savings are greater when the size of the network increases. Power consumption can further be reduced and a more realistic network model of NoCs can be created if the interconnects are also taken into account for which works are being done.

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