Multi Attribute Test Pattern Optimization for Test Power Minimization in Digital Circuits

Y.Sreenivasula Goud, B.K.Madhavi

Abstract--- Test patterns are the primary bit patterns in need for testing a digital circuitry. Majority of the logical device developed are tested for all functionality before its practical usage. The logical denote and functional complexity has developed new constraint in testing of digital circuit. In developing test patterns for digital test operation, the need of optimal pattern selection are major concern. To develop an optimal test pattern alignment to conserve test power utilization, a new test pattern generation using multi attribute Decision logic and pattern sequencing is proposed. The proposed approach develop a new decision approach in test pattern optimization using the test coverage density and fault test reliability and provide a low power testing approach in digital circuit testing. The simulation result for the proposed system defines the significance of test pattern optimization in power conservation.

Index Term: Test pattern optimization, low power, fault test density, digital fault test unit (DFTU)

I. INTRODUCTION

Increase in logic density, improvement of new technology in digital definition, logical integration and functional verification has outcome the possibility of developing high complex operation under a single chip implementation. Increase in logical integration has led to the development of new challenges with its testing. The conventional fault testing approach has become exhaustive in generating test pattern and applying for fault testing for large complex digital circuitry. Towards optimizing the fault test pattern generation various approaches were developed in past. The past approaches were developed with the scan test, roving test and redundant test approach. The sources of the faults are the carrier effect [1], Electro migration [2], and time dependent dielectric breakdown [3] in the digital circuit. The test demands a large processing overhead and the latency of fault diagnosis result is slower time to market. Towards the diagnosis of faults in digital architecture, test patterns are passed to test the stuck-at faults, bridging faults and delay faults [4]. However, due to large interconnection and larger transitions of input patterns, the test reliability is minimized. In the approach of roving or redundant test method, the test patterns are moved between each logical interconnection in a random manner to evaluate the test performance. However, this tracing results in high testing time, which needs to be minimized. In such testing approach, the flow of data from on Input line to the output line is traced in a non-linear manner, resulting in large testing overhead. In addition, the boundary scan test and the logical interconnections test are carried out in two different stages. These testing constraints to, 1) Random data flow, and 2) multiple testing's for boundary scan and system testing, lead to larger test time, larger area overhead and lower fault coverage. To obtain a common objective of boundary-scan and system testing, a hybrid coding with the feature of I/O testing and logical block testing is focused. Towards fault detection, In the test operation in digital circuit testing, test pattern such as the regular test expression in a random manner are applied. The DFT approach [5-8] are used in a liner, random or predefined state transition manner to reduce the test search overhead. In [9] a pattern based approach for fault testing based on state transition minimization is defined. The approach defined a pre flow of testing sequence using unique state transition for minimizing the fault test transitions. A CRC based approach defined in [10] was outlined in to define the error correction logic in fault diagnosis. In [11] a low cost fault test optimization is developed. In [12] an approach defines the ASIC based fault testing in Digital circuitry. A eight parallel bit pattern sequence was outlined in [13] to minimize the fault testing overhead. wherein methods were developed for test Power minimization by reducing the scan effort or the pattern sequencing, the minimization of test pattern by intelligence approach is to be developed to give the best suited test sequence with minimal testing overhead. The conventional approaches were optimized in consideration of a single parameter of fault coverage, however the reliability of the test pattern in fault testing is not been evaluated. In this paper, a new multi attribute test pattern generation using the pattern sequencing is developed. the rest of the paper, is outlined in 6 section. Section 2 outline the test pattern generation, section 3 present the approach of intelligent test pattern optimization using decision approach based on fault coverage density. Section 4 present the simulation result of the proposed work, and section 5 present the conclusion of the presented work.

II. TEST PATTERN ALIGNMENT

A good fault testing approach must be computationally efficient with accurate detection of defect behaviors. Generally, detection of all faults through one single fault model is not possible. Fault models are of two types, single fault model and multiple fault models. Single fault model is defined for circuit with 1 fault value; multiple fault modelsare defined for circuit with multiple faults in a CUT. In addition to single and multiple fault models, an equivalent fault model is also used. In such fault model, two

Revised Manuscript Received on December 22, 2018.

Y.Sreenivasula Goud, Department of ECE, Ravindra college of Engineering for women, Kurnool, AP, India.

Dr.B.K.Madhavi, Department of ECE, Sreedevi women's engineering college, Hyderabad, Telangana, India.

different fault locations illustrate identical fault behavior for all input patterns. In system level testing the faults considered for testing is stuck-at faults 0 or 1. At the transistor level stuck-short or stuck-open faults are observed. Wherein stuck-open condition, the output voltage is observed to be retaining the last result value, stuck-short is caused due to shorting of V_{DD} to V_{SS}. In addition to these faults, a Bridging fault is observed, where a short is observed at the adjacent wires. To detect these faults automatic test equipment (ATE) were used. ATE consists of an ATPG unit, a UUT unit and a Response analyzer (RA) unit. In the analysis of test faults in digital circuit, a single and multiple faults diagnosis is developed. Test patterns were developed with the objective of fault detection using the Linear feedback shift register (LFSR) with XOR logical gates were used in for random pattern generation. A polynomial equation defining the LFSR operation given as $F = p^4 + p + 1$ for a 5 bit LFSR. The pattern bit in the LFSR is iterated in a random sequence and a feedback shift operation is made in random pattern selection. The random pattern generator uses the dynamic shift operation in a linear fashion in generating the test pattern. each of the test pattern is buffered and passed as a test sequence for fault detection. The count of this random sequence is very large in many complex test circuitry, which leads to large delay in fault testing. The redundant pattern in test sequence result in high power dissipation. To minimize the power consumption, in this paper a decision based approach using dual decision metric of fault density coverage and fault reliability factor is developed. This approach gives a significant pattern selection.

III. MULTI-OBJECTIVE PATTERN SEQUENCING

In the approach of test pattern optimization a correct pattern selection is a major need. This approach, defines the selection of pattern using decision based logic using the multi attribute factor and pattern alignment following genetic and ANT optimization technique. The optimization approach, defines the decision function as a recursive decision operation given as, a bit swap and block swap method . A random selection of the data block for the pattern generation as observed lead to overhead. In the process of bit pattern selection, the optimization function is controlled via a toggling value between each bit in a block considered. To optimist the position of each bit in constraint to the converging factor, each information bit is considered as a particle in iterations is used to determine new particles. The proposed bit optimization algorithm is as presented below,

Algorithm: Multi attribute patterns selection

Step1 Buffered test patterns are selected as the primary aligned pattern.

Step 2 Each of the pattern combination is computed for the fitness metric.

Step 3 Each of the test sequence is defined by a multi attribute fitness factor given by,

$$faultdetectionefficiency = \frac{numberofdetectedfaults}{totalnumberoffaults - numberofundetectablefaults} \quad (1)$$

and the reliability factor defined as the probability of the system operating normal for a time t, given as,

$$P(T_n > t) = e^{-\lambda t} \quad (2)$$

where λ is the failure rate define as the sum of all individual failure rates,

$$\lambda = \sum_{i=0}^{k} \lambda_i \ (3)$$

Step 4 The two simulative parameters are tuned for the maximization function.

Step 5 The patterns are shuffled for each iteration and best fitness factor is derived.

The pattern selection has the benefit of test pattern optimization giving maximum fault coverage with higher reliability factor. To optimize the pattern selection and validate over the test circuit, a simulation is performed as outlined below.

IV. SIMULATION RESULT

Towards realizing the suggested approach, an ATE unit was developed. The unit was developed with three basic block units of Automatic Test Pattern Generation (ATPG), Unit Under Test (UUT) and Output Response Analyzer (ORA). To define the suggested architecture a HDL definition of these units are developed using VHDL language. In the present test, two different logic were chosen, The fault diagnosis were developed for a struck at -0 and stuck-at -1 fault. The logical circuits considered for the fault testing is presented in figure 1,2 respectively. These approaches were taken for the testing of long, short and global signaling faults.

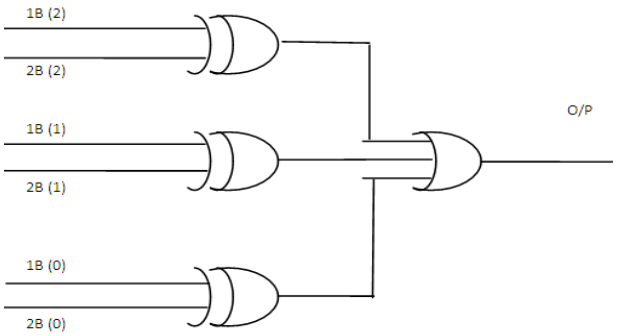

Figure 1: Digital circuitry for fault test analysis .

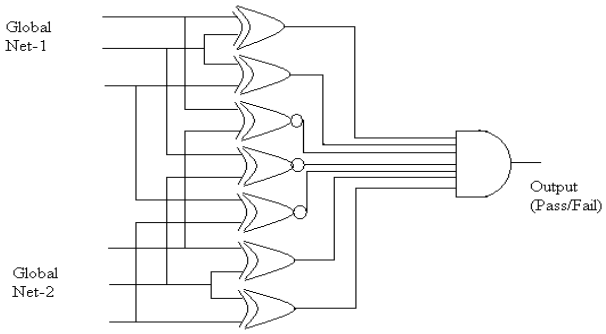

Figure 2: Response Analyzer for the fault diagnosis

The simulation result obtained is as illustrated below.

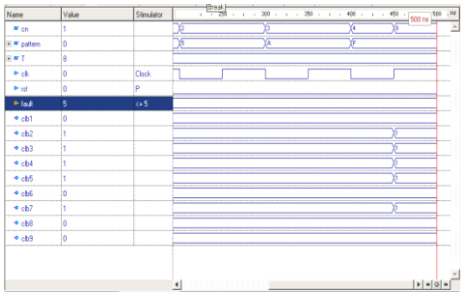

Figure 3: Result for the fault detection with 1 line fault.

The timing result for the test scan of the implemented architecture is presented in Figure 3. To test interconnects, a test pattern is generated. These test patterns are generated using a cascaded 2 bit counter logic, to generate alternate and continuous test bits, towards fault testing. The interconnect faults are observed at each scan level and the result is buffered at the corresponding fault locations. The fault signal is used to record the total faults encountered during the testing scan.

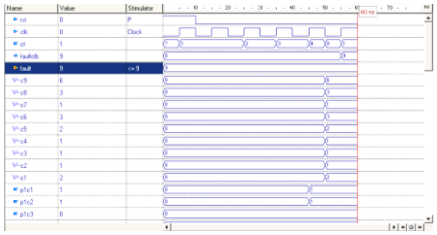

Figure 4: Result for the fault detection developed approach multiple line.

On the completion of test scans over a faulty circuit interconnects the accumulated fault count is observed to define the measuring metric. The faults in this case is propagated due to the bridging of interconnection observed at different fault location in the test circuitry.

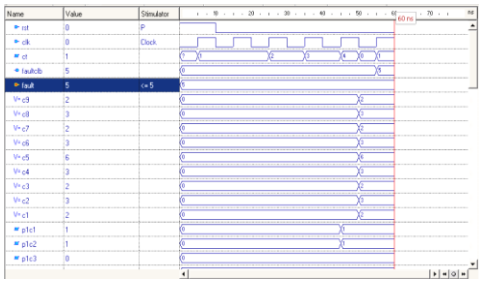

Figure 5: Result for fault with metric count

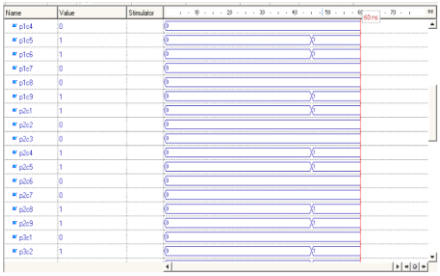

Figure 6: Result for the fault detection with multiple fault metric count

The analysis of the fault density and it reliability factor is presented in table 1.

Table 1: Reliability factor of the developed fault test approach

Fault coverage (%)	40	50	60	70	80	90
Fault Reliability (%)	67	79.8	81.7	89.7	93.6	96.6

The device utilization for the develop approach is outlined in figure 7 below. To realize the implement approach over a programmable device, a FPGA device of Xilinx is chosen and developed code is targeted to observe the implementation requirement. The logical requirement for the developed approach is presented in figure 7.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	113	88,192	1%	
Number of 4 input LUTs	123	88,192	1%	
Logic Distribution				
Number of occupied Slices	134	44,096	1%	
Number of Slices containing only related logic	134	134	100%	
Number of Slices containing unrelated logic	0	134	0%	
Total Number of 4 input LUTs	261	88,192	1%	
Number used as logic	123			
Number used as a route-thru	138			
Number of bonded IOBs	34	1,164	2%	
IOB Flip Flops	14			
Number of PPC405s	0	2	0%	
Number of GCLKs	1	16	6%	
Number of GTs	0	20	0%	
Number of GT10s	0	0	0%	
Total equivalent gate count for design	2,633			
Additional JTAG gate count for IOBs	1,632			

Figure 7: Summarized synthesis report for the developed estimation system.

Timing report for the implementation is observed as,

Minimum period: 7.693ns (Maximum Frequency: 129.984MHz)

Minimum input arrival time before clock: 2.423ns

Maximum output required time after clock: 3.113ns

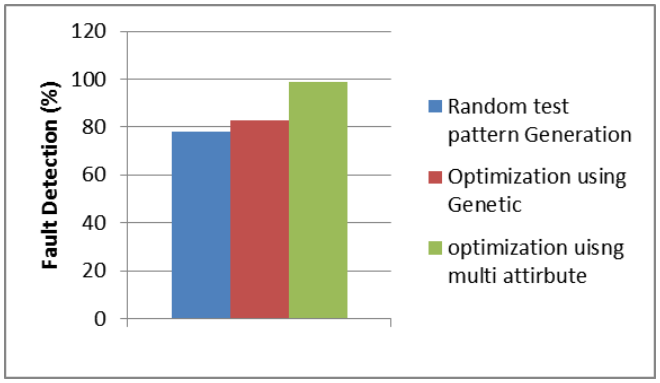

Figure 8: Comparative plot for fault detection coverage for the developed approach

The observed result illustrated an higher fault coverage probability from the random and genetic based fault test pattern optimization.

V. CONCLUSION

This paper develop a new multi attribute test pattern optimization using decision logic. A multi attribute pattern using fault reliability factor and fault coverage density. The

optimization using past approaches were minimized using the pattern sequencing or decision approach. However, the decisions were developed with a primal objective of minimizing the fault test patterns. No effort were made in observing the test pattern reliability or fault coverage. This limitation is overcome by developing a multi attribute monitoring and decision approach.

VI. REFERENCE

[1] C Guerin, V Huard, A Bravaix, "The Energy-Driven Hot-Carrier Degradation Modes of nMOSFETs", IEEE Transactions on Device and Materials Reliability, Volume 7, Issue 2, June 2007, pp.225-235.

[2] J Lienig, G Jerke, "Electro migration - a tutorial introduction", International Journal of Electronics, Volume 69, Issue 3, 1990, pp. 333-338.

[3] K P Cheung, "Can TDDB continue to serve as reliability test method for advance gate dielectric", International Conference on Integrated Circuit Design and Technology, October 2004, pp 345-348.

[4] Parag K. Lala, "Fault Tolerant and Fault Testable Hardware Design", Prentice Hall International, 1984, p. 263.

[5] Z. K. Baker and V. K. Prasanna, "High-throughput linked-state matching for intrusion detection systems," in Proc. Symp. Arch. For Netw. Commun. Syst. (ANCS), Oct. 2005, pp. 193–202.

[6] Y. H. Cho and W. H. Mangione-Smith, "A state matching co-processor for network security," in Proc. 42ndIEEE/ACM Des. Autom. Conf., Anaheim, CA, Jun. 13–17, 2005, pp. 234–239.

[7] Y. H. Cho and W. H. Mangione-Smith, "Fast reconfiguring deep packet filter for 1+Gigabyte Network," in Proc. 13th Ann. IEEE Symp. Field Program. Custom Comput. Mach. (FCCM), 2005, pp. 215–224.

[8] C. R. Clark and D. E. Schimmel, "Scalable state matching on high speed networks," in Proc. 12th Ann. IEEE Symp. Field Program. Custom Comput. Mach. (FCCM), 2004, pp. 249–257.

[9] S. Dharmapurikar and J. Lockwood, "Fast and scalable state matching for content filtering," in Proc. Symp. Arch. for Netw. Commun. Syst. (ANCS), Oct. 2005, pp. 183–192.

[10] M. Roesch, "Snort- lightweight intrusion detection for networks," in Proc. 15th Syst. Administration Conf. (LISA), 1999, pp. 229–238.

[11] P. Piyachon and Y. Luo, "Design of high performance state matching engine through compact deterministic finite automata," in Proc. 42nd IEEE/ACM Des. Autom. Conf., 2008, pp. 852–857.

[12] M. Gokhale, D. Dubois, A. Dubois, M. Boorman, S. Poole, and V. H. Granidt, "Towards gigabit rate network intrusion detection," in Proc. the Eleventh Annual ACM/SIGDA International Conference on Field- Programmable Logic and Applications (FPL '03), 2002, pp. 404–413.

[13] R. Sidhu and V. K. Prasanna, "Fast regular expression matching using FPGAS," in Proc. 9th Ann. IEEE Symp. Field-Program. Custom Comput. Mach. (FCCM), 2001, pp. 227–238.