Strained Si/SiGe/Si Nano-Channel HOI MOSFET

Lalthanpuii Khiangte, Rudra Sankar Dhar

Abstract— Strained Si technology has headed in the development of single or dual channel strained silicon MOSFETs devices. Comprehending the need of advancement in recent technologies with miniaturized features, developing a novel MOSFET on ultrathin double strained Si with strained SiGe sandwiched in between and forming a tri-channel MOSFET has been the crux of this present research. Incorporation of quantum carrier confinement effect on the ultrathin dual strained Si layers in the channel has been implemented to counterbalance the threshold voltage roll-off induced by the strained layers. A comparison of the conventional strained silicon on relaxed silicon-germanium with double strained silicon channel MOSFET has been perceived leading to eloquent drain current enhancement of ~49% with a small reduction in the threshold voltage caused by the additional bottom strained Si layer. Further, 100nm and 50nm channel length have been compared and a superior device characteristic for the reduced device dimension is attained as the prominence of velocity overshoot is more in short channel device approaching to quasi-ballistic transport in the channel region.

Keywords— double strained Si; SOI; strained SiGe velocity overshoot; threshold voltage; MOSFET; HOI; transconductance (gmmax); quantum confinement; DIBL.

1. INTRODUCTION

A considerable amount of attention has been given to strained technology in the last decade for its ability to enhance carrier mobility and drive current for MOSFETs [1]. Literature suggested beneficial stress techniques for n-MOSFETs such as: (a) globally strained substrate, (b) stress memorization technique, and (c) tensile overlayer [2]-[9] and various structures of strained device with Si/SiGe material developed as: (1) Strained silicon (s-Si) on relaxed SiGe, (2) s-Si/strained SiGe (s-SiGe) dual channel layer, (3) direct s-Si on insulator and (4) Heterostructure on insulator (HOI) or on bulk [10]. Strain techniques does not compromise long term reliability aspects and has only a marginal impact on the quality of gate oxide has been validated [11]. But, a major concern with strained Si is the reduction of threshold voltage (V_{th}) which occurs due to decrease in band gap with increase in strain. On this account, detailed investigations suggested that for s-Si layer thickness of ~3nm, the benefits of using higher Ge mole fraction can be retained while maintaining the V_{th} reasonably large [12][13]. Hence, $Si_{1-x}Ge_x$ forms a better option for the dual channel MOSFETs.

This paper is focused on the development of a novel double strained Si channel heterostructure on insulator MOSFET featuring an additional bottom strained Si layer in the channel region which sandwiches $Si_{1-x}Ge_x$ between making a distinguished structure than the conventional single strained Si SOI MOSFET, resulting in an enhanced drain current. An in-depth study and analysis of double strained Si channel MOSFET in nano-regime has been performed, where drain current, and transconductance enhancements are compared for 100nm and 50nm channel length devices. Physics of velocity overshoot effect has also been analyzed for 50nm channel length HOI MOSFET, which elucidated carriers approaching the quasi-ballistic transport.

II. DEVICE STRUCTURE

Incubating the benefits of SOI MOSFET with the ability to enhance carrier mobility by strained Si technology[15]-[20], doubly due to the additional s-Si layer discriminates this novel device structure and its superior characteristics to the conventional device (single s-Si MOSFET). Fig. 1 exemplifies the two s-Si layers which are introduced in the channel region for the first time, sandwiching the SiGe layer, hence crafting a strained SiGe layer. This novel device structure thus consists of a tri-layered channel forming the heterostructure-on-insulator (HOI) MOSFET. To fabricate heterostructure on insulator MOSFET, strained Si, strained $Si_{1-x}Ge_x$, each layer is grown respectively on the relaxed $Si_{1-y}Ge_y$ layer and transferred to the insulator preserving the original strain state. Ultrathin strained Si surface layer of ~2nm thick has been employed so that holes are not entirely confined at the surface, resulting in reduced influence of higher Ge content on the s-Si layer with this advancement these two s-Si layers formed the quantum well for carrier confinement. With parameters listed in Table 1, two devices have been designed: Device A -100nm, and Device B-50nm gate length double s-Si channel along with the conventional device-single s-Si specified as in [12].

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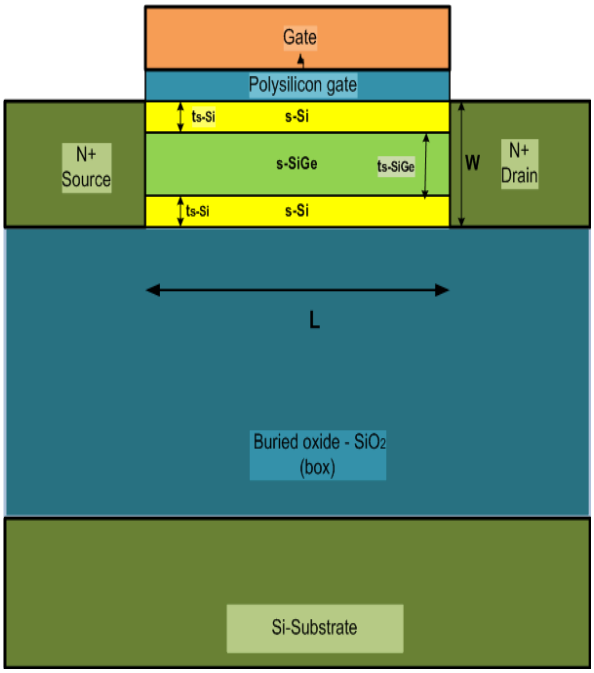

Fig. 1. Double s-Si with s-SiGe HOI MOSFET

TABLE I. DEVICE PARAMETERS

Parameters	Values
Channel Length (L)	50nm, 100 nm
Ge mole fraction	0.4
s-Si layer thickness ($t_{s\text{-}Si}$)	2 nm
Gate Oxide thickness	2 nm
Source/Drain doping (N_D)	10^{19} cm^{-3}
channel doping (N_A)	10^{16} cm^{-3}
Drain bias (V_{DS})	50mV

III. RESULTS AND DISCUSSION

Using device parameters tabulated in Table I, simulation of the device structure shown in Fig.1 by 2D SYNOPSIS Sentaurus TCAD tool [22], [23], incorporating multi-valley model for both band structure and electron mobility [23] for strained induced band gap reduction and change in electron mobility respectively. Quantization effects were accounted by the 1D Schrodinger model [23] in which the Schrodinger and Poisson's equations were solved simultaneously on the non-local-mesh created between the s-Si and the dielectric interfaces. Drain current enhancement of ~49% was observed for Device A at 50mV drain-source voltage as shown in Fig. 2. over the conventional device which is essentially due additional strained Si layers in the channel region, favorable for the increment of electrons with enhanced mobility

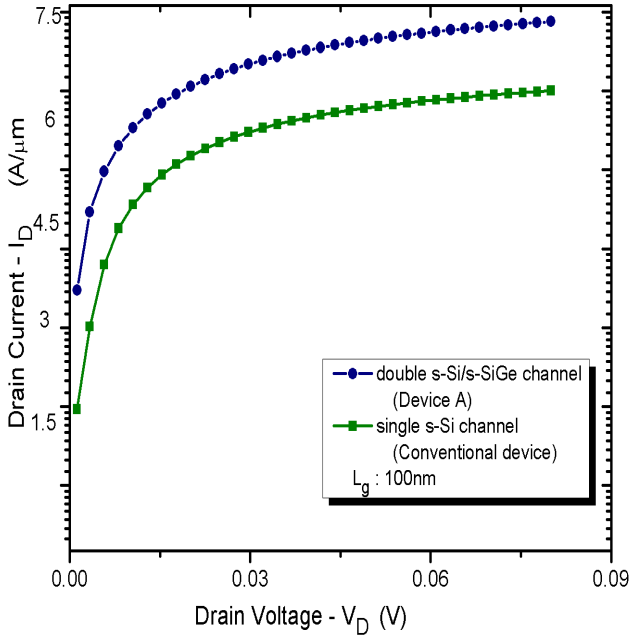

Fig. 2. I_D-V_D characteristics depicting 49% enhancement in drive current for 100nm channel length HOI MOSFET over 100nm channel length Conventional devices

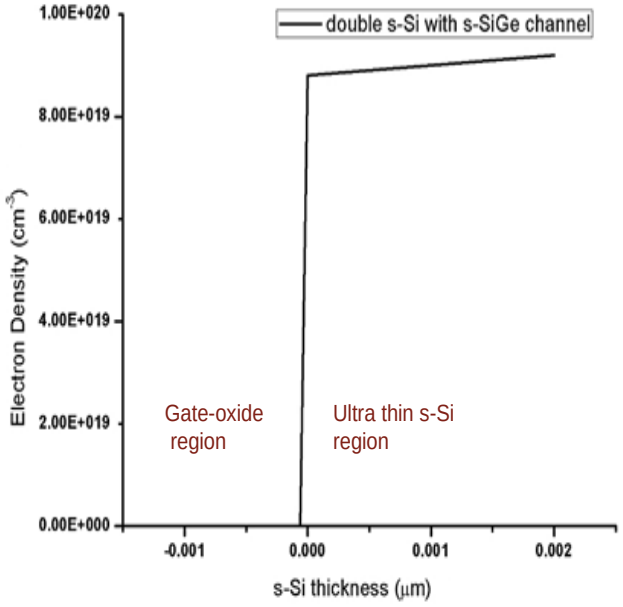

Fig. 3. Carriers confinement in the ultrathin s-Si layer of Device A (100nm double s-Si HOI MOSFET)

Trace of carrier confinement in the s-Si layer was obtained as illustrated in Fig. 3 due to the quantization effect. Thus, energy band gap increased balancing the threshold voltage roll-off due to strained layers. A clear insight of velocity overshoot [24] being more prominent in reduced channel length is depicted in Fig. 4.

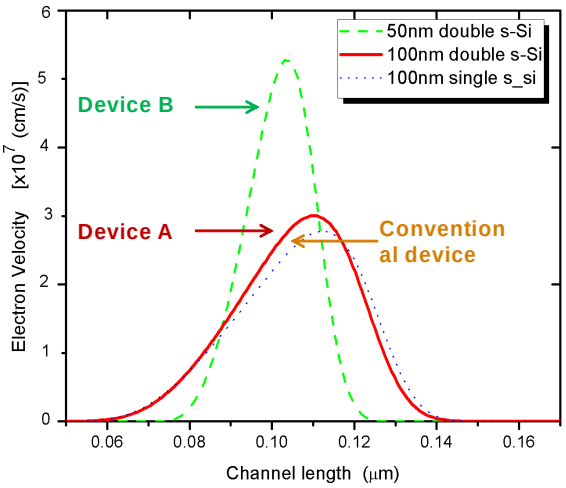

Fig. 4. Electron velocity variation along the channel length compared between Device-A, Device-B and single s-Si channel MOSFETs.

With the reduction of channel length and increased in lateral electric field in Device-B the velocity overshoot condition is acquired i.e. non-equivalence of momentum relaxation time and energy relaxation time, result in low scattering and carriers do not have time to heat up. The electron velocity becomes greater than the saturation velocity. Hence, carrier transport approaches quasi-ballistic in nature result in drain current enhancement ($\Delta I_D = (I_D^{50nm\ double\ s\text{-}Si} - I_D^{100nm\ double\ s\text{-}Si})/I_D^{100nm\ double\ s\text{-}Si}$) of ~41.3% for Device-B (50nm channel length) in comparison to Device-A (100nm channel length) as shown in Fig. 5.

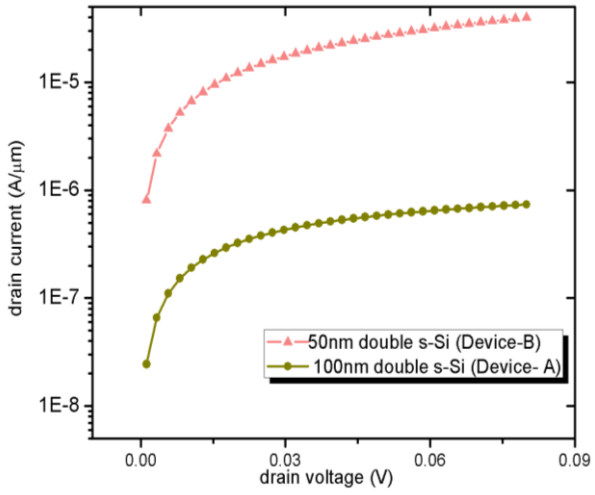

Fig. 5. I_D-V_D characteristics depicting 41.3% enhancement in drive current for 50nm channel length over 100nm channel length in HOI MOSFET devices

Distinct view about the short channel effects are exemplified by Fig.6 in which threshold voltage and DIBL and transconductance (gmmax) variation as a function DIBL has been obtained for each of the three devices (Device A, Device-B and Conventional Device). A 25.25% threshold voltage roll has been attained in 50nm channel length in comparison to 100nm channel length for double s-Si MOSFET with a higher DIBL. A remarkable increase in transconductance is achieved featuring velocity overshoot [25], which is a tradeoff between transconductance and DIBL observed due to the short channel effects in the HOI MOSFET devices.

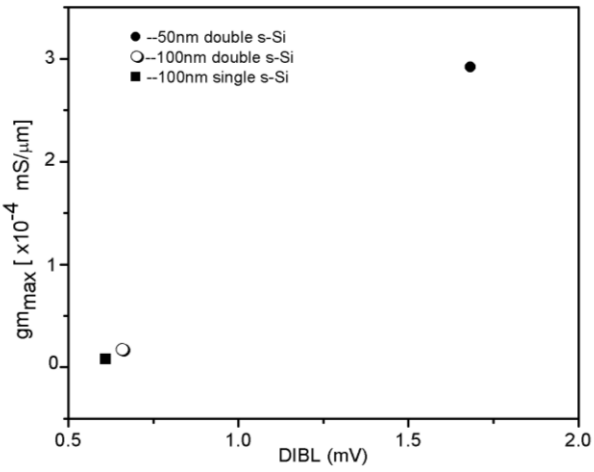

Fig. 6. Transconductance (gm_{max}) as a function of DIBL for Device-A, Device-B and Conventional.

IV. CONCLUSION

Double strained Si layers in the channel region of Heterostructure on Insulator MOSFET have been developed and analyzed. With intrusion of the additional strained Si layer in the channel region an eloquent drain current enhancement of 49.3% has been obtained for 100nm channel length device in comparison to the single s-Si SOI MOSFET device. Velocity overshoot has been perceived in the sub 100nm device (Device B) resulting in improved drive current along with high gmmax attained in the 50nm short channel length device. Increased transconductance in this short channel-MOSFET was observed due to the effect of velocity overshoot experiencing ballistic carrier transport within the channel of the HOI MOSFET.

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