Theoretical Analysis of CMOS circuits in 90 nm Technology

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Abstract: ***In this paper a novel design of 1-bit CMOS full adder cell using XNOR gate and Multiplexer, This paper CMOS not gate and full adder calculate the theoretical value of dynamic power, leakage power, load capacitance, percentage error and switching activity., The results show that the proposed technique in terms of power consumption, delay are used in 90 nm technology***

Keywords: Dynamic power, load capacitance, switching activity, leakage power

I. LITERATURE SURVEY:

As demand for transportable product is increasing the requirement for low-power style is changing into a significant issue in high performance digital systems, like microprocessors, digital signal processors (DSPs) and alternative applications. Increasing chip density and better in operation speed cause the planning of terribly advanced chips with high clock frequencies. Low power style of VLSI circuits has been known as a essential technological would like in recent years because of the high demand for transportable client physical science product [1-5] 1 bit CMOS Full Adder circuits are wide extend in horribly considerable Scale Integration (VLSI) systems and are utilized in numerous Arithmetic and Logic Applications Viz. addition, subtraction and multiplication. Adders become integral realistic block in Digital signal process, Image process and Microprocessors applications and that they conjointly kind the very important electronic equipment of a mainframe, floating range of transistors, chip area, power dissipation, that has raised the obligation for low power and high speed, high performance and to space circuits [6-8]. the 1-bit CMOS full adder purpose unit ,cache and operation unit. the arrangement and also the recital of the total Adder circuits are supported circuits profit was ascertained, the circuit occupies low space, consumes low power and operates at lower in operation voltage. it's tough and even obsolete to stay full voltage swing operations the styles think about few transistors for low power consumption. [9]

As demand for Portable products is increasing the need for low-power design is becoming a major issue in high performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications. Increasing chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. Low power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products [1-5] 1-bit Full Adder circuits are admired in Very Large Scale Integration (VLSI) systems and have been in employment in different Arithmetic and Logic Applications Viz. addition, subtraction and multiplication. Adders have become integral functional block in DSP, Digital Image processing and Microprocessors applications and they also form the significant circuitry of a Central Processing unit, floating point unit, cache and memory access unit. The circuit design and the performance of the CNOS full Adder circuits are based on number of transistors, IC chip area, power dissipation [6-8]. The 1-bit CMOS full adder circuit was observed, the Full adder circuit occupies low area, less power consumption and it operates at lower operating voltage. It is not easy and even out of date to keep full voltage swing operations the designs considers a small number of transistors for less power consumption. [9]

II. PROPOSED WORK AND SIMULATION RESULTS:

3.1 Proposed1 CMOS NOT gate

3.1.1Theoretical analysis of CMOS NOT gate circuit [2-9]

In 90 nm Technology varying theoretical parameter for CMOS circuits are

nMOS transistor

Table 1 nMOS transistor Vt

MOS Current	Normal Vt	High Vt	Low Vt
I_{on}	0.68 mA	0.63 mA	0.74 mA
I_{off}	165 nA	30 nA	300 nA

pMOS transistor

Table 2 pMOS transistor Vt

MOS Current	Normal Vt	High Vt	Low Vt
I_{on}	0.37mA	0.35mA	0.39 mA
I_{off}	78 nA	21 nA	135 nA

Table 3 resistance value of MOSFET

NMOS MOS Current	Normal Vt	High Vt	Low Vt
I_{on}	1.7KΩ	1.9KΩ	1.6KΩ
I_{off}	22MΩ	40MΩ	4MΩ
PMOS MOS Current	Normal vt	High vt	Low vt
I_{on}	3.2KΩ	3.4KΩ	3.0KΩ
I_{off}	72MΩ	57MΩ	88MΩ

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Table 4 W/L ratio of nMOS and pMOS

Channel dimensions	NMOS	PMOS
W	1.2 µm	3 µm
L	0.1 µm	0.1 µm

Theoretical calculation of dynamic power

$$P_{total} = P_{Dynamic} + P_{Leakage}$$

$$P_{Dynamic} = 0.5V_{DD}^2.f.C.N$$

$$P_{leakage} = V_{DD}I_{leakage}$$

Where,
V_{DD}= power supply
f =clock frequency
C_L=load capacitance
N =switching activity

3.1.2 Calculation of CMOS NOT gate dynamic power:

The Dynamic power for CMOS gate is represented below which the Eq. is shown above [2-9]

$$P_{Dynamic} = 0.5V_{DD}^2.f.C.N$$

N=?, C_L=?

Considering NOT gate for calculation of the dynamic power, the truth table is represented in Table 5[2-9]

Table 5 truth table of NOT gate

Input	Output
0	1
1	0

N = Switching activity
P = no of inputs (1)
Q = number of zeros enter in output Colum (1)
N_{0-1}= Q. (2^P-Q)/ (2^{2P})
N_{0-1} = 0.25

3.1.3 Gate capacitance per unit area (C_{ox})

Cox = $\epsilon_o \epsilon_r$ / Tox,
ϵ_o = 8.854*10 -12 ; (F/m) permittivity of medium
T_{ox} =2. 05*10^{-9} ; effective oxide thickness (gate)
ϵ_r = 3.9 ; relative permittivity of sio2
C_{ox}= (3.9*8.854*10^{-12}) /(2.05*10^{-9}) = 15*10^{-3} Farads

3.1.4. Gate capacitance (Cg)

Cg= (W.L.C_{OX}) ---NMOS
Cg = (1.2*10^{-6}*0.1*10^{-6}*15*10^{-3}),
Cg = (3*10^{-6}*0.1*10^{-6}*15*10^{-3}), --PMOS
Cg = 1.8*10^{-15} F --- NMOS
Cg = 5.4*10^{-15} F ---PMOS
(3/2) Cg = 2.7*10^{-15} F----NMOS
(3/2) Cg = 8.1*10^{-15} F-PMOS

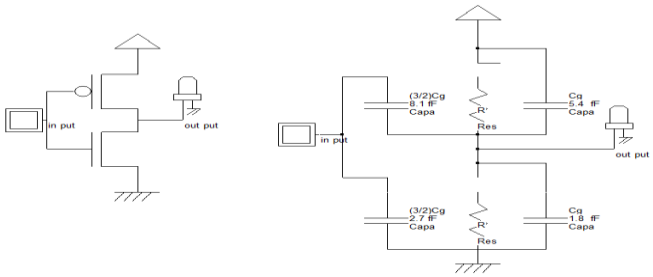


Fig.3 Resistance and capacitance of CMOS NOT gate

N=0.25, VDD=1.2v,

Total Load Capacitance=2.2 Ff,
Time period= 5ns, f =1/T
P_D =0.5* N f C_L V_{DD}^2
P_D =0.5*0.25*2.2*10^{-15} * 0.200*10^9(1.2)^2
P_D=0.792*10^{-6} Watts

3.1.5. Leakage power ($V_{DD}.I_{leak}$)

Table.6 find the average resistance of leakage power

transistor	Input –low	Input-high
pmos	ON(3.2KΩ)	OFF(72MΩ)
nmos	OFF(22MΩ)	ON(1.7KΩ)
Total resistance	22MΩ	72MΩ

Average resistance= (22MΩ +72MΩ)/
=47 MΩ
I_{leak}=V_{DD} / R average
I_{leak}= 1.2 /47*10^6
Leakage power= $V_{DD}.I_{leak}$
P_{lea}=1.2*0.025*10^{-6}
P_{lea} =30*10^{-9} Watts

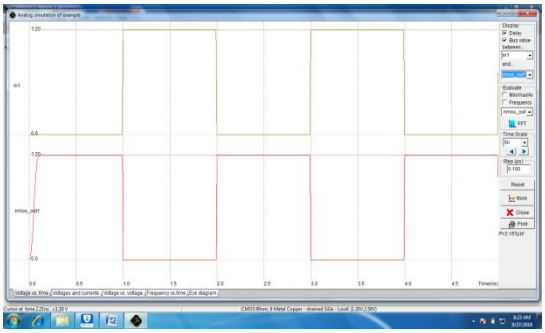
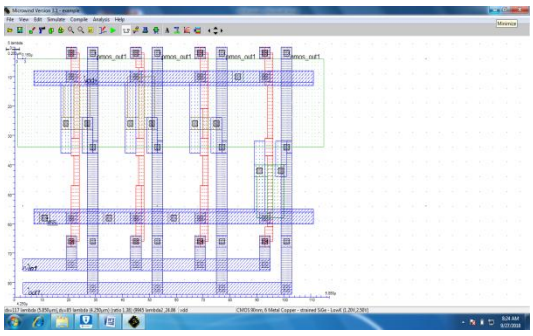


Fig.1 simulation results of CMOS NOT gate



3.2 Proposed 2 CMOS 10 T- Full Adder Model 1

The 10T full adder model1 is based on the following Boolean equations. The Boolean equations for the SUM and CARRY signals are given by Eq.1 and Eq..2. The gate implementation of 10T full adder is shown in Fig 4.1.

SUM = (A⊕ B) C^I+ (A ʘ B) C (1)
CARRY = (A ʘ B) A + (A⊕ B) C (2)

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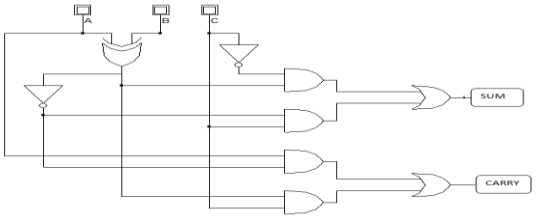

Fig 4 Gate level implementation of 10T Full Adder model 1

3.2.1 Derivation for SUM

The sum (SUM) output signal represents the summation result of the three input signals (A, B, Cin). The SUM equation of 10T full adder model 1 can be derived follows:

$SUM = AB^{I}C^{I} + A^{I}B^{I}C + ABC + A^{I}BC^{I}$

$SUM = C\,(A^{I}B^{I} + BA) + C^{I}\,(AB^{I} + A^{I}B)$

$SUM = (A \odot B)\,C + (A \oplus B)\,C^{I}$

3.2.2 Derivation for CARRY

The carry Eq. of 10T Full adder model1 can derived from the Eq. as follows.

$CARRY = AB + BC + CA$

$= AB\,(C + C^{I}) + AC\,(B + B^{I}) + BC\,(A + A^{I})$

$= ABC + ABC^{I} + ACB + ACB^{I} + BCA + BCA^{I}$

$= ABC + ABC^{I} + ACB^{I} + BCA^{I}$

$= AB\,(C + C^{I}) + C\,(AB^{I} + BA^{I})$

$= AB + (AB^{I} + BA^{I})\,C$

$= A\,(A^{I}B^{I} + AB) + (AB^{I} + BA^{I})\,C$

$CARRY = (A \odot B)\,A + (A \oplus B)\,C$

3.2.3 Modular Description

The 10T full adder is divided into three different modules based on functionality, they are namely

1. XOR and XNOR logic generation module
2. Sum generation module
3. Carry generation module

Fig 5 and 6 shows the block diagram of 10T- full adder model 1 in which the three different modules are separated.

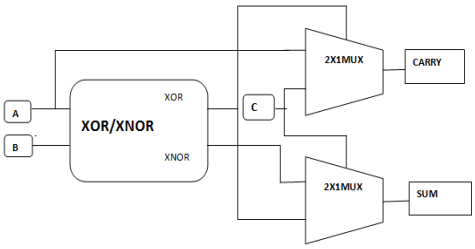

Fig 5 proposed 10T- Full Adder model 1 block diagram

3.2.4 XOR and XNOR logic generation

The XOR and XNOR logic generation is the first module in 10T full adder model 1 design. It is a logic gate which produces the XOR and XNOR output of two binary numbers. The output of this module is given to other modules in 10T- full adder model 1 for generation of sum and carry signal.

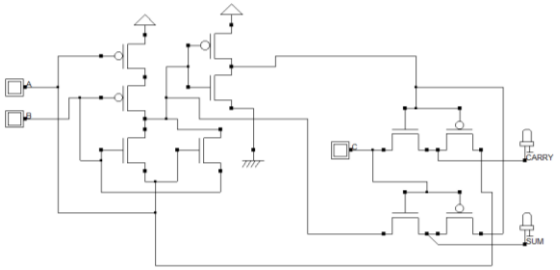

Fig 6 Module description of CMOS 10T-full adder model1 circuit

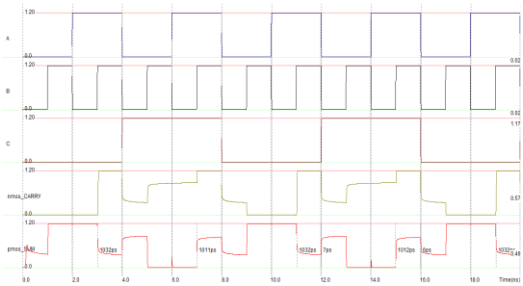

Fig.7 simulation result of proposed full adder model1

3.2.5. percentage of the error between simulation and theoretical results

We are calculating the percentage of error between simulation and theoretical results for the full adder model 5.

The Dynamic power in simulation is (E) =12 (µw)

The Dynamic power in theoretical is (T) =14 (µw)

Percentage of error = (|T-E|/T)*100%

= (14-12)/14

= 14%

Table 7 Comparison of theoretical and practical analysis of proposed full adder model and NOT gate.

Proposed models	Theoretical dynamic power (µw)	Theoretical leakage power (nw)	practical total power (µw)
CMOS NOT gate	0.792	30	3.187
10- Full adder model 1	14	23	12.28

III. CONCLUSION

This paper a novel design of a 1-bit CMOS full adder cell using two XNOR and one MUX, with reduced number of transistors In this paper CMOS not gate theoretical parameters are dynamic power has o.795(µw),theoretical leakage power has 30 nw ,theoretical load capacitance is 2.2 Ff, theoretical switching activity is 0.25 and full adder theoretical value of dynamic power is 14 (µw), leakage power is 23nw. The results show that the projected method in terms of power consumption, delay capacitance of load like parameters are used in 9onm technology

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