Performance Comparison for Ripple Carry Adder Using Various Logic Design

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Abstract--- CMOS transistors are extensively used in designing digital circuits. Transistor level design is an important aspect in any digital circuit designs particularly in full adders. Full adder is the basic part in any of the arithmetic circuits. FinFET is another technology that has a longer channel gate. Carbon Nanotube field effect transistor (CNTFET) is the most optimistic technology which is three terminal device similar to MOSFET. The semiconducting channel between the two contacts called drain and source consists of the nano tube. This paper presents Ripple carry adder (RCA) using static and dynamic logic styles with CMOS, FinFET and CNTFET technologies in 20nm technology with supply voltage of 0.9v and simulation is done by using Synopsys HSPICE Tool.

Index Terms - Ripple Carry Adder, Static and Dynamic Logic Styles, CNTFET, FinFET and HSPICE Tool.

1. INTRODUCTION

The increasing for low power very large scale integration (VLSI) can be addressed at different design levels, such as architectural, circuit, layout and the process technology level. Conventional CMOS logic style presents robustness against voltage scaling and high noise margins, so allowing a reliable operation at low voltages [1-5]. In this paper, a Ripple Carry Adder circuit using 1-bit full adder with CMOS, FinFET and CNTFET technologies has been designed with different low-voltage low-power logic styles i.e. static and dynamic logic styles and its propagation delay, dynamic and static power dissipation were taken and analyzed. The design is simulated using Synopsys HSPICE Tool at 20nm technology with supply voltage of 0.9v. This paper is structured as follows Section-II presents the Review of FinFET and CNTFET. Section-III represents about the Static and Dynamic logic styles. Section-IV tells about Design and analysis of Ripple Carry Adder using different logic styles. Section-V shows the results. Section-VI is done with the conclusion of the paper.

2. REVIEW OF FINFET AND CNTFET

As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the nanoscale. FinFETs are double-gate devices. The main challenges in this regime are twofold: (a) minimization of leakage current (Sub threshold þ gate leakage), and (b) reduction in the device-to-device variability to increase yield.

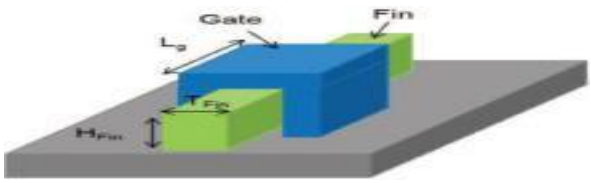

Fig 1: FinFET structure

Figure 1 shows the 3D structure of FinFETs and displays several of the most important FinFET parameters: height of the Fin (HFin), its width or body thickness (TFin), and FinFET channel length (Lg). Due to its structure FinFETs have several advantages including controlled fin body thickness, low threshold voltage variation and lower operating voltage. CNTFET is a sheet of hexagonal arranged carbon atoms rolled up in a tube of a few nanometers in diameter, which can be many microns long. These nanotubes are graphene strips rolled up into tabular shapes. Graphene is a single sheet of carbon atoms arranged in the well-known honey combination structure. The minimization has always a key role in electronic evolution; at each generation the miniaturization allows to obtain higher speed, lower power dissipation, lower costs and higher number of gates on chip. The below figure shows CNTFET structure same as CMOS.

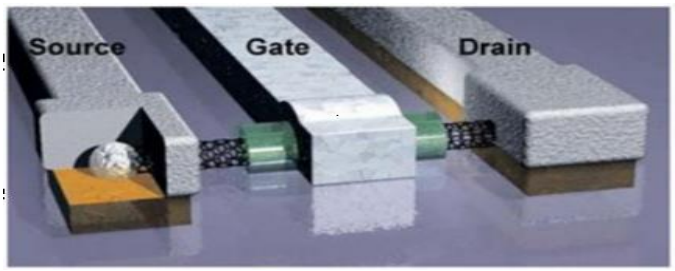

Fig 2: CNTFET structure same as CMOS structure.

3. STATIC AND DYNAMIC LOGIC STYLES

3.1 Static Logic Style

Static logic allows versatile implementation of logic functions based on static, or steady state behavior of simple CMOS structures. A typical static logic gate generates its output levels as long as the power supply is provided. Static logic design eliminates the precharging stage and thus reduces the extra power dissipation caused by clocking. There are three types of static logic styles: Full Static logic

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style, Complementary Pass Transistor (CPL) Logic Style, Double Complementary Pass Transistor (DPL) Logic Style.

3.1.1 Full Static Logic Style

The serial connections of the nMOS and pMOS transistors require increased width in order to acquire a reasonable conducting current to drive capacitive loads. This is because connecting the pMOS or nMOS devices in series can be visualized as a number of cascaded transistors. The delay time imposed by these devices is defined by

$$\text{Ŧ} = RC \qquad (1)$$

$$1/R \propto W/L \qquad (2)$$

Where, C is the capacitance, R is the resistance, L is the channel length, and W is the channel width, which is inversely proportional to R. Therefore, to minimize the delay time, W must be increased. Full static logic style XOR using CMOS, FinFET and CNTFET technologies are given in figures 3.1.1.(a)-(c)

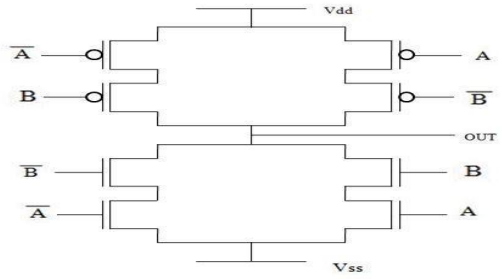

Fig 3.1.1(a): CMOS full static XOR.

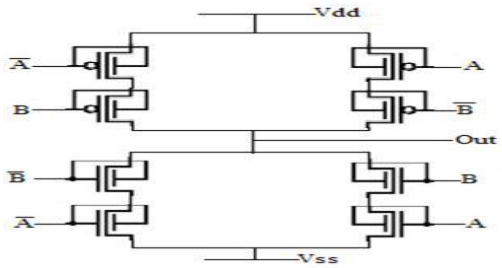

Fig 3.1.1(b): FinFET full static XOR.

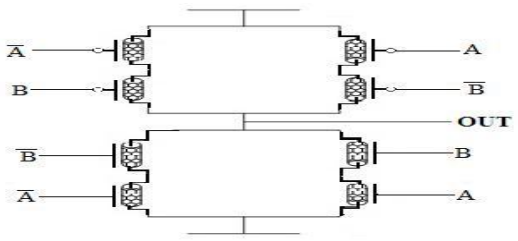

Fig 3.1.1(c): XOR implementation of CNTFET full static logic style.

3.1.2 CPL Logic Style

The major distinction between the pass-transistor logic family and the CMOS logic style is that the source node of the MOS transistor is connected to the input signals rather than to the power supply voltage. This logic eliminates the problem of vigilantly sizing the serial transistors, thereby requiring only half as many transistors as compared to the full static CMOS XOR gate. When the output of the nMOS pass transistor network at node X is logically high, at (VDD-VTh), where VTh is the threshold voltage, it causes a major setback by inducing an incomplete turn-off of the pMOS in the inverter; pMOS device is then coupled across the output of the inverter gate in order to pull up the output node X to full VDD. CPL logic style XOR using CMOS, FinFET and CNTFET technologies are given in figures 3.1.2(a) – (c).

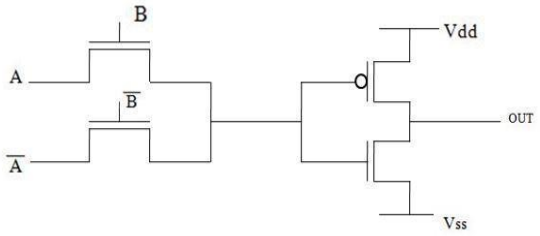

Fig 3.1.2(a): CMOS CPL XOR.

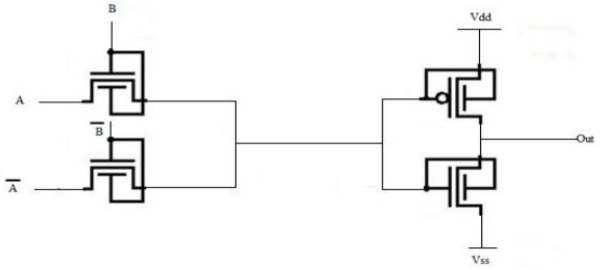

Fig 3.1.2(b): FinFET CPL XOR.

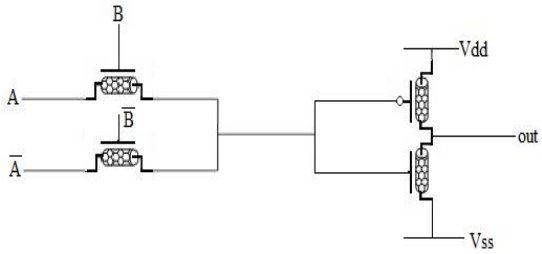

Fig 3.1.2(c): CNTFET CPL XOR.

3.1.3 DPL Logic Style

Another logic design that uses pass transistors is the DPL, which is a verification of the CPL the XOR gate using the DPL is depicted in fig: 3.1.3 (a) by using both the pMOS and nMOS devices, the DPL prevents the problem of the nMOS threshold voltage dropping in CPL logic design. The XOR gate using the DPL with an array of nMOS pass transistors using CMOS, FinFET and CNTFET technologies are given in figures 3.1.3(a) – (c).

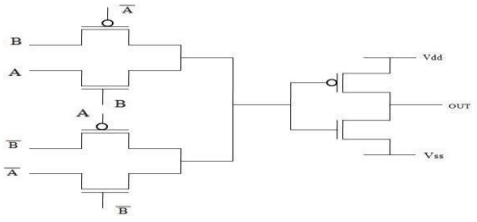

Fig 3.1.3(a): CMOS DPL XOR

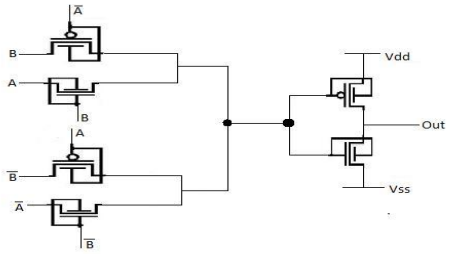

Fig 3.1.3(b): FinFET DPL XOR.

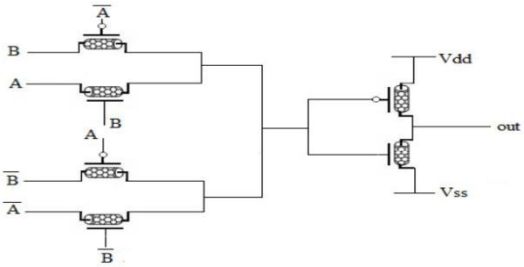

Fig 3.1.3(c): CNTFET DPL XOR.

3.2 Dynamic Logic Style

In high density, high performance digital implementations where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits offer several advantages over static logic circuits. The storage of all dynamic logic gates depend upon temporary storage of change in parasitic. Static CMOS offers good performance but cannot keep up with dynamic logic styles in terms of propagation delay. In contrast to the static gates design, dynamic gates are clocked and work in the precharge and evaluation phases. There are two types of dynamic logic styles: Double-rail domino dynamic logic style, Single-rail domino dynamic logic style.

3.2.1 Double-Rail Domino Dynamic Logic Style

Figure 3.2.1 (a) shows the double-rail Domino logic style utilized to construct the XOR gate. Contrary to static techniques, dynamic design requires a precharge and an evaluation phase. When the CLK signal is at low value, precharge stage occurs while the evaluation stage takes place when the CLK signal is at high value. Because of the precharge and evaluation phases, the dynamic design abolishes all the spurious transitions and its corresponding power consumption, which is intrinsically present in any static logic designs. Nevertheless, devices such as the clock driver actually dissipate additional power. Double-rail domino dynamic logic style using CMOS, FinFET and CNTFET technologies are given inn figure 3.2.1(a) – (c).

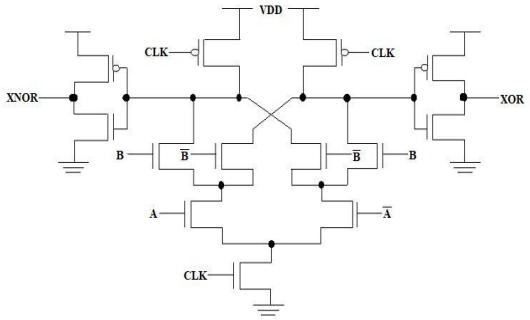

Fig 3.2.1(a): CMOS Double Rail Domino Dynamic logic XOR.

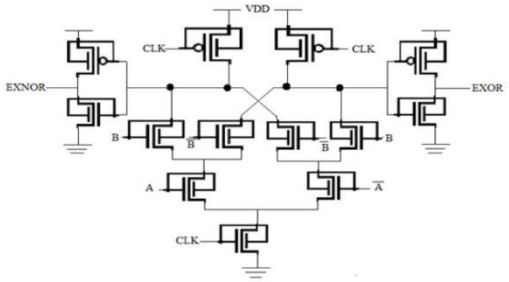

Fig 3.2.1(b): FinFET Double Rail Domino Dynamic logic XOR.

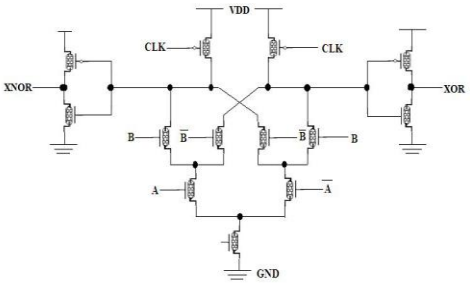

Fig 3.2.1(c): XOR implementation of CNTFET Double Rail Domino Dynamic logic XOR.

3.2.2 Single-Rail Domino Dynamic Logic Style

The double-rail inputs are only necessary for XOR/XNOR gate implementation. For other logic gate functions, such as NAND and NOR, the single-rail inputs are possible. Accordingly, power dissipation is alleviated. The XOR gate realization employing the single-rail domino dynamic logic is demonstrated using CMOS, FinFET and CNTFET technologies are given in Fig. 3.2.2(a) – (c)

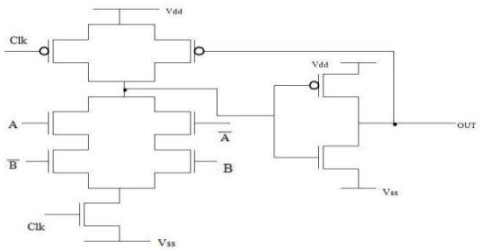

Fig 3.2.2(a): CMOS Single Rail Domino Dynamic logic XOR.

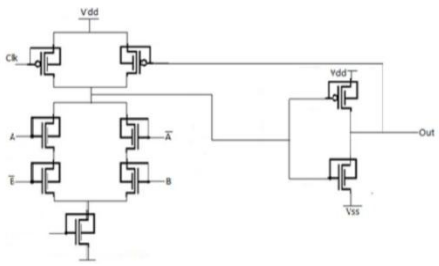

Fig 3.2.2(b): FinFET Single Rail Domino Dynamic logic XOR

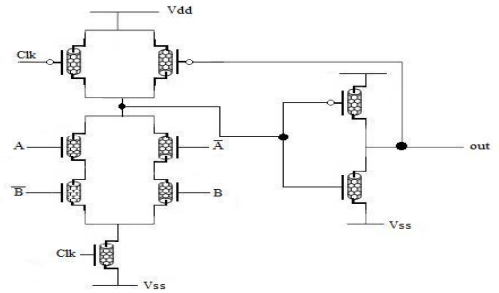

Fig 3.2.2(c): CNTFET Single Rail Domino Dynamic logic XOR

4. DESIGN AND ANALYSIS OF RIPPLE CARRY ADDER USING VARIOUS LOGIC DESIGNS (RCA)

Ripple Carry Adder (RCA) is designed using various logic styles such as Full Static logic, CPL logic, DPL logic, Double-rail logic and Single-rail logic, known as Full Static RCA, CPL RCA, DPL RCA, Double-rail RCA and Single-rail RCA respectively. The basic unit of RCA is a full adder. It can be extended indefinitely to any number by connecting the carry-out of the previous 1-bit FA to the carry-in of the next 1-bit FA. In this paper 4-bit RCA is designed using logic styles. A 4-bit RCA consisting of 4 single-bit FAs is described in Figure 4.

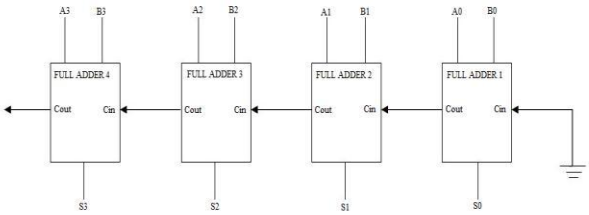

Fig 4: Block diagram of Ripple Carry Adder (RCA).

The figure 4 shows the 4-bit RCA where, individual full adder block contains two XOR gates. These XOR gates are replaced by logic styles like full static XOR, CPL XOR, DPL XOR, Double-rail domino dynamic XOR and Single-rail domino dynamic XOR and operation is performed. These logic styles are replaced in place of XOR in RCA and its performance comparison in terms of power and delay are analyzed using CMOS, FinFET and CNTFET technologies.

5. RESULTS

5.1 Analysis of CMOS, FinFET and CNTFET Based XOR Using Various Logic Styles

The design of XOR gates using various logic styles with CMOS, FinFET and CNTFET technologies which are discussed in section 4 are simulated and analyzed. These designs are simulated using Synopsys HSPICE tool at 20 nm technology with 0.9V supply [6-9]. The performance parameter values of propagation delay, dynamic and static power are tabulated in Table 1, Table 2 and Table 3 respectively. Simulation results of full static XOR, CPL XOR, DPL XOR, Double-rail XOR and Single-rail XOR are shown in figure 5.1, figure 5.2, figure 5.3, figure 5.4 and figure 5.5 respectively.

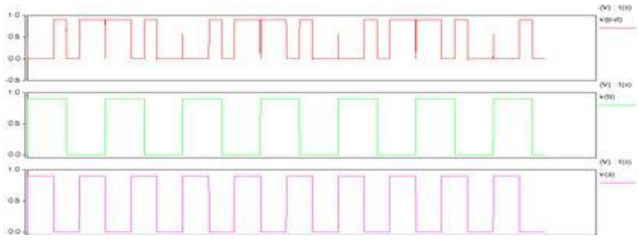

Fig 5.1: Output waveform of full static XOR Logic Style.

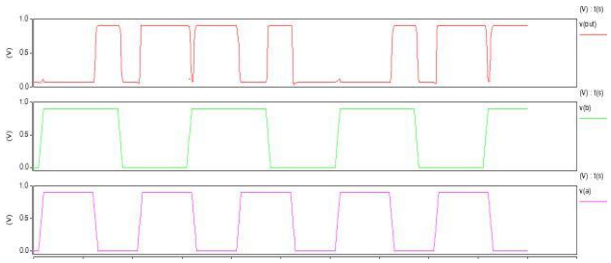

Fig: 5.2 Output waveform of CPL XOR Logic Style.

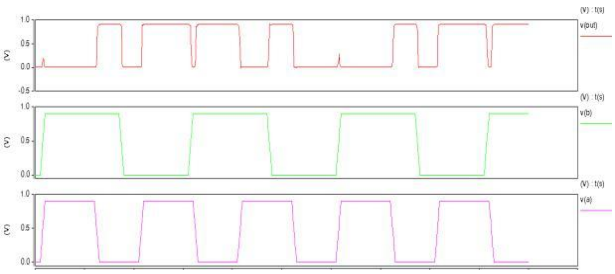

Fig 5.3: Output waveform of DPL XOR Logic.

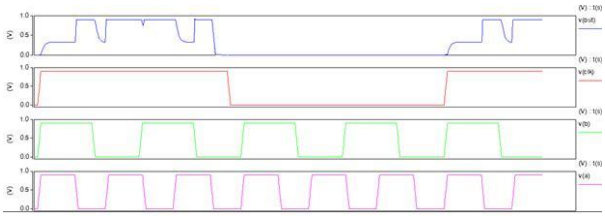

Fig 5.4: Output waveform of Single rail XOR Logic.

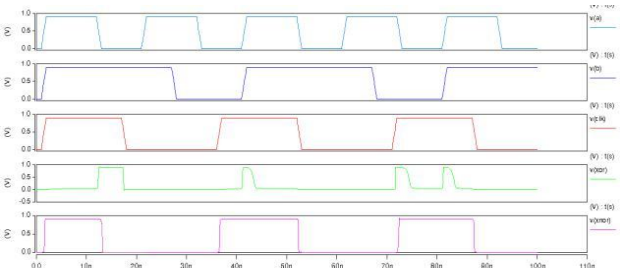

Fig 5.5: Output waveform of Double rail XOR Logic.

Table 1: Propagation Delay Comparison for three technologies.

Propagation Delay (Nano Sec)	CMOS	FINFET	CNTFET
Full Static XOR	0.024	0.147	0.021

CPL XOR	11.07	11.04	10.11
DPL XOR	19.93	11.21	11.02
Single rail XOR	10.75	10.95	10.11
Double rail XOR	11.04	10.80	10.12

Table 2: Dynamic power Comparison for three technologies.

Dynamic Power (Micro Watts)	CMOS	FINFET	CNTFET
Full Static XOR	0.41	7.16	0.131
CPL XOR	4.05	6.10	0.012
DPL XOR	1.09	6.94	0.159
Single rail XOR	6.03	28.1	0.015
Double rail XOR	2.57	20.8	0.017

Table 3: Static power Comparison for three technologies.

Static Power (Femto Watts)	CMOS	FINFET	CNTFET
Full Static XOR	8.29	143.3	2.63
CPL XOR	81.03	122.0	0.24
DPL XOR	21.96	138.9	3.18
Single Rail XOR	120.6	563.6	0.30
Double Rail XOR	51.53	417.7	0.35

5.2 Analysis of CMOS, FinFET and CNTFET Based RCA Using Various Logic Styles

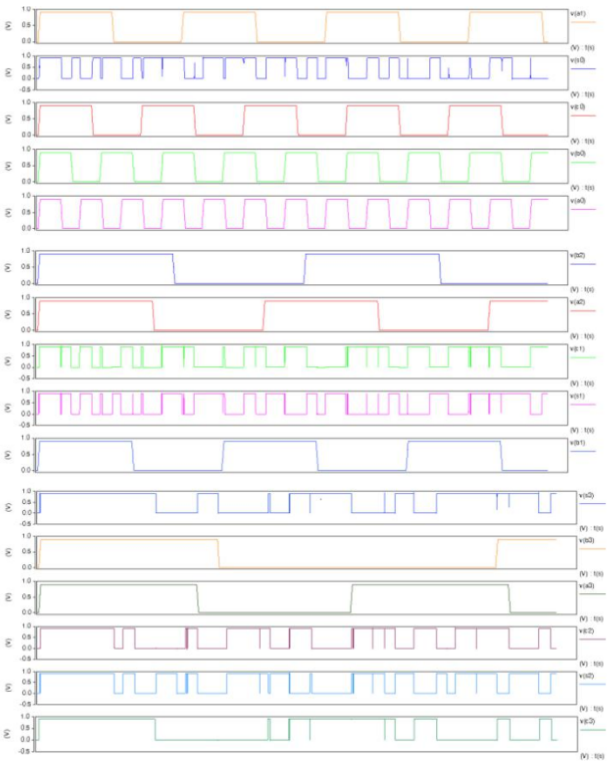

Fig 5.6: Output waveform of RCA using full static Logic.

RCA is implemented and analyzed using various logic styles with CMOS, FinFET and CNTFET technologies. These RCA designs are simulated using Synopsys HSPICE tool at 20 nm technology with 0.9V supply and the performance parameter values of propagation delay, dynamic and static power are tabulated in table4, table5, and table6 respectively. Simulation result of RCA using full static XOR is shown in figure 5.6

Table 4: Propagation Delay Comparison for RCA using three technologies.

Propagation Delay (Nano Sec)	CMOS	FINFET	CNTFET
Static XOR	79.5	0.068	0.022
CPL XOR	10.01	0.098	0.008
DPL XOR	10.04	0.063	0.017
Single rail XOR	4.30	0.129	0.029
Double rail XOR	0.041	0.018	0.014

Table 5: Dynamic power Comparison for RCA using three technologies.

Dynamic			

Power (Micro Watts)	CMOS	FINFET	CNTFET
Static XOR	9.48	9.08	0.113
CPL XOR	0.19	45.1	0.106
DPL XOR	4.85	46.9	0.108
Single rail XOR	50.4	7.94	0.092
Double rail XOR	156.8	170.9	0.082

Table 6: Static power Comparison for RCA using three technologies.

Static Power (Femto watts)	CMOS	FINFET	CNTFET
Static XOR	189.7	181.7	2.26
CPL XOR	3.94	903.6	2.13
DPL XOR	97.13	939	2.17
Single rail XOR	1008.1	158.8	1.85
Double rail XOR	3137.1	3419.3	1.65

CNTFET Full static RCA has 99% better speed performance than CMOS Full static RCA and 66% better speed performance than FinFET Full static RCA. CNTFET CPL RCA has 99% better speed performance than CMOS CPL RCA and 91% better speed performance than FinFET CPL RCA. DPL CNTFET RCA 99% better speed performance than CMOS DPL RCA and 72% better speed performance than FinFET DPL RCA. Single rail CNTFET RCA has 99% better speed performance than CMOS Full static RCA and 76% better speed performance than FinFET Single rail RCA. Double rail CNTFET RCA has 65% better speed performance than CMOS Double rail RCA and 18% better speed performance than FinFET Double rail RCA.

CNTFET Full static RCA has 98% less dynamic and static power dissipation than CMOS Full static RCA and 98% less dynamic and static power dissipation than FinFET Full static RCA. CPL CNTFET RCA has 45% less dynamic and static power dissipation than CMOS CPL RCA and 99% less dynamic and static power dissipation than FinFET CPL RCA. DPL CNTFET RCA 97% less dynamic and static power dissipation than CMOS DPL RCA and 99% less dynamic and static power dissipation than FinFET DPL RCA. Single rail CNTFET RCA has 99% less dynamic and static power dissipation than CMOS Full static RCA and 98% less dynamic and static power dissipation than FinFET Single rail RCA. Double rail CNTFET RCA has 99% less dynamic and static power dissipation than CMOS Double rail RCA and 99% less dynamic and static power dissipation than FinFET Double rail RCA.

6. CONCLUSION

This paper presents design of RCA using different Low voltage Low power logic styles such as full static XOR, CPL XOR, DPL XOR, Double-rail domino dynamic XOR and Single rail domino dynamic XOR using CMOS, FinFET and CNTFET technologies. All these designs are simulated using Synopsys HSPICE Tool at 20nm technology with supply voltage of 0.9v.The performances of all these designs are compared in terms of Propagation Delay, Dynamic Power Dissipation, and Static Power Dissipation. These 5 logic styles are comparatively analyzed.

Compared to CMOS, FINFET technologies CNTFET has less propagation delay, less dynamic and static power dissipation than CMOS and FINFET technologies.

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