

Performance of Space Vector PWM based Induction Motor Drive using dspace

Syed. Munvar Ali, V.Vijaya kumar Reddy, M.Surya Kalavathi

Abstract— A discontinuous space vector pulse width modulation (DSVPWM) is presented for v/f control of the induction motor drive to reduce common mode voltage (CMV). The continuous space vector pulse width modulation (SVPWM) algorithms use two zero state voltage vectors at the beginning and end of the switching pattern. More ever SVPWM generate more CMV at zero voltage vectors where as in active zero state pulse width modulation (AZSPWM) algorithms CMV is minimized because of effective zero state voltage vectors. However SVPWM and AZSPWM algorithms use both zero voltage vectors at a time. The proposed DSVPWM based induction motor drive use only one zero voltage vector at a time reducing switching losses and harmonics in output phase voltages and currents. Experimental studies have been carried out for SVPWM, AZSPWM and DSVPWM based induction motor drive in dspace environment and results are presented.

Keywords- SVPWM, AZSPWM, common mode voltage, DSVPWM, zero voltage vectors.

I. INTRODUCTION

Induction motor drives in variable speed applications are getting popular because of developments in pulse width modulation (PWM) switching strategies [1]. The dynamic behavior induction motor drive with space vector pulse width modulation (SVPWM) is of interest by many researchers for medium and large scale industrial applications. The advantages of induction motor drives are replacing the DC motor drives in variable speed applications [2].

The low cost and simple construction of induction motor drives have to be operated with constant air gap flux which is achieved by changing supply voltage and frequency simultaneously. The working of the PWM inverters by several conventional PWM algorithms are discussed in [3]. The drawbacks of basic PWM techniques such as low DC bus utilization, variable switching frequency of the inverter and high value of lower order harmonics elevates the use of SVPWM inverters [4-8]. This can be carried out by SVPWM based voltage source inverters. SVPWM algorithm gives high quality of output voltage as the reference vector is synthesized by the nearest active and zero voltage vectors surrounding it in a sector. The sector identification is done by the angle calculation of reference voltage vector. The drawback of the SVPWM algorithm is it generates more CMV variations which cause bearing failure of the induction

motor and electromagnetic interference with nearby equipment. Various hybrid filters has to be used to reduce the CMV [9-13]. This additional hardware equipment increase the cost and weight and leads to the complexity of the drive system. There are several algorithms which are designed to reduce the CMV and they are presented in [14-24]. The reduced common mode voltage PWM (RCMVPWM) algorithm avoids the use of zero voltage vectors which leads to the reduction of CMV. The different RCMVPWM algorithms are AZSPWM, remote state PWM (RSPWM) and near state PWM (NSPWM) [20-24]. Among all AZSPWM algorithms use simplified approach to create effective zero state voltage vector. It uses two active voltage vectors with equal times which are in opposite to each other. The AZSPWM algorithms use instantaneous phase voltages to calculate switching times. It generates high harmonic variations. SVPWM algorithm has less total harmonic distortion (THD) but generates high CMV where as AZSPWM algorithms give lower CMV but generates high THD. The limitations of both SVPWM and AZSPWM algorithms can be avoided by implementing discontinuous space vector PWM (DSVPWM) algorithm. DSVPWM uses only one zero voltage vector at a time in entire switching pattern to reduce CMV and THD.

This paper presents the performance of the conventional induction motor drive by SVPWM, AZSPWM and DSVPWM algorithms and the results are plotted for the phase voltage, phase current, CMV and THD. The experiments are carried out on 1 H.P, 410 V, 5 A, 1470 RPM induction motor using real time dspace interface.

II. CONVENTIONAL SVPWM AND AZSPWM ALGORITHMS

The drive is operated in v/f control maintaining constant air gap flux. Initially induction motor is operated by SVPWM inverter giving two level output phase voltage. Inverter output frequency is controlled by varying the modulation index (Mi). The block diagram of induction motor by SVPWM inverter is shown in Fig. 1. The SVPWM inverter produces 8 voltage vectors V_0, V_1 through V_7 among V_0 and V_7 are zero voltage vectors as shown in Fig. 2. The reference voltage vector (V_{ref}) which is falling in any one of the six sectors can

Revised Manuscript Received on December 22, 2018.

Syed. Munvar Ali, Assistant Professor, EEE department, N.B.K.R. Institute of Science & Technology, Vidya Nagar, Andhrapradesh, India (e-mail : syedmunvarali@gmail.com)

V.Vijaya kumar Reddy, Director, N.B.K.R. Institute of Science & Technology, Vidya Nagar, Andhrapradesh, India. (e-mail : v_vkreddy@yahoo.co.in)

M.Surya Kalavathi, Professor, EEE department, JNTUH, Hyderabad, Telangana, India. (e-mail : munagala12@yahoo.co.in)



Performance of Space Vector PWM based Induction Motor Drive using dspace

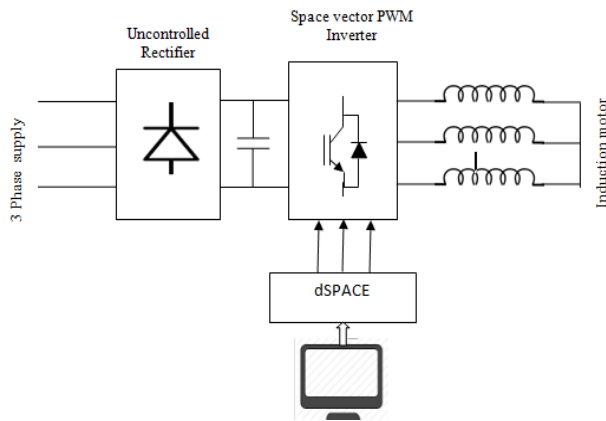


Fig. 1 Block diagram of dspace based space vector based induction motor drive

be synthesized by volt-sec balance principle considering T_s as sampling time period.

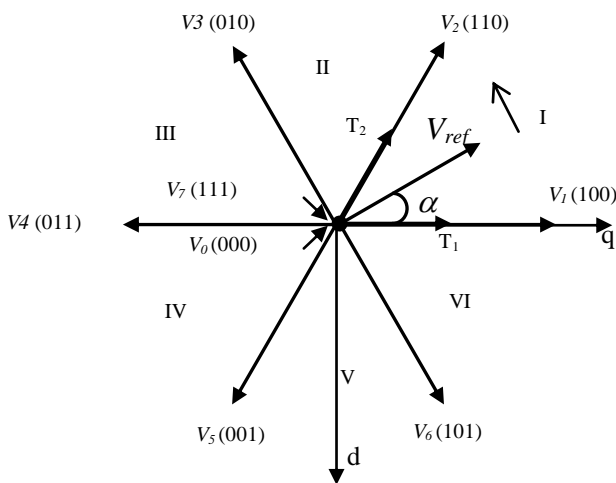


Fig. 2 Voltage space vectors of a SVPWM inverter

The zero voltage vector times are distributed evenly among two zero voltage vectors at the starting and ending of the switching pattern and the reference voltage vector is produced by volt-time balance expression and is written for sector-I as in (1).

$$V_{ref} T_s = V_1 T_1 + V_2 T_2 + V_0 T_0 + V_7 T_7 \quad (1)$$

By using (1), the voltage vector times for sector-I are calculated as in (2), (3) and (4).

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i * \sin(60 - \alpha) * T_s \quad (2)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i * \sin \alpha * T_s \quad (3)$$

$$T_z = T_s - T_1 - T_2 \quad (4)$$

The modulation index (M_i) is calculated as $M_i = \pi V_{ref} / 2V_{dc}$. The inverter pole voltages and CMV calculation for total 8 switching states are given in Table. 1.

The CMV is the potential difference between the load neutral and the negative terminal of the DC bus and is represented as in (5)

$$V_{com} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \quad (5)$$

As observed from Table. 1. The magnitude of CMV depends on switching states selected, and the use of zero switching states give more CMV. In order to reduce CMV the use of direct zero state vectors is avoided and instead of that effective zero voltage vectors are created which results in active zero state pulse width modulation (AZSPWM) algorithms. The different configurations of AZSPWM algorithms according to how the zero state voltage vectors are created are classified as AZSPWM1, AZSPWM2 and AZSPWM3 algorithms.

Table I. pole voltages and cmv of the svpwm inverter

Switching state	Inverter pole voltages			V_{com}
	V_{ao}	V_{bo}	V_{co}	
$V_0 (000)$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
$V_1 (100)$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{6}$
$V_2 (110)$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$
$V_3 (010)$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{6}$
$V_4 (011)$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$
$V_5 (001)$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{6}$
$V_6 (101)$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{6}$
$V_7 (111)$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$

In SVPWM algorithm for every 600 rotation of a reference vector in space vector hexagon the two adjacent active vectors and two zero voltage vectors are synthesized where as in AZSPWM algorithms active vectors remain same but instead of zero voltage vectors any one of the three combinations V_1 - V_4 , V_2 - V_5 or V_3 - V_6 can be used. The generation of three AZSPWM algorithms are shown in Fig. 4. The switching times of the space vectors are calculated from the instantaneous phase voltages are given as (6)

$$V_{an} = V_{ref} \cos(\theta) \quad (6)$$

$$V_{bn} = V_{ref} \cos\left(\theta - \frac{2\pi}{3}\right) \quad (6)$$

$$V_{cn} = V_{ref} \cos\left(\theta - \frac{4\pi}{3}\right)$$

Then, at each instant, the high (V_{max}), medium (V_{mid}) and lower (V_{min}) values of 3-phase voltages are calculated and the switching times are derived as (7)

$$T_1 = \frac{T_s}{V_{dc}} (V_{max} - V_{mid})$$

$$T_2 = \frac{T_s}{V_{dc}} (V_{mid} - V_{min}) \quad (7)$$

$$T_2 = \frac{T_s}{V_{dc}} (V_{mid} - V_{min})$$

Then, by using the space vector concept, the favorable switching sequences are calculated as illustrated in Table 2.

Table2. Switching Pattern for active zero state Algorithms

SECTOR	SVPWM	AZSPWM1	AZSPWM2	AZSPWM3
1	0127-7210	3216-6123	5122-2215	4211-1124
2	0327-7230	4321-1234	6233-3326	5322-2235
3	0347-7430	5432-2345	1344-4431	6433-3346
4	0547-7450	6543-3456	2455-5542	1544-4451
5	0567-7650	1654-4561	3566-6653	2655-5562
6	0167-7610	2165-5612	4611-1164	3166-6613

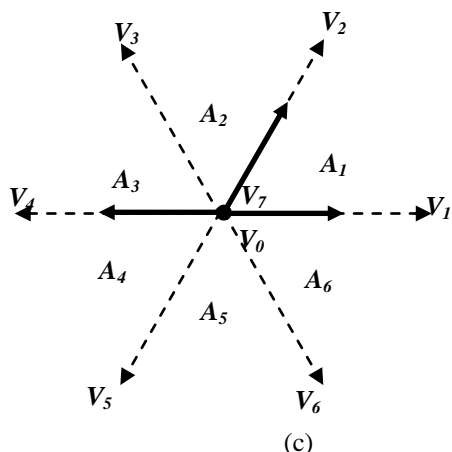
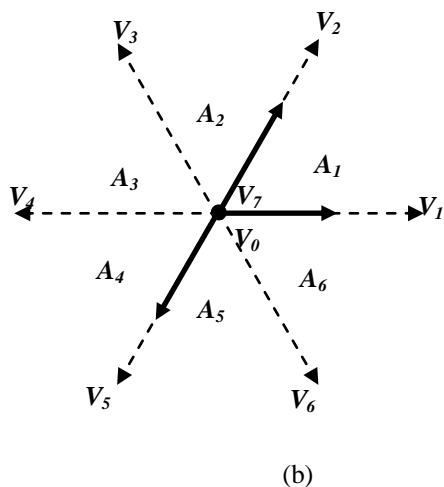
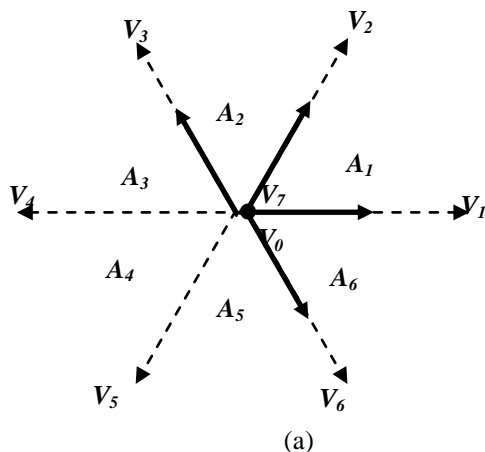


Fig. 3 Voltage space vectors distribution of AZSPWM algorithms

III. PROPOSED DISCONTINUOUS SVPWM BASED INDUCTION MOTOR

In the present discontinuous SVPWM the zero voltage vectors are not combinely used, only one of it is used at a time. There is no change in active voltage vector times. The zero state vector time is divided as T_{01} and T_{02} and their expressions are derived and shown as (8).

$$T_0 = T_s - T_1 - T_2 \quad (8)$$

$$T_{01} = a_0 T_0$$

$$T_{02} = (1 - a_0) T_0$$

The switching states of the voltage vectors are shown in Table 3

Table3. Switching Sequences for DSVPWM Algorithms

Sector	DSVPWM
1	721-127 812-218
2	832-238 723-327
3	743-347 834-438
4	854-458 745-547
5	765-567 856-658
6	816-618 761-167

From eq (8) the value of a_0 is either 0 or 1. The value of a_0 in all sectors to generate discontinuous SVPWM is shown in Table 4.

Table 4. VALUE OF a0 IN ALL SECTORS BY DSVPWM ALGORITHM

sector	1	2	3	4	5	6
a_0	1 0	0 1	1 0	0 1	1 0	0 1

In sector -I from 0 to 300 the value of a_0 is 1 and then it is 0 from 300 to 600 and for the remaining sectors it is shown in Table 4.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

To evaluate the performance of conventional induction motor drive in v/f control experimental studies have been done on various PWM algorithms. The gating signals to the PWM inverter is given by the dspace. The experimental set up is shown in the following figure. The control signals to the inverter are generated at a switching frequency of 3K.Hz. The induction motor parameters are 1 HP,440V,5A,1470 rpm.



Performance of Space Vector PWM based Induction Motor Drive using dspace

The results of phase voltage, current, CMV variations phase current and voltage THD for SVPWM, AZSPWM1, AZSPWM2, AZSPWM3 and DSVPWM algorithms are shown in Fig. 4, Fig. 5, Fig. 6, Fig. 7 and Fig. 8 respectively.

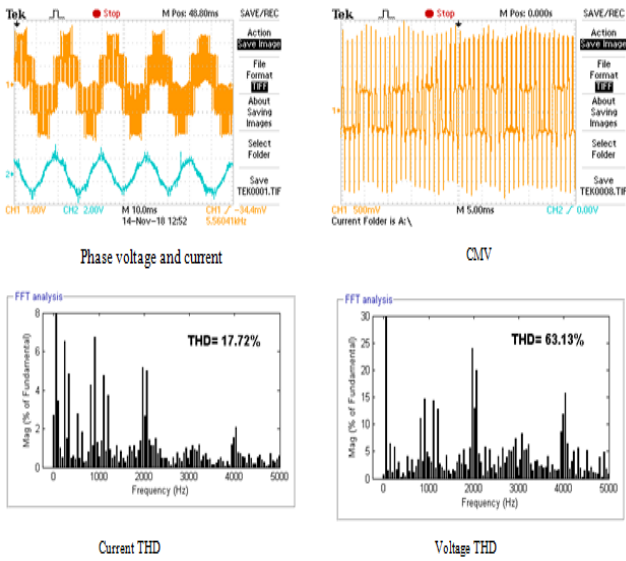


Fig. 4 Phase voltage current and CMV plots with THD for SVPWM based induction motor drive

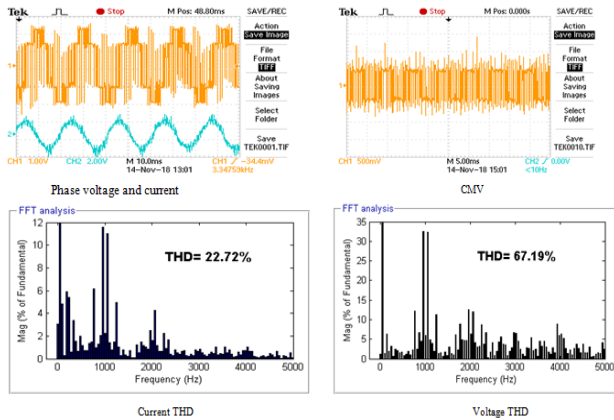


Fig. 5 Phase voltage current and CMV plots with THD for AZSPWM1 based induction motor drive

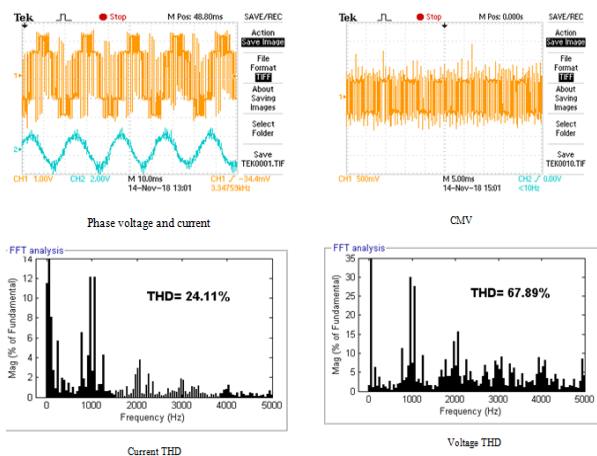


Fig. 6 Phase voltage current and CMV plots with THD for AZSPWM2 based induction motor drive

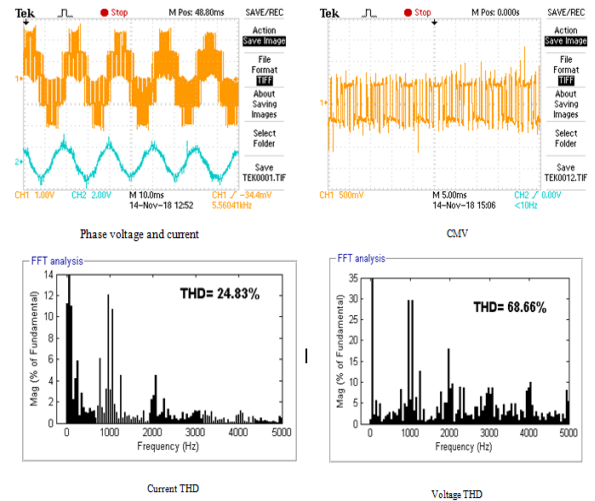


Fig. 7 Phase voltage current and CMV plots with THD for AZSPWM3 based induction motor drive

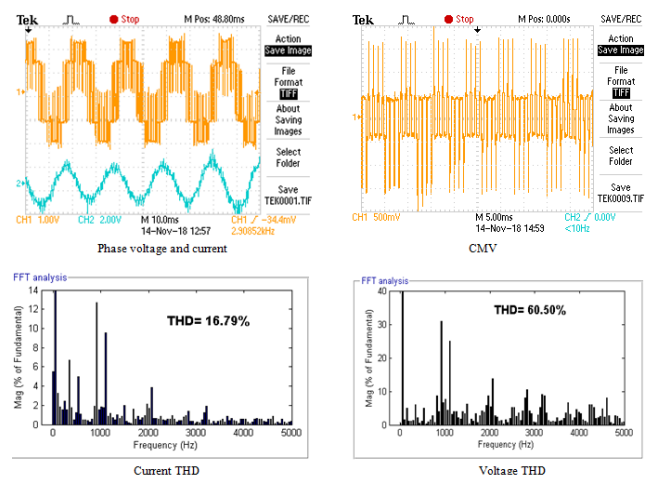


Fig. 8 Phase voltage current and CMV plots with THD for DSVPWM based induction motor drive

V. CONCLUSIONS

DSVPWM based conventional induction motor drive has good performance. It produces output phase voltage and current with less THD comparing with continuous SVPWM and different configurations of AZSPWM algorithms. In proposed DSVPWM one zero switching state is avoided in one sampling time period resulting in reducing the switching losses of the inverter.

REFERENCES

1. Joachim Holtz, "Pulsewidth modulation – A survey" IEEE Trans. Ind. Electron., vol. 39, no. 5, Dec 1992, pp. 410-420.
2. Marian Gaiceanu, Silviu Epure, Cristinel Radu Dache, Razvan Buhosu, Iulian Ghenea, Cristian Vidan, "Laboratory power inverter platform for variable speed drive", Electrical and Electronics Engineering (ISEEE) 2017 5th International Symposium on, pp. 1-6, 2017
3. S. P. Jena and K. C. Rout, "Comparative Analysis of Harmonic Reduction of VSI Fed Induction Motor Using SVPWM and Sinusoidal PWM," 2018 2nd International Conference on Trends in Electronics and Informatics (ICOEI), Tirunelveli, India, 2018, pp. 1-5.

4. Jalnekar,Rajesh&SJog, K. "Pulse-Width-Modulation Techniques: A Review" IETE Journal of Research. 2015.
5. Aboadla, Ezzidin & Khan, Sheraz & Habaebi, Mohamed & Gunawan, Teddy & Hamida, Belal & Yaacob, Mashkuri."Effect of modulation index of pulswidthmodulation inverter on total harmonic distortion for sinusoidal. pp192-196, 2016.
6. W. Makhubele,Josias & A.Ogudo, Kingsley. "Analysis on Modulation Techniques of an AC drive with Respect to Harmonic Content and Efficiency. pp1-8, 2018.
7. Aboadla, Ezzidin & Tohtayong, Majdee & A. Bin Aznan, Khairil & Khalil, Ashraf & Khan, Sheraz & Habaebi, Mohamed & Gunawan, Teddy & Hamida, Belal & Yaacob, Mashkuri. "A comparative study between SPWM and SHE-PWM modulation techniques for DC-AC inverters".pp 1-5, 2017.
8. Ronanki,Deepak&AbdulAzeez,Najath & Patnaik, Lalit & S. Williamson, Sheldon".Hybrid multi-carrier PWM technique with computationally efficient voltage balancing algorithm for modular multilevel converter". 224-229,2018.
9. M. Ghosh Majumder, A. K. Yadav, K. Gopakumar, K. R. R. U. Loganathan and L. G. Franquelo, "A Five-Level Inverter Scheme Using Single DC Link with Reduced Number of Floating Capacitors and Switches for Open-End IM Drives," in IEEE Transactions on Industrial Electronics.doi: 10.1109/TIE.2019.2898594
10. Reddy, B & Reddy Kondreddy, Sreekanth & Siva Reddy Beduduri, Samba. "Novel single phase full bridge inverter formed by floating capacitors. International Journal of Power Electronics and Drive Systems (IJPEDS). 7. 193. 10.11591/ijpeds.v7.i1.pp193-201. 2016.
11. Kirthika Devi, V.S. & Srivani, S G."A new PWM technique for symmetric and asymmetric seven level multilevel inverter topology with reduced number of DC sources". International Journal of Applied Engineering Research. 10. 22299-22311.2015
12. S.Kwak &S. Mun, "Model predictive control methods to reduce common mode voltage for three-phase voltage source inverters," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 5019-5035, Sept. 2015.
13. Junjie, li & Jiang, Jianguo. "Active Voltage-balancing Control Methods for the Floating Capacitors and DC-link Capacitors of Five-level Active Neutral-Point-Clamped Converter. Journal of Power Electronics. 17. 653-663. 2017.
14. T. Ahmad and Z. Miao, "Common mode voltage reduction schemes for voltage source converters in an autonomous microgrid," 2015 North American Power Symposium (NAPS), Charlotte, NC, 2015, pp. 1-5.
15. Z. Li, Y. Guo, Z. Song, H. Li and X. Zhang, "Modified Synchronized SVPWM Strategies to Reduce Common-Mode Voltage for Three-Phase Voltage Source Inverters at Low Switching Frequency," 2018 21st International Conference on Electrical Machines and Systems (ICEMS), Jeju, 2018, pp. 1330-1334.
16. D. Han, Y. Wu, S. Li and B. Sarlioglu, "Zero state common mode voltage control in motor drives through inverter topology," 2017 IEEE Transportation Electrification Conference and Expo (ITEC), Chicago, IL, 2017, pp. 556-560.
17. P. Garg, S. Essakiappan, H. S. Krishnamoorthy and P. N. Enjeti, "A fault tolerant three-phase adjustable speed drive topology with active common mode voltage suppression," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2828-2839, May 2015.
18. A. P. B. Jyoti, J. Amarnath and D. S. Rayudu, "A family of scalar based reduced common mode voltage PWM algorithms for induction motor drives with reduced complexity," International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), Jaipur, 2014, pp. 1-7.
19. X. Guo, D. Xu and B. Wu, "Four-Leg Current-Source Inverter With a New Space Vector Modulation for Common-Mode Voltage Suppression," in IEEE Transactions on Industrial Electronics, vol. 62, no. 10, pp. 6003-6007, Oct. 2015.
20. N.A.M. Said, J. E. Fletcher, R. Dutta and D. Xiao, "Analysis of common mode voltage using carrier-based method for dual-inverter open-end winding," 2014 Australasian Universities Power Engineering Conference (AUPEC), Perth, WA, 2014, pp. 1-6
21. Hyeoun-Dong Lee and Seung-Ki Sul, "A common mode voltage reduction in boost rectifier/inverter system by shifting active voltage vector in a control period," in IEEE Transactions on Power Electronics, vol. 15, no. 6, pp. 1094-1101, Nov. 2000.
22. N. Choi, E. Lee and K. Ahn, "Space vector PWM for common mode voltage reduction and neutral point voltage balancing in three-level converters," 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEM-ECCE Asia), Hefei, 2016, pp. 2401-2405.
23. J. Hu, J. Tang, Y. Mei, S. Hu, W. Li and X. He, "Common-mode voltage analysis and suppression in five-level modular composited converter," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 4873-4878.
24. M. Cacciato, A. Consoli, G. Scarcella and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," IEEE Trans. on Industry Applications, vol. 35, no 2, pp. 469 – 476, March-April 1999.