Design and implementation of low power 5 stage Pipelined 32 bits MIPS Processor using 28nm Technology

V.Prasanth, V.Sailaja, P.Sunitha, B.Vasantha Lakshmi

Abstract*— *MIPS is a simple streamlined highly scalable RISC architecture is most used in android base devices and best suited for portable mobile devices. This Paper presents a design of 5 stage pipelined 32 bit MIPS processor on a 28nm Technology. The processor is designed using Harvard architecture. The most important feature of pipelining is performance and speed of the processor, this results in increase of device power. To reduce dynamic power using RTL clock gating inside FPGA device we presented a novel approach in this paper. Design functionality in terms of area power and speed is analyzed using kintex 7 platform board.

Keywords: RISC,MIPS, Clock Gating, Dynamic Power, FPGA,Pipeling

I. INTRODUCTION

For the past few decades MIPS processor played a major role in design of battery operated devices and is one of the major RISC processor which is delivering best performance with low power utilization in a given predefined silicon area .Cost and power saving are one of the significant features in designing SoC. Major difference between CISC and RISC processor is later uses instructions of less number and can be best used for embedded real time applications which occupies low are with high speed applications. Lot of research is going towards design of MIPS CPUs for smaller silicon area and lower power consumption. In This Paper we presented a MIPS processor using Harvard architecture. MIPS stand for “Micro-processor without interlocked pipeline stages” developed by ‘D.A.Patterson’ and ‘J.L.Hennessy’ is a computer architecture best suited for portable device applications. The main aim of this design is to create a faster processor using simple instruction set by including pipeline stages so latency can be reduced and speed is increased. Pipelining is a set of registers separated into 5 stages as fetch, decode, execute, memory access and write-back. Pipelining is a process of executing stage by stage with a clock synchronous network which helps in preventing loss of information and also enhance the speed performance of processor. The operations used by MIPS processor in instruction set which are generally used to access memory in MIPS processor are load and Store and other operations which are remaining are performed on register to register basis [2] this results in more clear instruction set design where it allows execution of one instruction-per cycle rate. The pipelining uses parallelism at instruction level to execute multiple instructions simultaneously using a single processor [2]. The major disadvantage with MIPS processor design is dynamic power consumption results due to clock power and switching-activity. Clock Gating is a method which employed in the design to reduce power consumption [17] by reducing switching activity of non active blocks. Total power consumption results with switching activity, capacitance and voltage swing of the transistor and major component is Clock power with respect to overall dynamic power consumption, the effective usage of clock can minimize power consumption. Clock gating is method which disables the clock signals in case of modules that are no use of the total hardware. Nowadays the most important performance factor in embedded portable applications is to maintain trade of between power speed and area. Due to major advancement in technology towards low power devices design engineers have to compromise with area and speed.

II. ARCHITECTURE of 32 bits MIPS PROCESSOR

A. Single Cycle MIPS Processor

The Design of MIPS Processor includes is as shown in figure:1

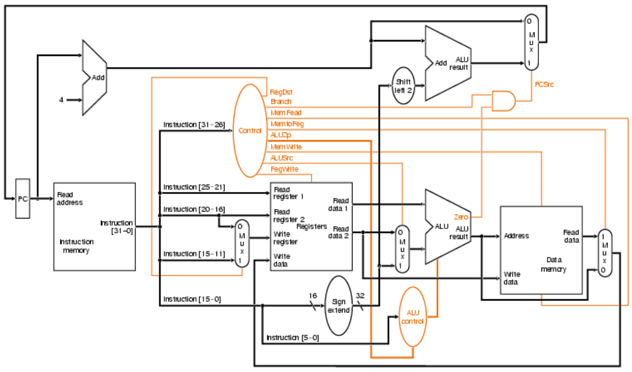

Figure 1. Architecture of Single Cycle MIPS Processor

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The 3 different types of instruction used in MIPS are ALU Instructions, Load and Store Instruction and Branch and Jump Instructions.

a) ALU Instructions: These Instructions used two registers and single ended extended registers to perform operations of arithmetic and logic as ADD, MUL,SUB,OR, AND, etc, Instructions.

b) Store and Load Instructions: Arithmetic and logic operations of these operands contain base registers and offset and collectively called them as ‘effective addresses. To operate data in main memory, Registers copies the data first. A load word instruction copies data from main memory into a register. A store word instrcution copies data from a register into main memory.

c) Branch and Jump Instructions: These instructions are used to control conditional transfer.

Every Instruction in MIPS processor in implemented using 5 clock cycles namely as

1. Instruction Fetch(IF): Fetching current instruction from memory through PC and PC is updated to next by adding 4 to PC (PC+4)
2. Instruction Decode (ID) : Translate the opcode of the instruction to appropriate control, sign extended if needed, fetch operand values from the registers and Computes the possible branch target address.
3. Execute (EX) : Activate appropriate functional unit – Adder, Multiplier, Divider, Logical Unit. It performs operations for Memory Instruction, Register-Register Instructions and Register – immediate Instructions.
4. Memory Access (MEM): Load and Store Instructions are being performed, if load instruction its read from Memory and store instruction writes to Memory address.
5. Write Back : Register Files get the final result with Write signal.

Three types of Instruction formats are used in this MIPS processor: R-type, I-type and J-type.

Register-type format(R Type)

opcode	rs	rt	rd	Shift amount	function

6 5 5 5 5 6

SUB, ADD, MUL operations are used in this format.

Immediate-type format (I type)

opcode	rs	rt	Address

6 5 5 16 (offset)

Load and store instructions of I-Type

Jump-type format (J Type)

opcode	Address

6 26 (offset)

Used by jump and Branch Instructions

B.Multiple Cycle MIPS Processor

Multistage-pipeline allows a CPU to perform more than one instruction at a time. Efficient pipeline is achieved with the predictability (and similarity) of the time for all instructions

Instruc. No.	Pipeline Stage								
1	IF	ID	EX	ME	WB				
2		IF	ID	EX	ME	WB			
3			IF	ID	EX	ME	WB		
4				IF	ID	EX	ME	WB	
5					IF	ID	EX	ME	WB
Clk Cycle	1	2	3	4	5	6	7	8	9

Figure 2: 5 Stage Pipelining Structure

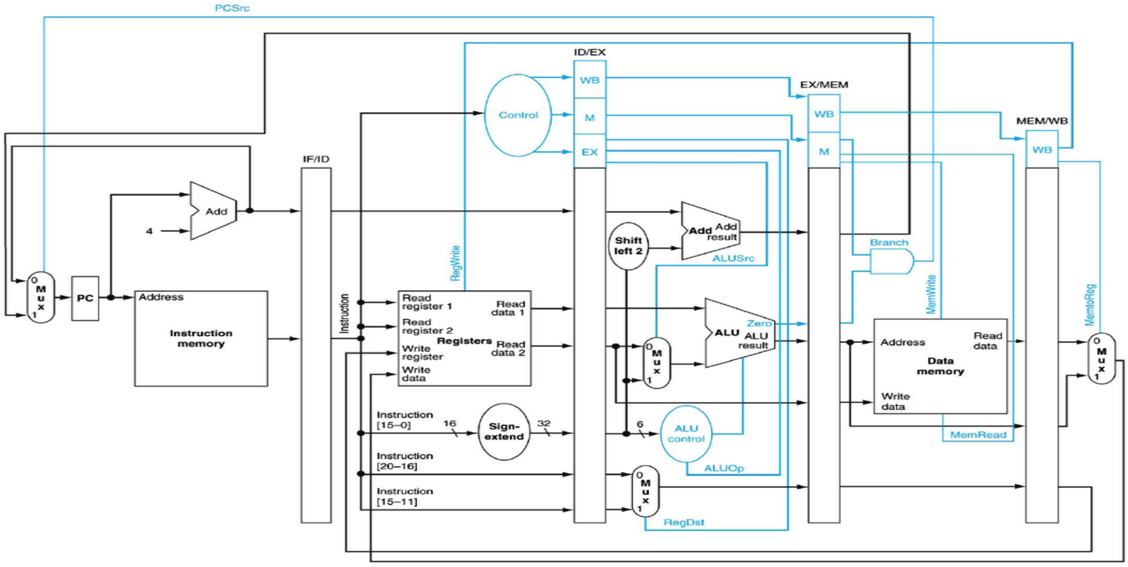

Figure 3: Architecture of Multi cycle 5-stage pipelined MIPS Processor

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The Main disadvantage of Single cycle when using Load word instruction where clock cycle will have same length for every instruction results longest possible path as load word uses five functional units which are as follows “instruction-memory, register-file, ALU, Data-memory and register-file” [10] again thus restricting the single cycle approach for smaller instruction. This can be avoided in Multi-cycle Approach where instructions are divided. The most advantageous in this execution is with this implementation functional unit can be used more than once. Comparing to the single-cycle and Multi-cycle the differences are that only one instructions and data uses only one Memory Unit, To hold the output value we use only one ALU, two adders and several output registers are added to the unit which are used in a later clock cycle. Output of the memory is saved by adding instruction register and the memory data register. Data is held in these registers with exception of the IR between a pair of adjacent clock cycles. a write control signal is required to hold the value in IR during the whole time of execution. Additionally a multiplexer is added to choose between the A register and the PC for the first ALU input and second ALU input is changed from a 2-to-4 multiplexer. A constant 4 sign extended number and shifted offset field for the branch instruction and PC is incremented these 2 inputs selected. A datapath is required to handle more branch and jump instructions. The three cases of R-type instructions, branch instruction and jump instruction cause three different values to be written into the PC: The PC Stores directly PC + 4 which is ALU output .After branch target address is computed by register ALUResult the 26 bits of lower part of IR is shifted left by 2 and concatenated with the upper 4-bits of the incremented PC for the jump instruction. If the instruction is branch, PC will be conditional for write signal. PC will have computed branch address if two registered which are compared are qual.. So two write signal are needed by PC, one is which WritePC if the write is unconditional (PC + 4 is value or for jump instruction) and if the write is conditional WritePCond. It also shows that the write signal for the PC is combined form the ALU zero bit and the two write signals WritePC and WritePCond by an AND gate and OR gate.

III. CLOCK GATING AND POWER CONSUMPTION

Frequency, switching activity as a function of voltage and charging and discharging of capacitances during the operation of the circuit are the major factor in Dynamic Power Consumption. The dynamic power consumption is generally defined as below

$$P = CV^2 f$$

Where F,C and V represent Clock Frequency, Capacitance and the voltage swing,

A. Clock Gating

One of the major important concerns for clock network design is power efficiency. In FPGA clock network connects to each and every flip-flop which has a significant impact on power every time clock cycle toggles. Present FPGA with 28nm technology accounts for 18% of total dynamic power dissipated in clock network. Due to flexibility of the clock network packing and placement constraint imposed by FPGA which results in power dissipation in other parts of the FPGA and quality will be reduced.

Clock gating is a method which reduces switching activity on circuit signals, by disabling the clocking of specific registers for the interim when the outputs of those registers are unimportant to circuit outputs [8]. Flexibility of Clock network has major disadvantage in regard to more capacitance formed on the clock nets, and clock signal which is routed through many switches results in increased dissipation of power. it is essential in the design to calculate the switching activity in the clock network and minimize the usage of clock results in minimal routing.

Clock-distribution network also impacts Computer-aided design (CAD) tools, so as to reduce the power in the design without compromising with clock frequency usage in the circuit. One of the minor constraints on the placement algorithm is non flexibility to supply enough clock signals to flip-flops in clock networked FPGAs, as well as logic elements are grouped into clusters using clustering algorithm. If the clock network doesn’t have flexibility will result in increased power dissipation and delay in a user circuit. This tradeoff between power and delay must be considered by vendors of FPGA for clock distribution networks

Clock Gating implementation at Chip Level:

Designing circuits on FPGA which result in more power consumption than ASIC design as most of the FPGA area is unused, at system level Clock gating is used to stop clock for an entire FPGA so the functionality in the design can be disabled. Switching of Logic is prevented in this. Freeze mode is used in Flash type FPGAs results flexible clock gating than clock gating at system-level, freezing clocks and by controlling input and output states.

B.Clock Gating at Design Level

Power saving technique which was normally used in RTL Design is Clock Gating. The two types of clock gating using in digital circuits are latch-free clock gating and latch-based clock gating. Latch- free clock gating uses a simple AND gate. But, in the design clock is to be enabled at rising edge and should hold it constantly until falling edge so as to prevent clock glitches.. In synthesis tools of FPGA clock gating is not performed automatically rather than user has to analyze the circuit and need to design own algorithm to enable and disable clock at predefined intervals without delimiting performance of the design.

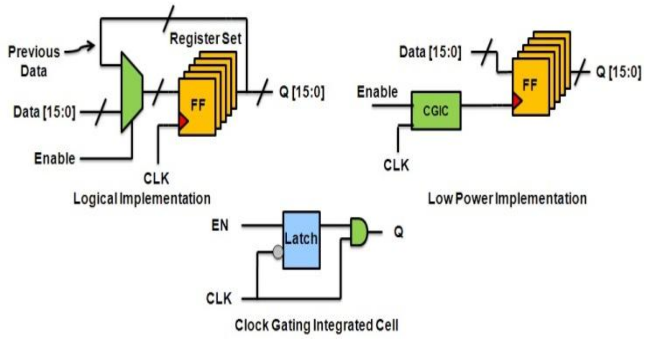


Figure 4: Clock Gating Approach across Pipeline Stages

IV.RESULT AND DISCUSSION

THE MIPS32 Processor is evaluated using Kintex-7 KC 707 Board which is 28nm Technology which uses differential Phase clock. The Integrated Clock Gating in FPGA is used in This Design to reduced switching activity of the Design. The Implementation resulted in Gated Clock for 100% BRAMs and 98% for IO Logic used in the design. In This Design without using clock gating we got 152mw Dynamic power and by implementation of Clock gating and reducing switching activity resulted in 18mw power. The Result is obtained for the case where more no of inactive blocks are presented Resulted in high power reduction.

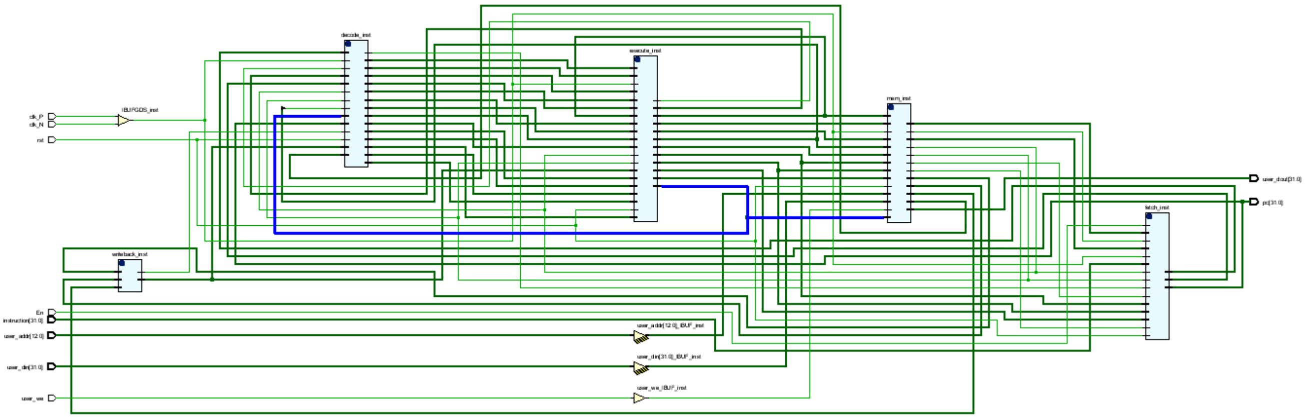


Figure 5:RTL View of 32 Bits MIPS Processor

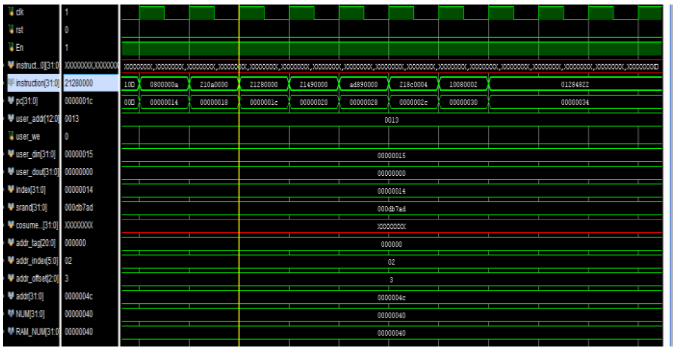
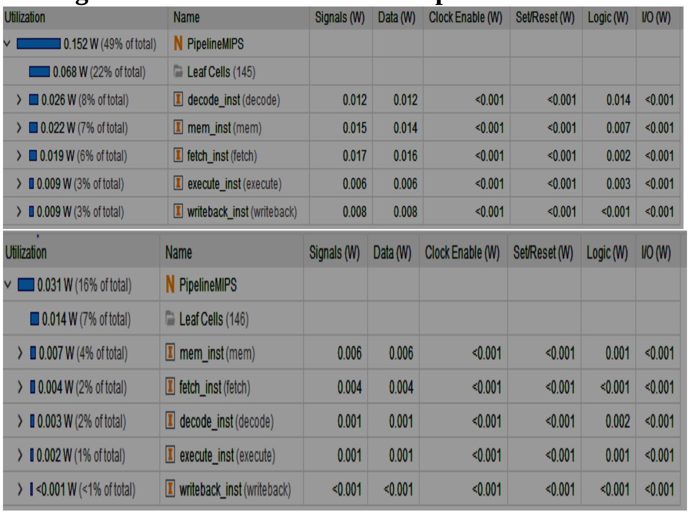


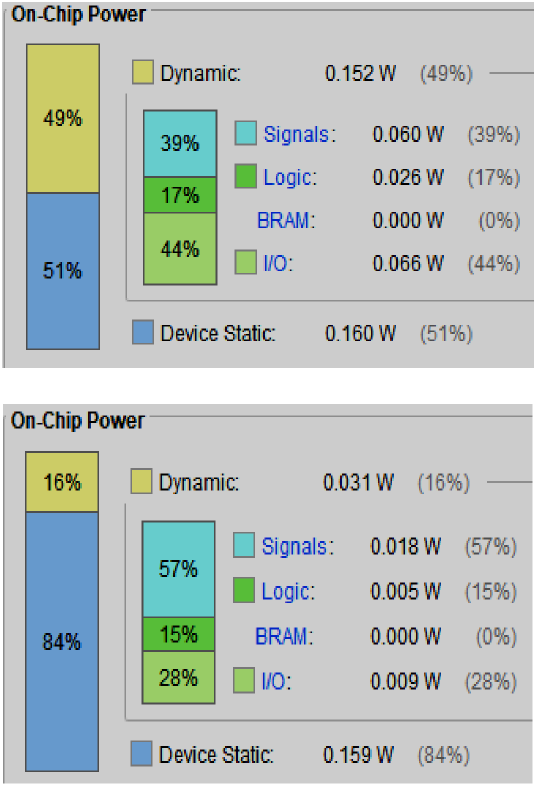
Figure 6: Simulation Result of Mips Processor



Utilization	Name	Signals (W)	Data (W)	Clock Enable (W)	Set/Reset (W)	Logic (W)	I/O (W)
0.152 W (49% of total)	PipelineMIPS						
0.068 W (22% of total)	Leaf Cells (145)						
0.026 W (8% of total)	decode_inst (decode)	0.012	0.012	<0.001	<0.001	0.014	<0.001
0.022 W (7% of total)	mem_inst (mem)	0.015	0.014	<0.001	<0.001	0.007	<0.001
0.019 W (6% of total)	fetch_inst (fetch)	0.017	0.016	<0.001	<0.001	0.002	<0.001
0.009 W (3% of total)	execute_inst (execute)	0.006	0.006	<0.001	<0.001	0.003	<0.001
0.009 W (3% of total)	writeback_inst (writeback)	0.008	0.008	<0.001	<0.001	<0.001	<0.001

Utilization	Name	Signals (W)	Data (W)	Clock Enable (W)	Set/Reset (W)	Logic (W)	I/O (W)
0.031 W (16% of total)	PipelineMIPS						
0.014 W (7% of total)	Leaf Cells (146)						
0.007 W (4% of total)	mem_inst (mem)	0.006	0.006	<0.001	<0.001	0.001	<0.001
0.004 W (2% of total)	fetch_inst (fetch)	0.004	0.004	<0.001	<0.001	<0.001	<0.001
0.003 W (2% of total)	decode_inst (decode)	0.001	0.001	<0.001	<0.001	0.002	<0.001
0.002 W (1% of total)	execute_inst (execute)	0.001	0.001	<0.001	<0.001	0.001	<0.001
<0.001 W (<1% of total)	writeback_inst (writeback)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001

Figure 7: Dynamic power a) without clock gating b) with clock gating



On-Chip Power

Dynamic:	0.152 W	(49%)
Signals:	0.060 W	(39%)
Logic:	0.026 W	(17%)
BRAM:	0.000 W	(0%)
I/O:	0.066 W	(44%)
Device Static:	0.160 W	(51%)

On-Chip Power

Dynamic:	0.031 W	(16%)
Signals:	0.018 W	(57%)
Logic:	0.005 W	(15%)
BRAM:	0.000 W	(0%)
I/O:	0.009 W	(28%)
Device Static:	0.159 W	(84%)

Figure 8: Onchip-Total Power a) without clock gating b) with clock gating

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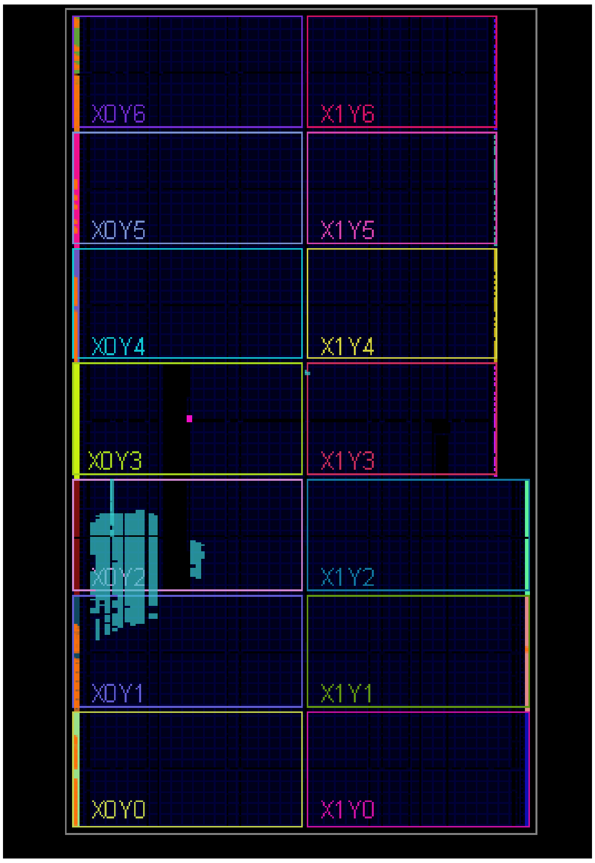
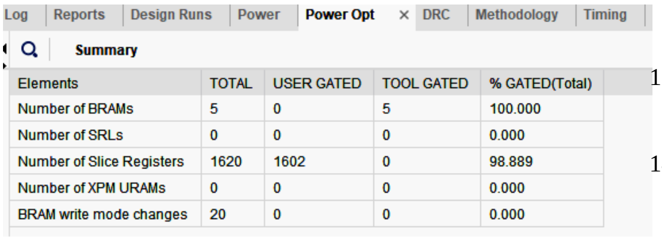


Figure 9: MIPS 32 implemented on Kintex-7 Device



Elements	TOTAL	USER GATED	TOOL GATED	% GATED(Total)
Number of BRAMs	5	0	5	100.000
Number of SRLs	0	0	0	0.000
Number of Slice Registers	1620	1602	0	98.889
Number of XPM URAMs	0	0	0	0.000
BRAM write mode changes	20	0	0	0.000

Figure 10. Power Optimization Report

CONCLUSION

32 bit MIPS processor is designed using Verilog HDL in Vivado HLS on Kintex-7 KC 705 Development Board. FPGA boards are internally having optimization of clock using Clock enable in the design which can reduce overall power of block design. In this paper we have utilized integrated Clock enable for clock gating so as to reduce power in the design. As the switching active in 5 stage pipeline is less and because of more number of pipeline stage registers will result in toggling of flip-flops in the design. This is reduced in our project by effectively gating the clock on inactive models which resulted in 73% of power reduction in Dynamic power.

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