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Design of Combinational Logic Circuits Using Memristor and CMOS Logic

Kichchannagari Omkar Reddy, D. Gracin, V. Ravi and S. Ananiah Durai

Abstract*: *Introduction of the memristor has paved the way to many inventions in VLSI domain. The properties of memristor such as the nanometer scale measurements and its non-volatile memory qualities have yielded more attention towards research people. The nanometer scale highlight of the memristor makes another door open for the realization of innovative circuits for logic blocks from the more standard designs. Non-volatile memory property empowers us to acknowledge new outline strategies for an assortment of computational components that prompt novel models. By this, there comes the idea of the combination of the Nano-scale memristor and CMOS, which ends up conceivable to diminish usage of silicon territory accordingly giving a promising alternative in the plan of memristor and CMOS based circuits. In this paper, we are presenting a combinational circuit design using memristor and CMOS logic as well as the implementation of a built-in self-test circuit to test the core functionalities of the logic. It is composed of a test pattern generator and output response analyzer which will compare the output response of the unit under test circuit with the pre-stored expected patterns of the unit under test. Designing the circuit utilizing this mix advantage of memristor and CMOS spares a great deal of chip space and power utilization and it is reliable as well.

Index Terms*: *CMOS, memristor,BIST, LFSR.

I. INTRODUCTION

Nowadays in the VLSI industry companies are funding more to nanomaterial's research where design engineers are looking for a Nano-scale device which is having good electrical property to use in the logic blocks designing, In this letter we are presenting a novel Nano-scale device called memristor[1] the name comes from the memory resistor it has the ability to memorize the past resistance it is pretty descriptive but if you don't know what resistance really is then that really doesn't mean anything. The behavior of the resistor can be explained with a simple practical example in place of resistor we take conductance which is the inverse measure of resistance. Imagine overhead water tank has a pipe if we want to empty the overhead tank we will open the nozzle of the pipe so that water will drain out from the pipe if there is only one pipe the time taken for draining of the entire tank is suppose 1 hour if we have two pipes the water will drain out only in half an hour here the pressure being exerted by the tank due to the gravity is analogy to the voltage and the diameter of the pipe is analogy to the conductance and flowing of the water through pipe is analogy for the current i.e. flow of electrons, if the diameter of the pipe is changing as the pressure exerted by the tank or the rate of flow of water is affecting the change in the diameter of the pipe is nothing but the change of conductance. In the same way, as we apply the voltage and direction of the current is responsible for the change of resistance in the memristor[2–5]. It describes a very broad class of resistance-changing devices. Achievable through different physical mechanisms, phases change, electrostatic, redox, etc. Many applications enabled by orthogonal properties means it is impossible to achieve certain properties at the same time and certain use such as oscillators high endurance (high endurance circuits will break the device, when we want for oscillations with the non-volatile property), memory incremental low decay (low decay if we need to apply large potential to device to switch between the states which lead to more energy dissipation), memristor is nothing but a resistive state machine. Memristor alone logic is having the disadvantage of endurance, reliability and signal restoration is not available we are proposing the hybrid memristor[6] and CMOS (Complementary metal oxide semiconductor) logic where the Nano-scale advantages of the memristor can be added[7] with CMOS reliability and signal restoration. This letter proposes a logic block of digital design such as AND, OR, NAND, NOR, MUX, DECODER and BIST unit(built-in-self-test).In today world testing is playing a major role in the VLSI industry where engineers are pushing their limits in detecting the faults in the design at various level. BIST[8–12] unit normally consist of 3 blocks first one is the test pattern generator which can be implanted with the LFSR(linear feedback shift register) and the unit under test is the circuit which we want to test and the last block is the ORA(output response analyzer) which is nothing but comparator which compares the output of the unit under test circuit to the pre-stored values in the RAM and gives out the result as pass or fails, every chip normally will have two modes one is the test mode and the other is the functional mode, in the test mode we can test the functional verification of the chip like all led are glowing or not the bus interface is functioning correctly or not and much more functionality can be tested and if the chip fails in the test mode which can be quickly debugged an issue can be identified. Testing can be formal verification which is exhaustive testing (checking for all possible input combinations), gate level testing (checking the functionality of each gate by giving the corresponding inputs and analyzing the outputs). The linear feedback shift register (LFSR) is of two types of internal and external XOR linear feedback shift register a where the first has more input combination as compared to the latter.

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II. *LITERATURE SURVEY*

As presented in[13] memristor has different voltage and current curve when compared to the basic resistor, inductor and capacitor which is called as the pinched hysteresis loop which can states as below when we increase the positive voltage of the memristor current through it will increase very small and this state is called as the high resistance state and if we further increase the voltage slightly then the current through it will increase rapidly and reached state called as the low resistance state as shown in Fig.1 and we will be using these states for our switching and from the low resistance state if you decrease the positive voltage the current will decrease gradually and it reaches zero when the voltage reaches zero and if you decrease the negative voltage current will decrease slowly and reaches the high resistance state and if voltage still reduces the current will decrease rapidly and reaches the low resistance state and from this point if you increase the negative voltage, current will also increase and when the voltage reaches near zero the current will also reach zero. This phenomenon of curve intersecting at the zero voltage and zero current is called as the pinched.

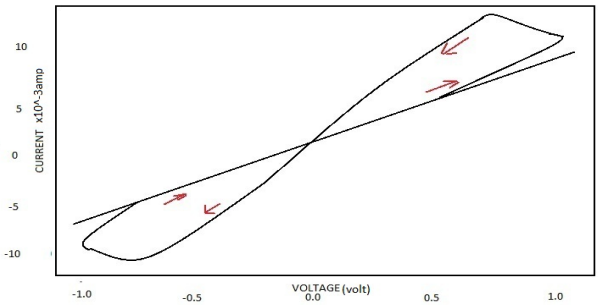

Fig 1: Hysteresis loop of the memristor.

We will present the polarity of the memristor as shown in Fig.3 if the current is flowing into the black mark then the resistance of the device becomes less and current flowing out of the black mark the resistance of the device increases Fig 2, integrated memristor with standard logic is having voltage as a logic state same as that of the standard CMOS logic which helps to use memristor as a combinational[14] element irrespective of the memory characteristic of the device and the initial state of the device. AND gate memristor circuit is shown in Fig.4.

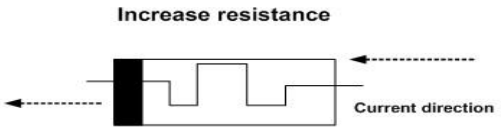

Fig 2: Memristor current direction for increased resistance

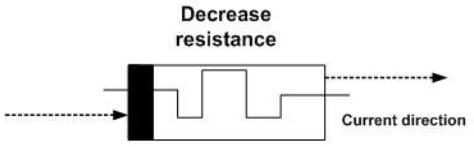

Fig 3: Memristor current direction for decreased resistance

A. Logic AND

As shown below[6] Fig 5 AND logic operation[12] as follows if both the inputs are having logic 0 or they are connected to the ground we assume that the output node is floating, so there is no voltage upon the memristor, therefore, there is no current flow through the memristor, so the output is also ground or logical 0. If we consider [6] Fig 6 both the input nodes are connected to VDD or having logical 1 both nodes are same voltage again no current flows through the memristor so the input voltage appears across the output which is logical 1, now if one input is 1 and another input is 0 we have two cases so consider one in this case one input is logical 1(upper memristor) and another input is logical 0(bottom memristor) so current flows from the upper memristor to the bottom memristor and because of the polarity of the memristor the resistance of the upper one is increased and the resistance of the lower one is decreasing so after enough time of this voltages will achieve the maximum resistance of the upper memristor R off (high resistance state) and minimum resistance for the lower memristor Ron (low resistance state) so it just a regular voltage divider and therefore the output resistance is under the assumption that R off is significantly higher than R, the voltage at the output is approximately equal to ground or logical 0.

$$V_{out}=V_{cc}\left(\frac{R_{on}}{R_{on}+R_{off}}\right)=V_{cc}\frac{R_{on}}{R_{off}}(R_{off}>>R_{on})$$ [15]... (1)

The gate as shown in Fig.4 is an AND gate [4], [16] with the inputs given as IN 1 and IN 2.

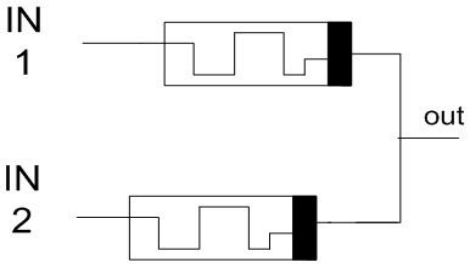

Fig 4: Memristive AND logic

When both inputs are 0 are applied, no current flows through it.

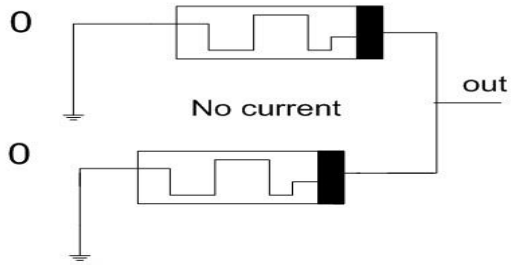

Fig 5: Memristive AND logic with 0 as Inputs

When both inputs are applied 1, the output is high.

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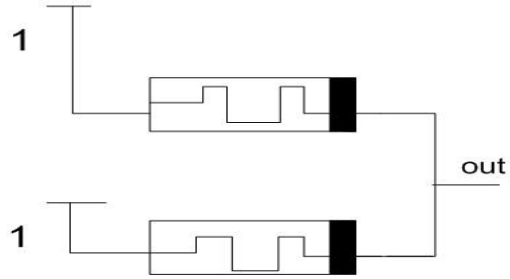

Fig 6: Memristive AND logic with 1 as Inputs

When uncommon inputs are applied to the memristor Fig 7, then there will be increased resistance and decreased resistance on the other side and there will be no output.

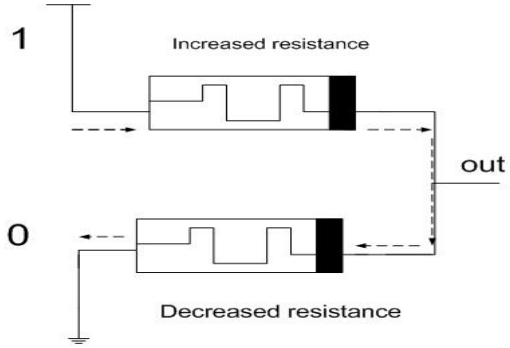

Fig 7 Memristive AND logic with one Input as 1 and another as 0.

B. Logic OR

Consider [12] for the OR gate just interchange the terminals of the memristor, for the case where both the inputs are the same logical value again no current is flowing then again the output will be same voltage as the input voltage, when both inputs are logical 0 output will be logical 0, and both inputs are logical 1 then the output will be logical 1, if consider the

Other two scenarios when the upper memristor input is logical 1 and lower memristor input is logical 0 current will flows from upper memristor to lower memristor, now the upper memristor resistance decreases and the lower memristor resistance increases after enough time will get the minimum resistance Ron in the upper memristor and the maximum resistance for the lower memristor and again it acts as a voltage divider output is logical 1(VCC) as shown in Fig.8

$$V_{out} = V_{cc}\left(\frac{R_{off}}{R_{on}+R_{off}}\right) = V_{cc}\,(R_{off} >> R_{on})\ [4] \qquad \ldots (2)$$

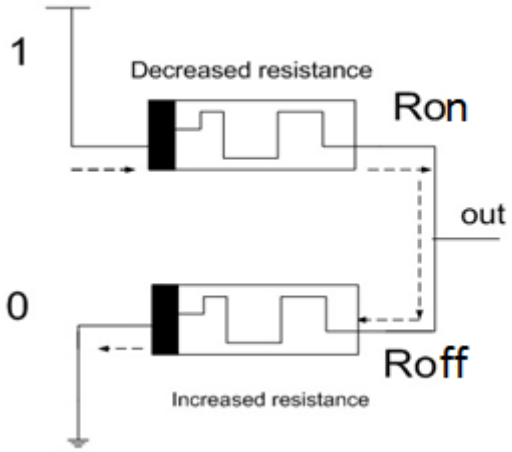

Fig 8: Memristive OR logic with one Input as 1 and another as 0.

Main drawback in the memristive chain is it is not having the property of the signal restoration as memristor is passive element consider if there is 1 percentage loss in stage 1 and 2 percentage loss in stage 2 so this 3 percentage total loss is not restored in the 3 stages, this can be avoided by using the memristor with standard CMOS logic Fig 9 as memristor is having voltage as a logic state.

Idea is to use the regular standard [4] CMOS logic for the amplification in the voltage level, integrating memristor with standard CMOS logic is nothing but to connect the memristor AND gate followed by the CMOS inverter and memristor OR gate followed by CMOS inverter which will be NAND and NOR logic implementation in memristor and CMOS logic as shown in Fig.10

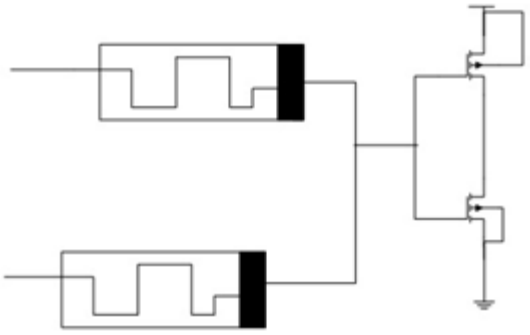

Fig 9: Memristive CMOS NAND logic

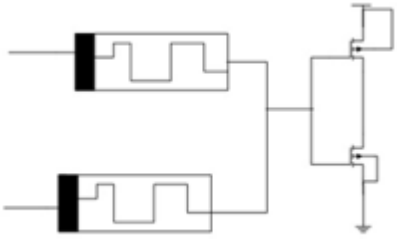

Fig 10: Memristive CMOS NOR logic

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III. *PROPOSED BUILT-IN SELF TEST SCHEME*

A. *Simulation setup*

Cadence:

Cadence tool is used to construct the circuit and analysis its output behavior. It has many kinds of analysis which are needed for the circuit. For us, we mainly did the transient analysis and parametric analysis for finding the appropriate values. We have used the 180nm technology for constructing and comparing.

B. *Simulation Results and Analysis*

Built-in self-test (BIST) is the approach of designing hardware in integrated circuits to allow them for self-testing, nothing but testing their functionality using BIST, thereby no need to connect the external testing equipment. BIST consists of three main blocks named as test pattern generator, unit under test and output response analyzer in this letter we are presenting the first two blocks which is test pattern generator and unit under test.

Test pattern generator can be implemented using the linear feedback shift register where we have two types which is internal XOR linear feedback shift register and external XOR linear feedback shift register, in case of the internal XOR linear feedback shift register the XOR gate is placed in between the D flip-flops so that we will get more test patterns, where we will present the fourth flip flop at the initial state (0001) and the feedback continues(1100), we can take output from all the four D flip-flops we will get approximately 15 different test patterns when using four D flip-flops as shown in Fig.8

The built-in self-test consists of the following

1. LFSR
2. XOR
3. MUX

The following circuits are being implemented using the memristive-CMOS logic by starting with the construction of the basic modules such as AND, NAND, MUX etc.

AND circuit is constructed using two memristors connected and output is taken at the common end as shown in Fig.11. The AND circuit constructed is the basic module in the construction of the NAND gate which will be used in theD-flip-flop.

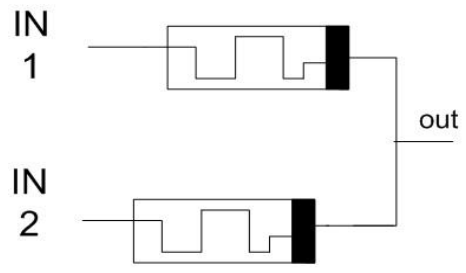

Fig 11: Memristive AND logic [17]

The waveform we get after doing the analysis of many values as shown in Fig.12

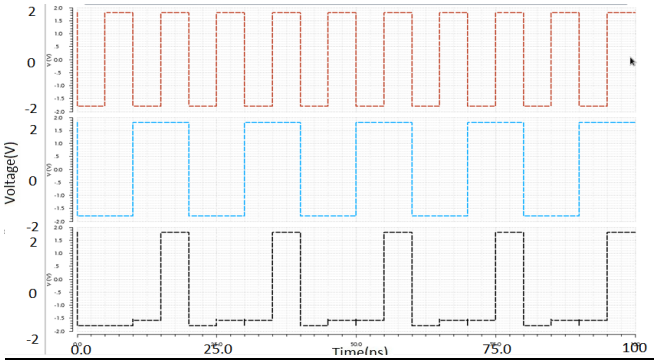

Fig 12: Memristive AND logic Output waveform

The NAND circuit Fig 13 is implemented with the help of the AND circuit and the CMOS inventor connected before the output. This circuit is used to construct the D-flip-flop in which this is used as the basic module, output waveform for NAND circuit Fig 14.

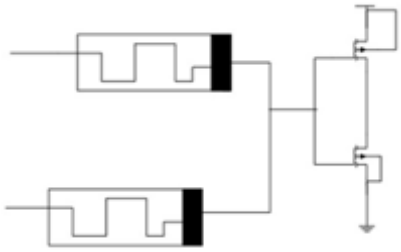

Fig 13: Memristive CMOS NAND logic

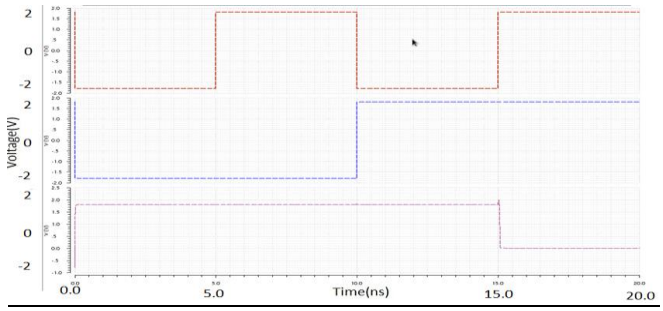

Fig 14: Memristive CMOS NAND logic Output waveform

C. LFSR Implementation

The built-in self-test circuit is used in almost all arithmetic circuits of the modern VLSI industry. The BIST circuit consists of the basic LFSR Fig 15, Fig 16. The LFSR gives the 15 combinations of the output. The LFSR is constructed using the memristive-CMOS logic in which the functionality is verified using the waveforms.

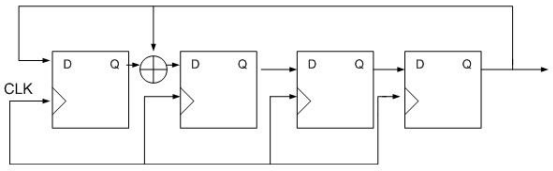

Fig 15: Memristive CMOS 4 bit LFSR circuit

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The LFSR circuit consists of the following

1.D – Flip-flop
2.XOR gate

The two are constructed using the memristive-CMOS logic and they are functionally verified using the cadence tool.

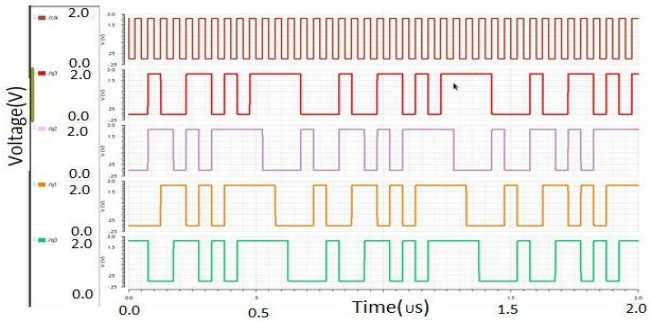

Fig 16: Memristive CMOS 4 bit LFSR Output waveform

By this, the testing of the circuits can be done by giving the pattern generated of this LFSR to the circuits and then the comparison outputs which are also stored in the memory of the arithmetic applications using MUX, which is the future scope of this project.

The MUX consists of the Combinations of the AND gates connected to CMOS logic followed by the inventor and the waveform is observed. In testing the MUX is which, the stored output is selected and the verification is done using the XOR gate. The MUX [17] has 4 inputs and one output. But our BIST circuit needs two inputs and one output. So we have constructed the required MUX which is shown in Fig 17, and Fig 18.

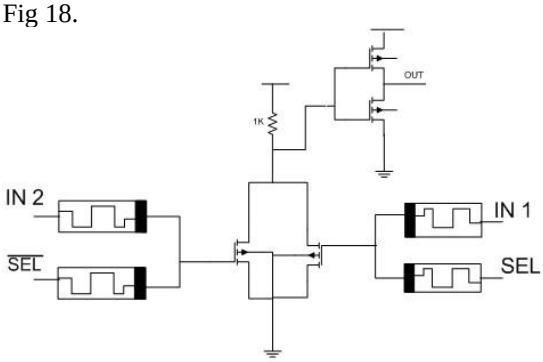

Fig 17: Memristive CMOS 2 to 1 MUX

The circuit is executed and the waveform generated is given to the XOR circuit for comparison.

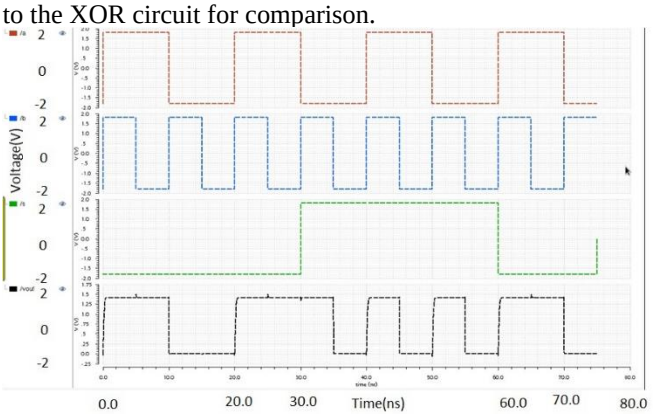

Fig 18: Memristive CMOS 2 to 1 MUX Output waveform

The XOR Fig 19, Fig 20 is circuit is implemented by using the memristive-CMOS logic, which is used to compare the outputs of the tested circuit and the stored memory values. As discussed earlier the MUX output will be given to this XOR gate. Then the output of this XOR gate can be used to see whether the circuit passes the test.

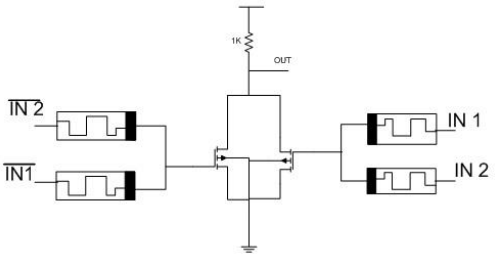

Fig 19: Memristive CMOS XOR logic

The waveform of this circuit as explained earlier is generated in the Fig 20.

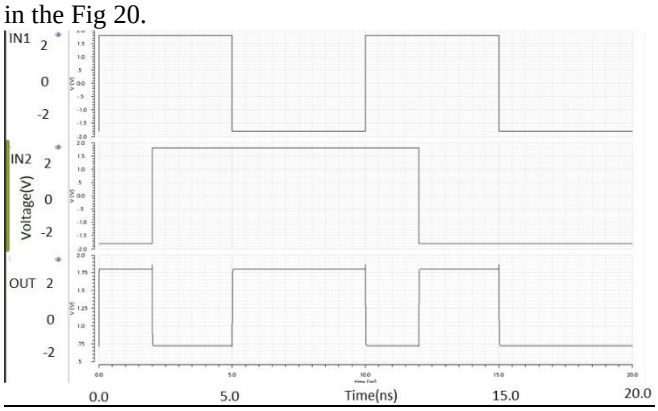

Fig 20: **Memristive CMOS XOR logic Output waveform**

The Encoder Fig 21 is also used in many arithmetic applications such as the adders, multipliers etc.

It compromises of the 4 memristors and the input that we apply.

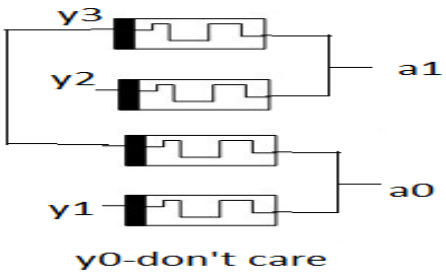

Fig 21: Memristive CMOS 4 to 2 ENCODER circuit

The circuit is made to run under different input combinations and the output is waveform is plotted Fig 22.

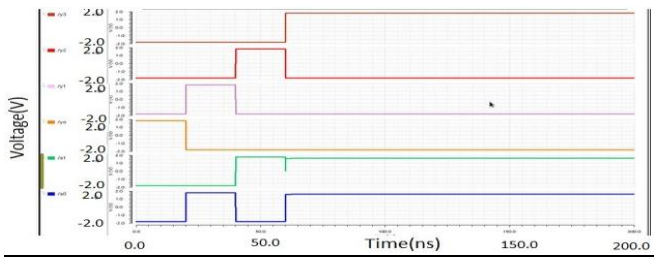

Fig 22: Memristive CMOS 4 to 2 ENCODER Output waveform

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D. Methodology

In this letter, methodologies followed is VTEAM (voltage threshold adaptive memristor) [18] where the logic level will be depending on the voltage across the memristor and CMOS logic (technology node GPDK 180nm).

$$i(t)=\left(R_{on}+\frac{(R_{off}-R_{on})}{(W_{off}-W_{on})}(w-w_{off})\right)^{-1}.v(t) \;..\; (3)$$

$$\frac{dw(t)}{dt}=\begin{cases} k_{off}\cdot\left[\frac{v(t)}{v_{off}}-1\right]^{\alpha_{off}}\cdot f_{off\,(w),0<v_{off}<v} \\ 0,\Longleftrightarrow v_{on}<v<v_{off} \\ k_{on}\cdot\left[\frac{v(t)}{v_{on}}-1\right]^{\alpha_{on}}\cdot f_{on(w),v<v_{on}<0} \end{cases} \quad (4)$$

K off and k on and alpha off and alpha on are constant threshold level voltage v off and von, f on, f off are window function depend on state variable boundary state depend on variable w off and won.

C.Power Delay Comparison (u watt, p sec):

The power and delay of the CMOS logic Fig 23 and the hybrid logic[19] is compared in the table 1 and table 2 in which the hybrid memristor is far better than the CMOS logic implementation. The power consumption is reduced to nearly 70 percent.

Table 1: Power Delay Comparison.

CMOS			HYBRID MEMRISTOR	
CIRCUIT	POWER	PROPAGATION DELAY	POWER	PROPAGATION DELAY
NAND	3.288uwatt	315.62psec	0.6uwatt	223.4psec
NOR	3.43uwatt	393.63psec	0.8uwatt	330psec
XOR	5.72uwatt	440psec	1.32uwatt	400.4psec
MUX	20.8mwatt	437.4psec	1.5uwatt	405.3psec
ENCODER	24.37mwatt	201.3psec	1.93uwatt	170.3psec

Many arithmetic circuits constructed with these outputs may have a lesser delay and power consumptions, and the testing of these circuits also can be done quickly.

D.Area Comparison (um):

The area comparison Fig 24 is done by the reference of the [6], in which the memristive-CMOS logic has also had a considerable reduction in the area.

Table 2: Area comparison.

NAME OF THECIRCUIT	MEM-CMOS(um)	CMOS(um)
NAND	4.8	8.5
NOR	4.8	8.5
XOR	6.8	11.8

IV. FUTURE SCOPE

The memristor is popular as a fourth fundamental circuit element and a strong candidate for the next generation memory and logic applications. After its first physical realization by HP group, different research groups around the globe have found out many interesting applications in various domains such as 3D memories,

In-Memory computing, neuromorphic applications, nonlinear dynamics, biomedical applications, soft computing, programmable analog circuits[20] etc. This property can also be utilized for the different logic application such as IMPLY[21] logic and MAGIC[22,23] logic, Akers Logic, Boolean logic[24] etc. Some recent studies show that scaling limit and a limited number of read-write cycles of flash memory forces to find new alternatives of denser with faster memories. Extending memristor CMOS standard logic to more complex combinational circuits like more inputs decoders which can be used in the memory design for addressing the crossbar where we use the row and column decoders and built-in self-test with all three blocks test pattern generator and the unit under test and output response analyzer implementation with memristor and CMOS standard logic.

V. CONCLUSION

We herewith investigated the design of combinational logic circuits using the emerging nano-device called memristor and CMOS device. Additionally, we proposed the built-in self –test circuits to test the core functionality of the logic gates. The investigated methods were validated with generic, efficient and analytically simpler VTEAM model for the memristor. As we have used generic model for memristor, it can be quickly adapted to any other memristor model available in the literature. This research work can be extended to test the memristor specific faults such as read disturb fault, write disturb fault, SET fault and RESET fault etc.

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