Layout Optimization using Euler's Path and Minimum Distance Rule

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Abstract*: Layout is an important step towards Integrated Circuit(IC) designing. The following research work focuses on the techniques that can be applied on layout to optimise the digital IC. The work discusses about other methods as well that are proposed to optimise ICs. However, this research work shows a step-by-step approach in implementing Euler's Path and Minimum Distance Rule. It targets the change in the switching power, layout area and delay in the circuit to show the effect of the proposed methods. Euler's Path and Minimum Distance Rule are the two techniques that are used on an example circuitry that implements (AB+CD)' Boolean expression. Cadence Virtuoso simulation tool is used for simulations and quantitatively analyse the mentioned parameters. Post layout simulations are used to get more realistic results because it takes parasitic elements into account as well. The results from layouts with and without the above techniques applied, is compared, showing a decrease in switching power, delay and layout area for the circuit with the optimization techniques. The results in this work show that with improvement in layouts of digital ICs, we can make ICs more reliable. More complex circuitry will benefit from these techniques because they will need lesser layout area which will aid in adding more circuitry and increasing the complexity further more.

Index Terms: Delay, Euler's Path, Layout, Minimum Distance Rule, Switching Power.

I. INTRODUCTION

Today, because many entire chips are printed at once, the cost of chips is proportional to the chip area, rather than the number of transistors, this makes the design process crucial and its optimization necessary [1]. Various processes are involved in the manufacturing an IC. Layout decides the placements of different IC components on the silicon wafer. It is an important physical design step for an IC. It is the representation of the IC in planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit [2].

System on Chip (SoC) technologies are dependent on the reduction of chip area because an exorbitant amount of transistors are used to make them, fitting all the required modules is crucial. Layout optimization helps in reduction of chip area which in turn will help in appending more circuits in the same chip. The growing requirements for Digital Signal Processing (DSP) processors have made it compelling to design ICs with less delay and faster response time. Faster response time can be obtained by increasing the channel width and decreasing the channel length, but increasing the channel width will result in the increase in IC area and decreasing the channel length will lead to channel length modulation. Delays are not only affected by the channel by also by the parasitic elements introduced during fabrication. Post layout simulation will show the parasitic elements. An optimized layout will aid in decreasing the delays in the circuit and give a higher response time. Many enhancement techniques are proposed to improve the performance of the circuits. Improving layout can significantly shrink the area and also elevate the performance of ICs. There are other methods like those explained in [3] and [4] which modify the Boolean expression by Functional Composition and Kernel Finder respectively. This is to be noted that Kernel Finder reduces the number of transistors for a particular Boolean expression implementation [5]. But these methods focus on optimizing the circuits and not their layouts. Wire-length Minimization and via minimization can optimize VLSI circuits [6]. These techniques not only optimize the circuits by reduction in the probability of short-circuit faults but also increase VLSI circuit yields. By using memetic algorithm in partitioning large systems and floorplanning their subcircuits further enhances on wire length minimization [7]. But wire-length minimization is effective for VLSI technologies less than 0.5 micrometer [8]. In layouts, the placement of the layout elements plays a very important role. It becomes the deciding factor for having better yield or better performance [8]. Euler's Path significantly optimizes the layout design. Euler's Path is a graphical method which states that every node and edge must be transversed at least once without repeating the edges [5] [9]. The complementary MOS circuit is divided into two parts- the nMOS pull down network that pulls the output to the ground and the pMOS pull up network which pulls the output to the voltage source. Two different graphs are created for each network where the gate and the interconnection between the source and the drain are represented by the edges. The drain and the source are represented by the node. The path that is followed in the pull up network must be followed in the pull down network as well. Minimum distance rule is a layout method to reduce layout area significantly. Some examples of minimum distance rule in Cadence® virtuoso® 64(180nm) are-

- Poly to Poly spacing must be greater than or equal to 0.3µm.
- Metal to Metal spacing must be greater than equal to 0.3µm.
- N-well to Oxide spacing must be greater than or equal to 0.5µm

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- N-well to N-well spacing must be greater than or equal to 1µm.
- Nimp to Nimp spacing must be greater than equal to 0.4µm [10].

Layout Design Rules must be followed during layout in order to avoid problems during the yield process. These guidelines basically specify the minimum width and minimum spacing between layout elements. According to Minimum Distance Rule by placing the layout elements equal to or slightly more than the distance, specified by the Layout Design Rules, will produce better layout. This paper proves how Euler's Path with Minimum Distance Rule optimizes layout. The work here focuses on switching power, delays and layout area for comparison.

A. Prior Work

R.H. Khade and D.S. Chaudhari show how Euler's Path can be used to decrease the area of layout [11]. It shows how a layout without diffusion breaks results in a smaller layout area. It explains a novel methodology of constructing a stick diagram for better implementation of Euler's Path Rule on complementary MOS logic circuit. But it does not show results on how Euler's Path has helped in decreasing the parasitic elements. The work focuses more on area aspect of the layout but shows less electrical related results. The work shown here is tested on industrial grade software which not only shows reduction in layout area but also gives electrically important results.

II. METHODOLOGY

This research work has been carried out in 180nm technology with an example circuitry having an expression (AB+CD)'. Below the steps carried out are illustrated.

Step 1: Creating the schematic of the circuit in Cadence® virtuoso® 64.

Cadence® virtuoso® 64 is a powerful tool for simulations of circuits, creating layouts and calculating various other parameters like switching power and delays in the circuit. The expression implemented is shown in Fig. (1). The schematic was simulated in ADE XL simulation tool with a transient time of 160ns where the pulses given to each gate has a period of 20ns with 100ps as their rise time and fall time and 0ns as their delay. The result is shown in Fig. (2).

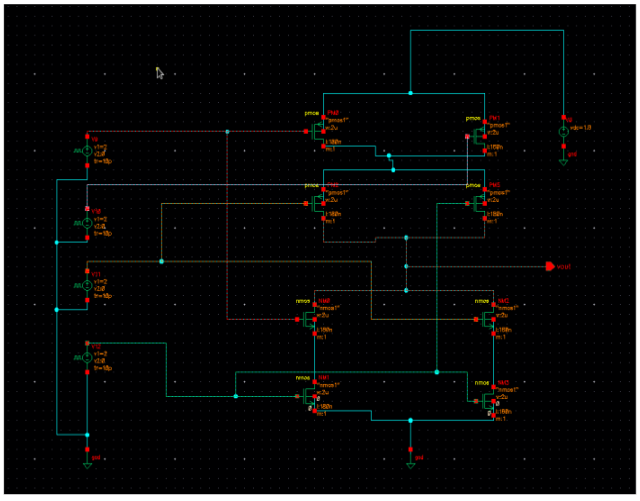

Fig (1): Schematic in CAD tool

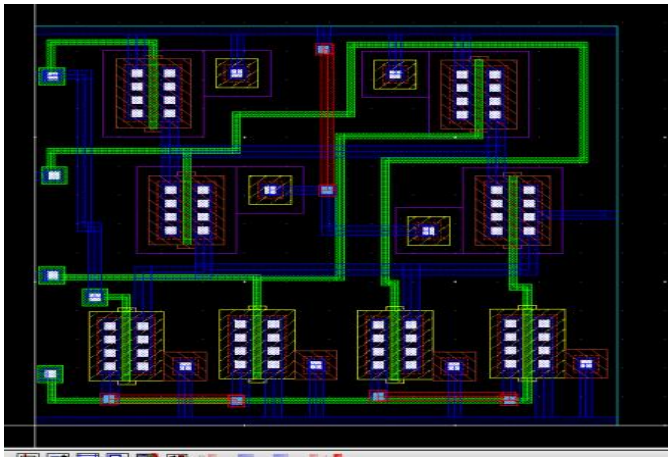

Fig (3): Layout

Step 2: Creating the layout and its physical verification.

After the simulation, the layout is created from the LAYOUT XL option of the CAD tool. Layout window was accessed and the layout was made with metal layouts and contacts. The drain, source, output and voltage source are connected with metals. The body of nMOS and pMOS are n-well and p-well respectively. The gates are connected with poly and for a poly and metal contact via are used.

Fig. (3) shows the layout of the given boolean expression. After the layout creation, physical verification has been carried out to check the quality of the layout using Cadence Assura which checks the Design Rule Check (DRC) and Layout Versus Schematic (LVS).

Design Rule Check checks physical layout of a particular chip layout satisfies a series of recommended parameters called design rules [12]. LVS determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design [13].

Step 3: Post-layout extraction.

Once the layout is made, its extraction gives the extracted view that contains the parasitic elements that arise due to the placement of the layout elements. Extraction was done for this layout to get a more realistic result. Assura's Quantus Extraction Solution (QRC) tool was used that generated the extracted file with all the parasitic capacitance and resistance. The extracted file is shown in Fig. (4). Fig.(5) shows a magnified image of the extracted view so that parasitic elements can be displayed. The above steps were for creating the extracted file for the layout without any

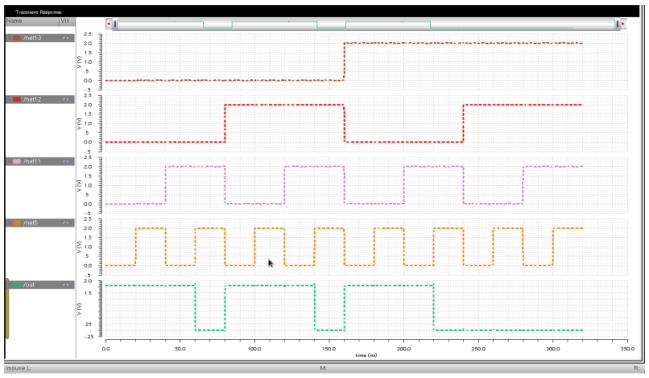

Fig (2): Simulation result in graph.

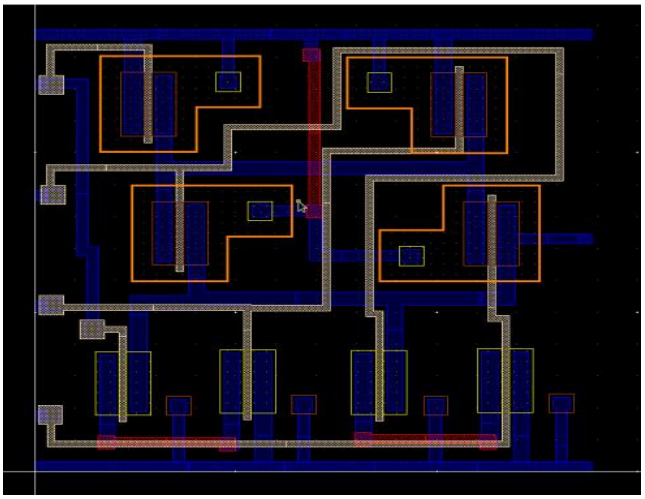

Fig (4): Extracted view of layout

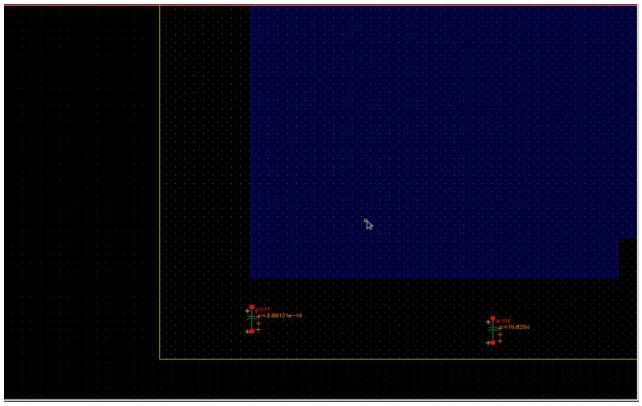

Fig (5): Magnified Extracted view of Layout

optimization. The next steps illustrated below shows the implementation of Euler's Path and Minimum Distance Rule in the layout on same Boolean expression.

Step 1: Making the Euler's Graph

The Euler's graphs are made for the pull up network and the pull down network. The edges have been labeled by the gates they represent. The graph is shown in Fig.(6)

The path taken for this Boolean expression is [C B A D]. Note that both the paths are possible, in accordance with the Euler's Rule, in nMOS logic and pMOS logic. This sequence is now used to make the stick diagram.

Step 2: Creating the stick diagram.

A stick diagram, shown in Fig.(7), is a means to express the layout information through the help of color lines/sticks. The metals are represented by blue lines, the red lines represent poly, the yellow represent p- diffusion and green represents n-diffusion.

Step 3: Creating the schematic.

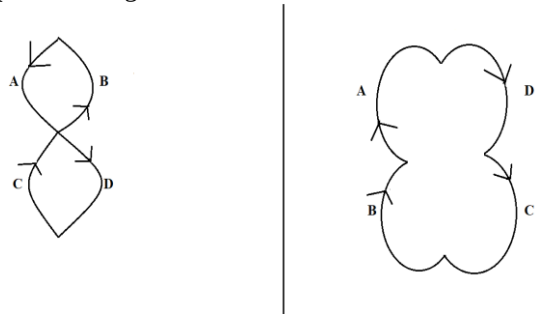

Fig (6): pMOS network on the left and nMOS network on the right

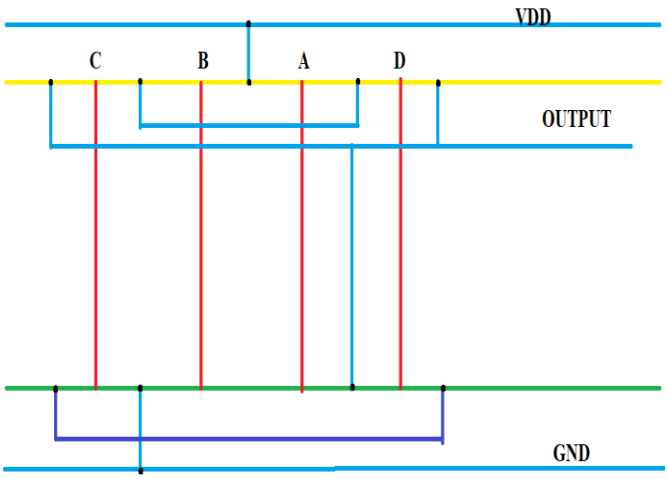

Fig (7): Stick diagram

According to the stick diagram, the new schematic, shown in Fig.(8), aids the Euler's path and will be helpful in creating the layout in the Virtuoso tool. The schematic is created keeping in mind the Euler's Path and then placing the input pins accordingly.

Step 4: Layout creation.

This layout involves the technique of depletion sharing. By this method the pMOS and nMOS transistors can be arranged in a single row similar to the stick diagram. This also reduced the number of bulk as one bulk each for nMOS and pMOS is enough for the entire array of transistors. Minimum distance is applied to the layout. The placement of the layout elements is done in the way by which they are having spacing between them which is equal to or slightly greater than the minimum distance specified by the Layout Design Rule. Fig. (9) shows the layout with above mentioned methods.

Step 5: Extraction of Layout

The extracted view for the optimized layout is created by the Assura's Quantus Extraction Solution QRC tool.

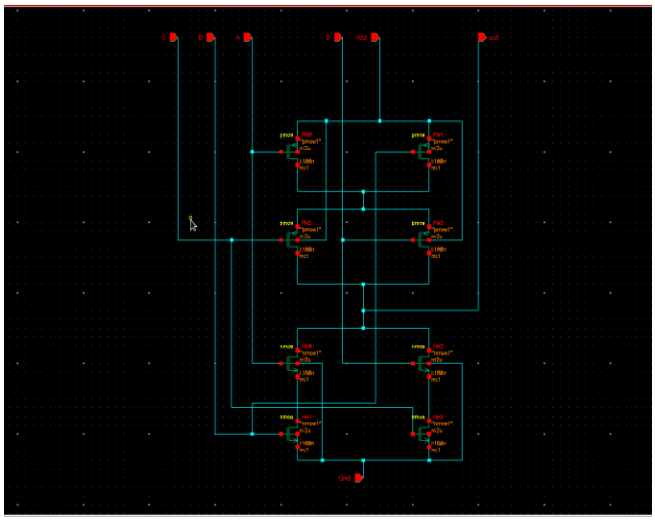

Fig (8): Euler Path influenced Schematic

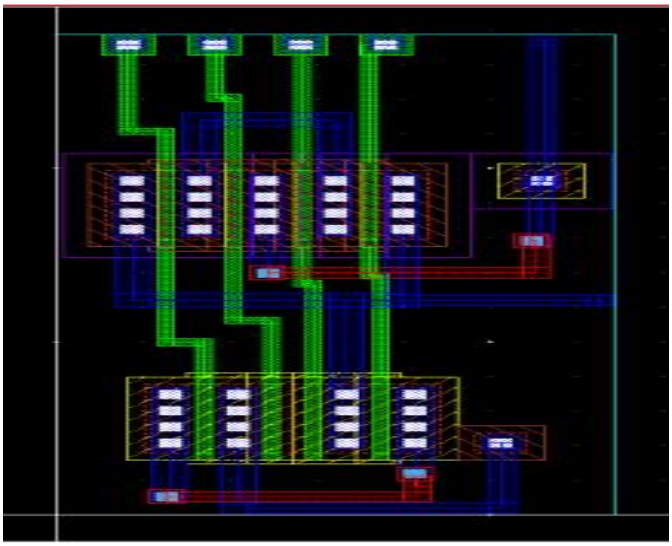

Fig (9): Euler's Path and Minimum distance Rule Implemented layout.

The extraction file used coupled cap extraction mode for realistic results and included the cross-talks problems caused by coupling parasitic capacitances. Fig. (10) and Fig.(11) show the extracted view of the layout with Minimum Distance Rule and Euler's Path by depletion sharing.

All the extracted files are simulated by Analog Development Environment L (ADE L) tool of Cadence Virtuoso. The extracted files are added to the simulator. 320 nanoseconds is taken as the transient time, their respective switching power and delays are calculated.

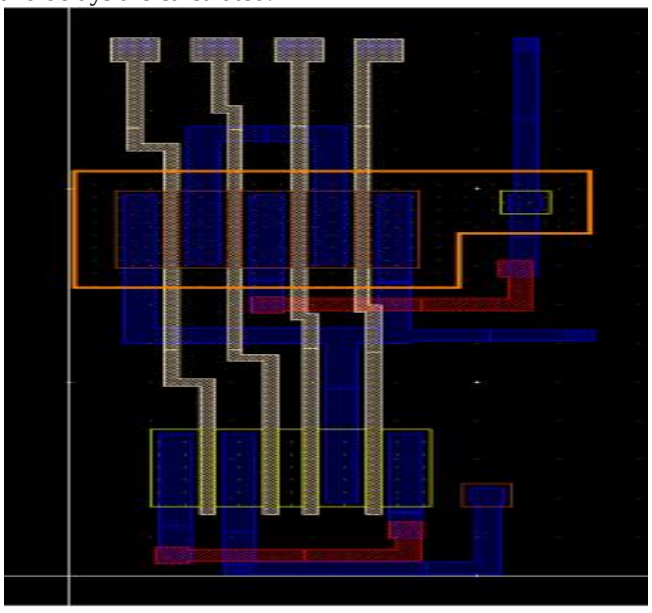

Fig (10): Extracted View of layout

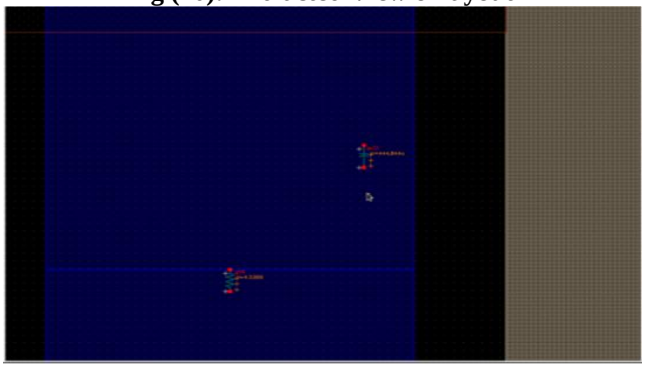

Fig (11): Magnified view of the extracted layout.

The delay is calculated for the second rising edge of the 4th wave, that is the D input, and the first falling edge of the output, see Fig.(2). The switching powers are shown in figure Fig. (12).

III. RESULTS AND DISCUSSIONS

The table 1 shows the power and delay of schematic without the extraction of layout and schematic with extraction of layout without any optimization techniques on it.

It is seen that there is a higher switching power and delay for the circuit with an extracted layout than circuit with just schematic. This is because the circuit with only schematic does not contain parasitic elements that are responsible for higher delays and switching power. The result for extracted layout presents a more realistic result than the idealized schematic result. The table 2 compares the power and delay for circuits with optimized layout and circuit without any optimization methods mentioned here. It also shows the comparison between the areas of layout without optimization, the boundary was allocated automatically by the Layout XL tool PR boundary and layout after applying the optimization techniques. The area was measured by ruler provided the Layout XL tool. Fig. (12) (a) illustrates the area occupied by layout without optimization and Fig.(13) show the layout with optimization.

The table 2 shows that there is a vast difference between the delays and power of layout with and without optimization. The layout with Euler's Path by depletion sharing and Minimum Distance Rule has a lot less power and delay compared to the layout without any optimization. There is a decrease of 5.855% in switching power, 21.839% decrease in delay and 53.588% reduction in layout area. This shows that Euler's Path and Minimum Distance Rule are effective methods in optimizing the Layout Design and also decreasing the layout area.

It is evident that if these optimization techniques are used for systems with greater number of transistors, their performance will improve greatly and the area occupied will also be drastically less.

Table 1: Power and Delay Comparison.

Parameter	Schematic only	Layout without Optimization
Power (µW)	617.301	675.750
Delay (ps)	29.470	41.210

Table 2: Comparison between layout width and without optimization

Parameter	Layout without optimization.	Layout with optimization.
Power (µW)	675.750	636.183
Delay (ps)	41.210	32.210
Area(sq µ m)	192.238	89.221

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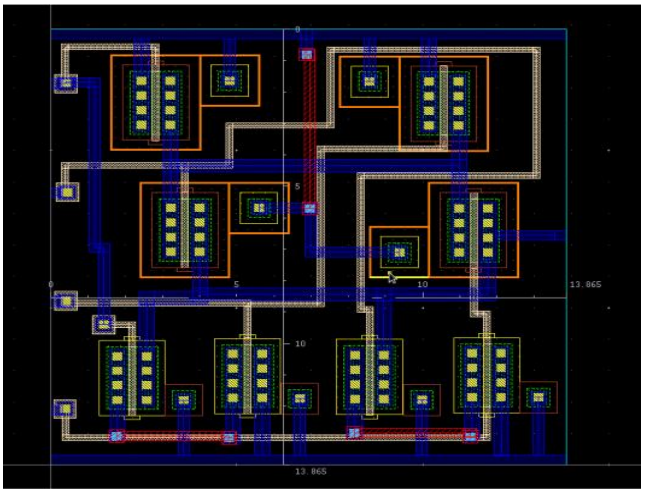

Fig (12): Area with ruler tool Layout without optimization

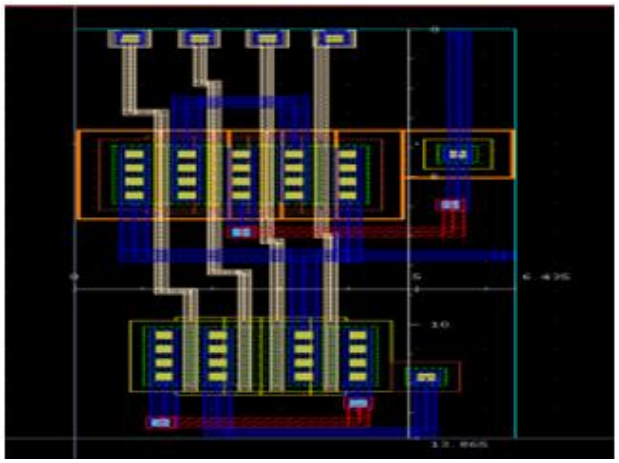

Fig (13): Optimized Layout with ruler.

IV. FUTURE WORKS POSSIBLE

Future work will include the automation of Layout with Euler's Path and Minimum Distance Rule which can decrease the time required to design the layout. Automating the Layout design with Euler's Path is shown in [5]. Adding Minimum Distance Rule will help in decreasing the white spaces automatically rather than manually checking for minimum space between the layout elements and then placing them. This way the optimizations can be applied on chips manufactured in the industry and can be applicable on any project conveniently.

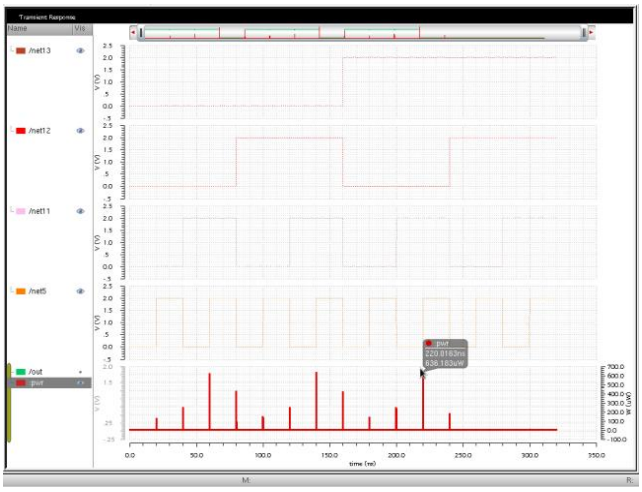

Fig (14): Switching Power of Output

V. CONCLUSION

The work here shows a bipedal technique for layout optimization. A Boolean expression was implemented without any layout optimization techniques. The switching power, delay and layout area were measured. This data, after being compared with a layout where the optimization techniques are applied, shows that these techniques are effective and improve the performance of the circuitry. Euler's path is applied to the layout of the circuit with the aid of a stick diagram which helps in the placement of the elements throughout the layout and connecting them easily. Minimum Distance Rule upon applying on the layout resulted in the removal of white spaces and hence, resulting in the reduction of the layout area by 53.588%. The post-layout simulation results in Cadence Virtuoso demonstrate improvement in terms of switching power and delays, proving the effectiveness of the proposed techniques. It is concluded that by application of the mentioned techniques we will make the digital ICs more reliable, enhance its performance and can make room for more circuitry. These techniques can be used in industries with automation for quicker and optimal post layout designs.

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