A Study and Hardware Implementation of Enhanced Isolated Boost DC-DC Converter with the Reduced Number of Switches

I. Gerald Christopher Raj, P. Soundar Rajan, G. Praveen Raj, J. Anjel

Abstract: ***For voltage gain utilization, the originators are foremost half lean towards the DC-DC boost converter. In any case, it needs the restriction in Vout by the additional transferral proportion, diminished efficiency and its necessity of voltage and current for response signals, that makes composite control system by means of expanded by and large expense. Besides, the Vout and efficiency are diminished because of the self- parasitic nature of power circuit parts. To overcome these disadvantages, this paper gives the theoretical enhancement and hardware execution of the DC-DC boost converter with the reduced number of switches circuit for acquiring high Vout and high enactment. The proposed circuit munificently will increase the high Vout by VDR with a closed loop proportional-integral controller. The converter circuit together with a closed-loop PID controller is created within the hardware prototype model. A point by point execution examination was completed under resistive loading conditions. Numerical verification results gave during this paper demonstrate the incredible course of action in the circuit with a theoretic circumstantial.***

Index Terms: ***DC to DC power conversion, voltage fed full-bridge (VFFB) converter, galvanic isolation, high- frequency step-up transformer, voltage doubler rectifier (VDR).***

I. INTRODUCTION

Renewable energy sources are splendid decisions contrasted with non-sustainable energy sources since they are endless and they do not contaminate our air and water like way consuming petroleum derivatives will do. To make any sustainable power system efficient, they need to have the appropriate converter. Assorted high increase DC-DC converters have been proposed to vary over the low voltages into a constant DC bus voltage. DC-DC converters are a progressively essential part in power electronic interfaces, for example, photovoltaic power systems and fuel cells. The converter should be able to do high control activity operation with a high voltage conversion proportion.

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High boost DC-DC conversion techniques are required in few applications for example fuel cells (FCs), medical types of equipment, solar photovoltaic (PV) systems and uninterruptible power supplies (UPS). For isolated topologies that give galvanic isolation, voltage-fed full-bridge (VFFB) and current-fed full-bridge (CFFB) DC-DC converters square measure normally utilized used. Since the significant voltage gain of the VFFB DC-DC converters is equipped by a high-frequency transformer with a high turn extent. To improve the voltage boost ability, a boost converter or an active-clamped three-level rectifier is related to the secondary side of the VFFB DC-DC converter. Also, the input current swells and turn ratio of the CFFB are lower than VFFB DC-DC converters. The CFFB converters, in any case, the resonance between the discharge inductor of the transformer and therefore the output capacitance of the primary switches reasons voltage spikes in the devices. To retain the voltage spike in CFFB converters, a passive snubber is employed, which causes power loss. To recover the imperativeness of the snubber in CFFB converters, active clamping circuits with extending size and cost have been proposed. In an attempt and avoid the need to use the active clamping circuits, soft-switching snubberless naturally clamped VFFB converters have been proposed.

The DC-DC venture-up (boost) power converter definitely bears the confined Vout because of the transferal gain proportion. Each output voltage and efficiency is additionally a lot of lessened because of the self-parasitic behavior of the facility circuit elements. Additionally, two sensors voltage and the current which are crucial for the controller calculation which increases the complication and overall expense of the system once exposed to high-voltage applications. Voltage Doubler Rectifier actualized in power circuit style of electronic elements is incorporated to DC-DC power circuit system recently. This gives a chance to structure high-voltage DC to DC converter circuit. Alternative solutions are also creating in kinds of literature to extend the V_O, notably on separating the load side so as to confirm the high-voltage procedure of the DC to DC converter. Whereas the other authors centered over the boost-strap capacitors, control molding, and the high-recurrence transformers. The half bridge is utilized for turned on/off alternative with a phase shift for conversion of the source for each cycle any of the switches is turned on. At the point when the SW1 is turned on the input section acts as the traditional boost converter and the voltage is kept in

input inductor and therefore the capacitor C1 as SW2 is turned on the voltage across the capacitor; C1 and C2 are accused and discharges through the transformer. The elective switching produces a difference in change of current across the transformer with a high frequency. The transformer is employed to step up with a limited gain, to resolve the size issues. The secondary side has a voltage doubler that doubles the input voltage twice. The LLC resonant converters are proposed that appropriate for high-voltage applications. Still, they need incredible execution simply round the resonant frequency in order to obtain high frequency. To induce M (gain), transformer magnetizing inductance ought to be very little that ascents magnetizing current and better conductivity and core losses. The execution of the proposed isolated boost dc-dc converter with a reduced range of switches is advantageous as compared to existing dc-dc configuration as:

[1] Increased voltage transfer (k) gain proportion.

[2] The big selection of control and lessened swell elements at the outputs.

[3] Increased power density likewise efficiency.

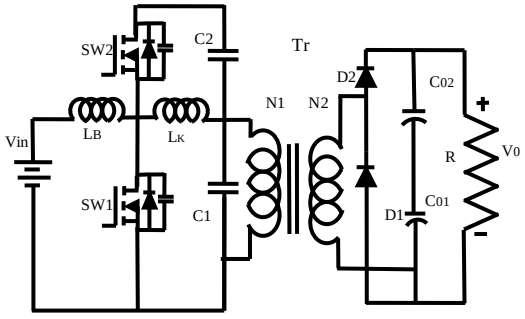

Fig. 1 Proposed two-switch, isolated boost DC-DC converter

II. PARAMETER DESIGN

A. Theoretical Analysis

[1] Comparison between switching losses reverberation procedures

Off-ramp and conductivity loss of the switches are briefed by the following derivations

$$P_{turn\ off} = \frac{1}{2} V_{turn} - V_{off} i_{turn\ off} \left(\frac{t_r}{T_s}\right) \quad (1)$$

$$P_{conduction} = R_{on} I_{rms}^2 \quad (2)$$

Where $V_{turn\text{-}off}$ and $i_{turn\text{-}off}$ at off-ramp moment, separately and t_r is upswing time. The t_r is limited to the switch's characteristics, but $V_{turn\text{-}off}$ and $i_{turn\text{-}off}$ rely upon converter's operation characteristics. Ron is conduction resistance of the switch. Thus switch losses will be acquired from,

$$P_{\_conduction} = P_{\_turn\ off} + P_{\_condction} \quad (3)$$

Reverberation processes of converters in directly above-resonance and less-resonance are inspected about their preferences and impediments are referenced. Task of Sw1 and Sw2 in diverse resonant approach is depicted individually. Thus, working in overhead-resonance can cause high switch misfortune. Obviously in beneath-resonance circumstance, Turnoff Current is way lower and variation of RMS current in every action modes is phenomenally low. To accomplish slightest switch loss, Sw1 must operate in under resonance to fulfill the accompanying state:

$$f_{r1} > f_s / 2D_{min} \quad (4)$$

Where D_{min} is least obligation cycle and f_{r1} (Resonance frequency for C1 and L_k) stated as follows:

$$f_{r1} = 1/2\pi\sqrt{L_K C_1} \quad (5)$$

By working indirectly above reverberation Sw2 can have +ve Turnoff Current. TOC in beneath reverberation is -ve. Thusly, Zero Voltage Switching condition for Sw1 is disposed and switch loss of Sw1 can rise and RRL of Sw2 the diode can build switch misfortune as well. Subsequently, Sw2 ought not to operate in beneath-resonance; along these lines, it needs to operate in above-resonance. In spite of the fact that in frequencies between two hundred fifty kHz and three hundred kHz Turnoff current is low, by diminishing obligation sequence it should be workable for Sw2 to arrive the underneath timbre area, prompting a rise in switch loss. The resonance frequency of C2 and Lk (f_{r2}) ought to be picked far away from limit frequency to guarantee the accompanying in-condition.

$$f_{r2} > f_s / 2(1 - D_{\min}) \quad (6)$$

f_{r2} is expressed as

$$f_{r1} = 1/2\pi\sqrt{L_K C_1} \quad (7)$$

Additionally, it will be appeared by operating in lower frequencies for f_{r2}, examination, and regulator of the projected converter will be more straightforward.

[2] ZVS Condition

As indicated by interval 5, once switch Sw1 cracks this OFF the current of LB moves through the D2 of Sw2, and therefore C2 of Sw2 and Sw1 are released and charged severally. Therefore the accompanying condition ought to be fulfilled with ensuring ZVS for Sw2.

$$-i_{s2}(t_4) = i_{lk}(t_4) - i_{in}(t_4) = i_1 - I_{in} \quad (8)$$

The current of the physique diode of Sw1 is dependably I_{in}, so this suggests ZVS for switch Sw2 accomplished for various stack collection (in the next section the demonstration is about i1= $2I_{in}$). At t_0 when Sw2 turns OFF, reference of i_{in} and i_{lk} variety flows through the physique diode of Sw1.

$$\frac{1}{2} L_B I_{LB}^2 = \frac{1}{2} L_B (I_{in})^2 > \frac{1}{2} c_{0ss,total} \left(\frac{V_{in}}{1-D}\right)^2 \quad (9)$$

$$C_{oss,total} = C_{oss,s1} + C_{oss,s2} \quad (10)$$

C_{oss} establishes the consistency of the Zero Voltage Switching condition of a lesser switch inside the entire load shifts.

[3] Voltage Gain

During the time $(1 - D)\ T_s = t_6 - t_4$ it can be said that,

$$(i_{c2}) + (I_{in}) = (i_{LK}) \quad (11)$$

The regular current of Sw2 is zero since it's in series with C2 (C2 = *i*Sw2). Amid the time $(1 - D)$, the average current of I_{lk} is equivalent to I_{in}, at that point

$$\frac{1}{2} i_1 (1 - D) T_s = I_{in} (1 - D) T_s \quad (12)$$

$$i_1 = 2I_{in} \quad (13)$$

By KVL law:

$$\langle V_{in}\rangle = \langle V_{LB}\rangle + \langle V_T\rangle + \langle V_{Lk}\rangle + \langle V_{c1}\rangle \quad (14)$$

$$\langle V_{in}\rangle = \langle V_{c1}\rangle \quad (15)$$

From t4 to $t6$ interval Iin flows through C1 and afterward current of C1 bounces to $i1$ after that diminishes straightly to zero, at the same time voltage of capacitor C1 amid the time $t4$ to $t6$ increases directly and after that it resonance and achieves its crest at $t2$, its base occurred at $t3$ and it would be consistent as far as possible of period. Amid t4 to $t6$, the voltage of C1 increases directly. The time interval between $t0$ to $t2$ is excessively short thus it very well may be accepted that throughout this V_{C1} is consistent.

$$\Delta V_{c1} = \frac{I_{in}}{c_1}(1-D)T_S \quad (16)$$

$$V_{c1}' = V_{c1}(t_0) = V_{in} + \frac{\Delta V_{c1}}{2} = V_{in} + \frac{I_{in}(1-D)T_S}{2c_1} \quad (17)$$

By the volt-second produce calculations on V_{c2} and from Figure 3.6, relationships among V_{01}, $V_{02,}$ and V_0 can be easily obtained as follows

$$V_{01} = (1-D+d_1)V_0 \quad (18)$$

$$V_{01} = (D-d_1)V_0 \quad (19)$$

And also V_{C2} can be represented as

$$V_{c2} = \left(\frac{D}{1-D}\right)V_{in} \quad (20)$$

$d1$ can be obtained as follows

$$d_1 = \frac{(1-D)\cdot\left(\frac{D}{1-D}V_{in} - (D-d_1)V_0/n\right)}{(D-d_1)V_0/n + V_{in} + \frac{I_{in}(1-D)T_S}{2c_1}} \quad (21)$$

Also

$$I_0 = \frac{1}{2}i_{D1(peak)}\cdot(1-D+d_1) \quad (22)$$

The output current can be acquired as a purse:

$$I_0 = \frac{\left[\frac{D}{1-D}V_{in} - (D-d_1)V_0/n\right]}{2nL_K}\cdot(1-D)(1-D+d_1)T_S = \frac{V_0}{R_L}$$

The voltage gain will be expressed as:

$$M = \frac{D}{\left(\frac{2nL_K f_s}{R_L(1-D+d_1)} + (D-d_1)\frac{1-D}{n}\right)} \quad (23)$$

[4] Input current ripple

Amid the time DTs switch Sw1 active and therefore the voltage crosswise over is Vin. Thus input current swell might be inferred as pursues:

$$\Delta i_{in} = \frac{V_{in}}{L_B}DT_S \quad (24)$$

[5] Voltage and current stress of semiconductors

By applying KVL on Sw1, Sw2, $C1$, and $C2$ at $t3$, the most extreme voltage of two switches can be communicated as below

$$V_{s1,max} = V_{s2,max} = V_{c2}(t_2) + V_c' = V_{in} + \frac{I_{in}}{2c_1}(1-D)T_s \quad (25)$$

In Zero Voltage Switch form, turn-on losses will be abandoned however ramp losses remain. So, it is vital to get TOV and TOC. As represented TOV of Sw1and Sw2 occurs at t4 and t0, respectively

$$V_{S1,turn-off} = V_{c2}(t_2) + V_{c1}(t_4) = \frac{D}{1-D}V_{in} + V_{in} - \frac{I_{in}}{2c_1}(1-D)T_S = \frac{V_{in}}{1-D} - \frac{I_{in}}{2c_1}(1-D)T_S \quad (26)$$

$$V_{S2,turn-off} = V_{c2}(t_3) + V_{c1}(t_0) = \frac{D}{1-D}V_{in} + V_{in} - \frac{I_{in}}{2c_1}(1-D)T_S = \frac{V_{in}}{1-D} + \frac{I_{in}}{2c_1}(1-D)T_S \quad (27)$$

Most extreme current of SW1 occurs amid t2 to t3

$$I_{s1,max} = I_{in} + \frac{V_{0s}/n - V_{ds}'}{\sqrt{L_K/c_1}} + I_{in+}\frac{\left[(1-D+d_1)V_0/n)V_{in} - \frac{I_{in}}{2c_1}(1-D)T_S\right]}{\sqrt{L_K/c_1}} \quad (28)$$

Ramp off Current of Sw1 and Sw2 and the SW2 is adequate to I_{in}

$$i_{sw1,turn-off} = i_{sw2,turn-off} = i_{s2,max} = I_{in} \quad (29)$$

Most extreme Vd1 is satisfactory Vo.

$$V_{D1,2-max} = V_0 \quad (30)$$

In light of Zero Current Switch in D1, D2 their ramp current is zero. Turn off and V/I of the planned converter switches are differentiated and L-L type HBC. In spite of the fact that TOC in linked with the proposed converter is nearly partial, amount of the switches are twice. Besides, TOV of Sw1 and Sw2 are lower and higher than comparing switches in, individually, and their regular is equal. Completely measures of switches are less than the proposed converter, yet Sw1, Sw2 assessment is higher.

B. Execution and study of proposed DC-to-DC converter

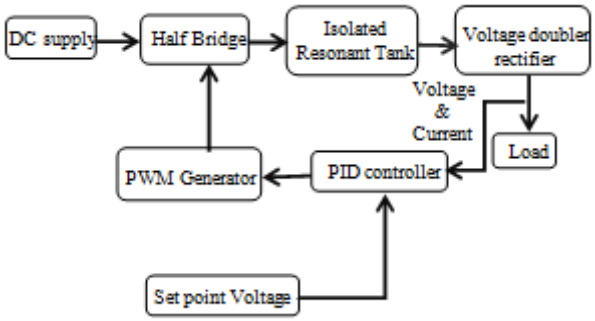

Fig. 2 Block Diagram of closed loop control for Isolated Boost dc dc Converter with the reduced number of Switches

Fig. 2. Demonstrates the closed loop PID controller structure for the circuit and exceptionally contains voltage and the current detecting element feedback. The criticism sign got from the Vdc is then contrasted and therefore the V_{ref}. Subsequently, the acquired error between the V_{ref} and the response gesture is connected to the PID regulator to compensate for the available error. The well-ordered indicator is given by the PID checker defines k for pwm generator. Then the accomplished k is contrasted and the higher-frequency gradient-signal to give pulses to the Sw1 and Sw2. The controller parameters are fine-tuned to get the set Vdc under different resistive conditions.

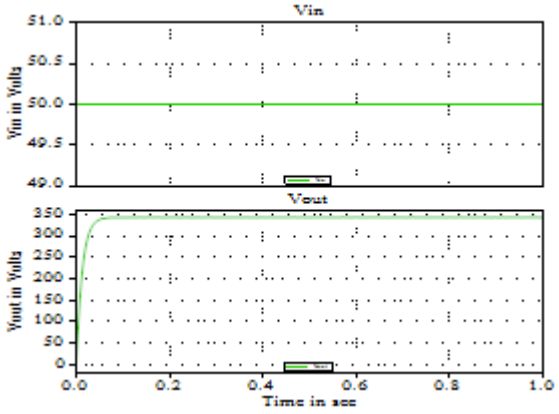

Fig. 3 Input voltage and an Output voltage of the Quasi-Resonant at closed Loop V_{in}=50 Vand V_{out}=343 V

III. SIMULATION AND EXPERIMENTAL RESULTS

The hardware paradigm is executed with comprehensive controller calculation inscribed in the examination are done on resistive stack variants to choose the exhibition of the Enhanced boost DC DC converter with the two switches. A numerical recreation with test verification outcomes furnished throughout this paper coordinates intimately with the analytical predictions.

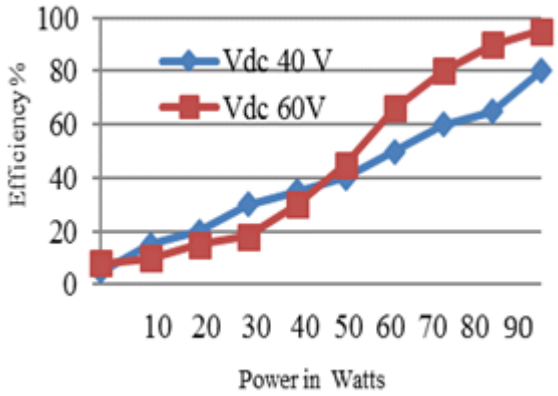

Fig. 4 Measured efficiency vs. output power of the Quasi-Resonant at Closed Loop

IV. CONCLUSIONS

Experimental execution of hardware model Isolated Boost DC-to-DC converter dependent on the controller is portrayed. The DC DC power converter with a diminished quantity of switches circuit coordinated with the voltage doubler rectifier delivers a great enactment V_o equated to the prevailing improvement DC DC converter with three switches. This strategy significantly beats the parasitic impacts and lessened swell at the V_o and I_o. A shut controller with V/I sensing element feedback, the calculation is produced to keep up the output voltage prerequisites under resistive loading conditions. Simulation results gave during this manuscript is as per the investigational outcomes that measures are verified by the theoretical expectations. Henceforth, the DC-to-DC converter is suitable for fuel applications.

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