

Digital Controller based Multi motor drive using SPWM

S.Rajasekaran, R.Anand, P.Muthukumar

Abstract: Controlling the speed of an induction motor through stator side is vital in industries. Multi motor speed control (MMD) is one of the inevitable needs in electrical companies like mills, crane etc. Individual converter is triggered by Field Programmable Gate Array (FPGA) with single digital controller is used to control the multi motor in this work. Due to this controller price and manual work have been reduced. Now a days, many controllers in need of digital execution. Electrical machines requires Sinusoidal Pulse Width Modulated (SPWM) converters for vary the speed. The generation of SPWM is done by using FPGA in this work.

Keywords: Multi motor drive, FPGA, SPWM.

I. INTRODUCTION

Automation is a vital issue of the factories in the earlier decades. This is very much needed in multi three phase induction motor drives [1]. When the input pulses are varied then the output voltage is also varied [2]. By producing the controlling input voltage of the motors using perfect pulses to the converter is the main task of the multi motor drive [3]. Xilinx software is used to produce the pulses using FPGA to attain the more precise control [4]. By the usage of the controller, the manual work and maintenance are trimmed down. SPWM inverters are producing harmonic less voltage at output which is used as a input of AC motor [5]. Set of pulses are developed by sinusoidal pulse width modulation. This paper deals with the reduction of Total Harmonic Distortion (THD) using proposed controller, further FPGA and its utilization also discussed.

II. SPWM TECHNIQUE

To produce the pulse width modulated pulses, three phase sine wave taken as the reference wave and triangular wave which has a higher frequency as carrier wave. The frequency of the triangular wave is higher than the reference wave. Pulse which is given to the switch is induced by comparing the reference signal and carrier signal. This comparison is done by comparator. For the multi motor drive set of pulses are developed using above mentioned technique.

By using the amplitude of reference and triangular wave the pulse is produced. These pulses are the reason to create output voltage of the inverter. The pulse width is varied by varying the voltage value of reference wave.

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$$\text{Modulation index } (M_i) = V_{\text{Ref}} / V_{\text{Car}} \quad (1)$$

Where,

V_{Ref} is the reference voltage

V_{Car} is the carrier voltage

Equation 1 gives the M_i using voltages.

$$M_f = f_{\text{sw}} / f_1 \quad (2)$$

Where,

f_{sw} is the switching frequency

f_1 is the fundamental frequency

Equation (2) gives the relation between f_{sw} and f_1 in the calculation of M_f .

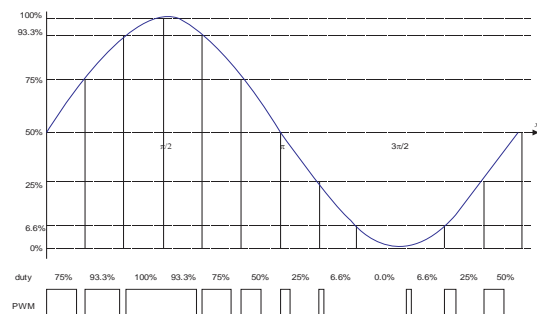


Fig. 1 Sine PWM sample points

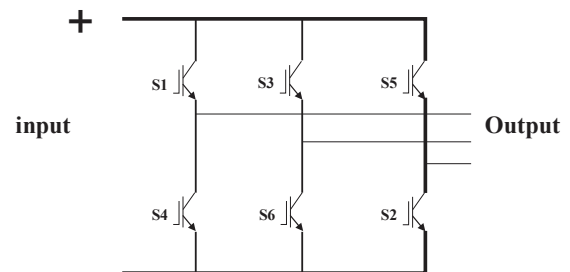


Fig. 2 Voltage Source Inverter

Up Down counters are used to produce the triangle signal counter in the frequency value of 10 KHz.

$$\text{Time } (t) = 1/\text{frequency } (f)$$

$$\frac{1}{10000} = 100000 \text{ ns} \quad (3)$$

The time period of switching pulse is given in the Equation 3.

A. Sine PWM Generation

Look up table is used to create the sinusoidal wave 256 positions are used to stock up the 360 degrees of sinusoidal wave every 8 bits of size in addition to sign bit $\sin 0=0$.

When angle is 90 degree, 8 bits are used and value is 255.

When angle is 270 degree, 8 bits are used and value is -255.



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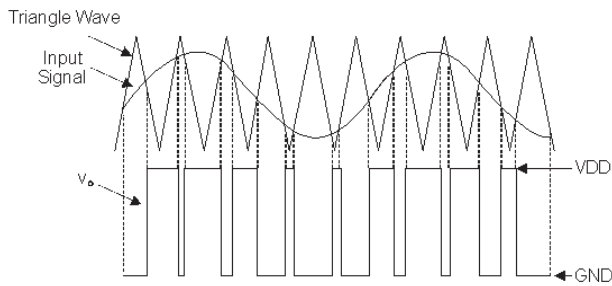


Fig. 3 SinPWM Pulse Production

Xilinx 12.1 is used in this work. The VHDL coding is generated in the above mentioned software. The integration capability of leading system is the special thing which is in Spartan-6. Spartan-6 XC6SLX25 has less price and larger volume requests. The equipment size is 17 x 17mm also it has 186 input output pins.

III. SPEED REGULATION OF MMD USING FPGA BY SPWM GENERATION

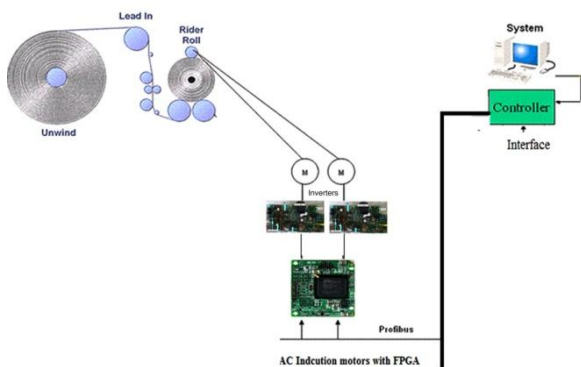


Fig. 4 Unit of paper rolling

If the speed of the one motor is varied then the sensor will act. It senses and gives the signal to FPGA. FPGA will produce the SPWM pulses for correcting and equating the motor speed to the other motors.

A. Port declaration

In the FPGA , pins P1 to p6 supplies pulses to Inverter 1. In case of changes required to resetting the data can be done in 8th pin. Like that way Inverter 2 receive PWM outputs of P1 to P4 pulses from the IC pin number 9 to 12 and supplies PWM out puts to unit 2 .The remaining two PWM outputs P5 and P6 for inverter 2 are supplied by pin numbers 28 and 29 pins respectively. To sense the signals for the feedback to precise controlling speed is done by the pins. The CAP pin 16 to is used catch the feedback signals for the perfect precise controlled output [6].

B. SPWM generation

As per the sine PWM concept, the sine PWM is generated by comparing three phase wave with triangular wave for each unit. The generated pulses are given to the inverter switches for the inverter 1 and 2 in each section simultaneously. The multi motors are getting controlled output voltage from the inverters. To get precise output speed feedback system helps through proximity sensor [7].

C. HardWare

The implemented system hardware setup with FPGA is shown in Figure 3.2. DC 600V is converted with the help of Voltage source power inverter and digital controller. The power device used in the converters is IGBT. The respective inverters take care of supplying corresponding controlled voltage /frequency supply to the two three phase AC supply for the two- three phase induction motors as declared by the key in the FPGA.



Fig. 5 Hard Ware Set Up

One set of developed SPWM signals from the digital controller is used to control inverter one's six IGBTs. The next set of pulse are developed similar manner for the inverter 2. The phase voltage is launched by SPWM signals. At any instant of time, a set of three switches will be ON state, either one upper and two lower switches, or two upper and one lower switch. A dead time is created between switching off the upper and lower switches.



Fig. 6 Two Different speeds

D. Multi Motor Drive Control

Multi motor speed control is achieved by the inverter circuits having variable SPWM pulses. SPWM pulses are developed with set of VHDL coding for each units and fused on it [8]. By selecting the proper key in the digital controller the particular inverter and induction motor unit is selected. This key acts as the interfacing device for the FPGA.

By pressing the keys in the controller gives various SPWM pulses for the inverters[12]. ie ,by adjusting the key position the pulses are varied because of its simple digital interface [9], [10]. SPWM signals for various speeds of two induction motors are detailed in Figure 3.4. The inputs 1 010110 is dedicated for unit 1 and 010101 for inverter 2. The speed varies as 1396 rpm and 740 rpm as per the controlled signals is shown in Figure 3.3.[11].

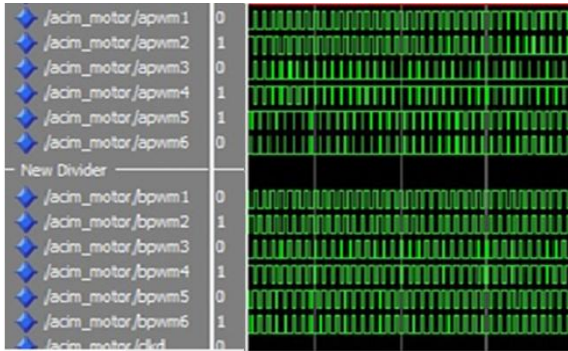


Fig. 7 Twelve SPWM Pulses

In the Figure 3.4, the upper pulses are dedicated for high speed motor and lower pulses are for low speed motor. According to these pulse the V/f signals will vary.

The developed sine waves in the digital controller of FPGA are shown in Figure 3.5. In the two wave forms, the first wave form is for the speed of 1400 and the corresponding frequency obtained is 50 Hz.

Similarly, the second wave is for next induction motor which rotates the speed of 740 rpm with the frequency of 28Hz.

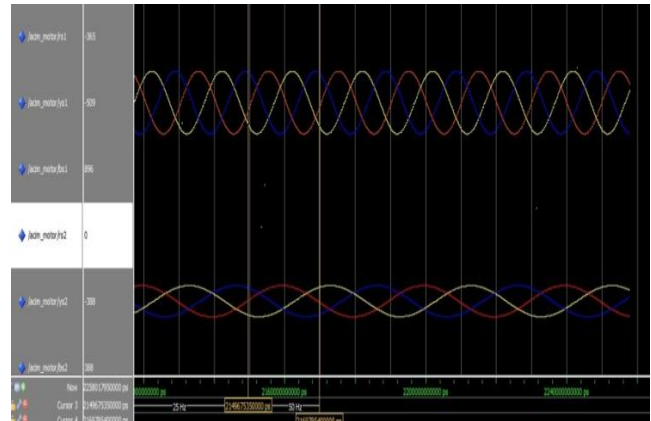


Fig. 8 Sine Waves for Multi motor control

Inverters 1 and 2 supplies controlled V/f to Induction motor 1 and 2 respectively from the corresponding controller pins signals from a single FPGA-Spartan -6. VTHD and ITHD values from the multi motor drive is listed in the Table I. Power switches creates Harmonics Distortion content in voltage and current are detailed in the table. From the results, it is found that the harmonics ranges for both the machines become nearly same for SPWM based speed control of MMD [13].

SI NO	IM 1			IM 2				
	THD %	Inverter Efficiency % at no load		THD %	Inverter Efficiency % at no load			
	V _{THD}	I _{THD}		V _{THD}	I _{THD}			
1.	4.9	5.1	12	87	4.9	5.1	12	87

IV. RESULTS

The complete analysis is taken from results of SPWM based speed control drives for MMD gives the voltage per frequency ratio is nearly same in particular speed [13]. It is found that, using a single FPGA for controlling more number of units gives effective usage of FPGA and minimizing human requirement and reducing processing time.

V. CONCLUSION

In this work, speed controls of Multi motor drives are investigated for SPWM technique. FPGA Digital controller is helped to develop SPWM pulses for two set of inverters. Investigation has given the effect of FPGA in parallelism for multi drives. Reliability of FPGA is identified for speed control techniques. Further, investigations are noted for higher DC bus voltage utilization and device usages. The results by the SPWM technique are conferred for various conditions. From all the analysis it is found that, VTHD and ITHD in SPWM technique is less. This investigation gives consideration on SPWM technique in multi motor drive using digital controller.

REFERENCES

1. S.Rajasekaran, V.Gopalakrishnan, 2016‘A FPGA Based Multi Motor variable Speed drive’ Asian Journal of Information Technology, vol. 15, no. 13, pp. 2186-2190
2. R Anand, P Melbamary, “Firefly Optimization Algorithm Tuned Fuzzy Sliding Mode Controller based Phase Shift Series Resonant DC to DC Converter” Asian Journal of Research in Social Sciences and Humanities 6 (8), 2016, pp.764-778
3. S.Rajasekaran ,Dr.V.Gopalakrishnan 2015‘Multi Motor Speed control using FPGA’ International Journal of Applied Engineering Research,ISSN :0973-4562,vol.10, no. 64,pp. 149-156.
4. S.Rajasekaran, V.Gopalakrishnan, Amal Dev V.R, “FPGA Implementation of a PWM for a three phase multimotor drive”, International Journal of Applied Engineering Research, pp.7-12, Vol. 10(64), 2015.
5. S.Rajasekaran, V.Gopalakrishnan, Sarath.C “FPGA Implementation of Flux and Torque Controller for A Three Phase Induction Motor” International Journal of Applied Engineering Research, pp167-173, Vol. 10(64), 2015.



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6. Das, B, Fancon, M, Kasari, PR &Chakrabarti, A 2015, 'Comparison of different PWM-VSI fed 3 phase IM based on modulation index and switching frequency', International Conference on Electrical, Electronics, Signals, Communication and Optimization, EESCO 2015.
7. Chen, B, Yao, W, Lu, Z & Lee, K 2014, 'A novel stator flux oriented V/f control method in sensorless induction motor drives for accuracy improvement and oscillation suppression', 2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014, pp. 5092-5099.
8. Lakka, M, Koutroulis, E &Dollas, A 2014, 'Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters', IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 356-365.
9. Boudjit, K &Larbes, C, 'A New Approach for Synchronisation Multiple Motors using DSP',International Conference on Systems, Signal Processing and Electronics Engineering (ICSSEE'2012) pp. 216-220.
10. De Castro, R, Araújo, RE & Oliveira, H 2009, 'Control in multi-motor electric vehicle with a FPGA platform', Proceedings - 2009 IEEE International Symposium on Industrial Embedded Systems, SIES 2009, pp. 219-227.
11. Iyer, J, Tabarraee, K, Chiniforoosh, S &Jatskevich, J 2011 'An improved V/F control scheme for symmetric load sharing of multi-machine induction motor drives', in pp. 1487-1490.
12. Jeftenic, B, Bebic, M &Statkic, S 2006, 'Controlled multi-motor drives', in International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM, pp. 1392-1398.
13. Ricci, F & Le-Huy, H 2002, 'An FPGA-based rapid prototyping platform for variable-speed drives', IECON Proceedings (Industrial Electronics Conference), vol. 2, pp. 1156-1161.