256K Memory Bank Design with 9T SRAM Bit Cell and 22nm CNTFET Optimizing for Low Power and Area

Y. Maheswar, B.L. Raju, K. Soundara Rajan

Abstract: In this paper, 9T bit cell is designed along with its periphery circuits to enhance the operating speed of 256 Kb memories. 9T SRAM bit cell is designed with 22nm FINFET technology to obtain optimum bit cell transistor geometry. For variations in transistor geometries, VDD and temperature, the leakage current for the designed bit cell is estimated. The peripheral circuitry transistor geometries are designed for applications with low power and high speed. 9T bit cell integrated with its periphery is designed to form 256 Kb memory with two 128 Kb memory banks.

Key words: Sub threshold SRAM, current sense amplifier, high speed, cross coupled inverter, 9T bit cell, CNTFET

I. INTRODUCTION

At Nano scale CNTFETs are promising for additional CMOS devices. The Carbon Nano tube Field Effect Transistor (CNTFET) is one of the most promising devices to surpass the MOSFET technology due to its limiting sizes towards the end of the technology roadmap of CMOS devices [1]. The Carbon Nano Tube Field Effect Transistor (CNTFET) has been continued as one of the substitutions to remove the conventional MOSFET because of its superior execution qualities and better properties of it. CNTFET based SRAM cells have been designed and compared with MOS based circuits [2][3]. 6T and 8T cells have been designed with low power consumption and noise margin. Novel six-transistor (6T) static random access memory (SRAM) bitcell design using CNTFETs with superior noise margin, while consuming low dynamic power and write ability margin under various PVT conditions [4]. SRAM cells are compared with CNTFET cells in terms of area, power and speed. 6T SRAM cell compared with 8T SRAM cell, 8T cell is designed to consume power less with wider noise margin. CNTFET cell is found to be faster than MOS based cell with 6 times faster, 10 times less power consumption [5-7]. Most of the literature reports SRAM cell design, it is required to evaluate the memory architecture that consists of multiple memory cells with the periphery. In [8] novel architecture has been presented with array logic that can reduce soft error with increase in area overhead.

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Differential 10T bit cell was presented in [9] with bit interleaving schemes between vertical and horizontal lines that could improve read stability. In [9], a novel scheme with supply voltage variation among basic nodes along the column was designed for 9T bit cell. In [10] novel architecture for 9T bitcell that completely isolates the data from the bitline during a read operation is presented. The 9T Cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption by 22.9% as compared to the 6T Cells. The leakage power reduction and read stability enhancement provided with the new circuit technique are also verified under process parameter variations. In [11] authors have designed bit cell which includes the transmission gate to implement column select and row select (WL) cell storage access. In order to prevent half-select mode operation this structure is used. One problem with this approach is that a floating inverter output (wle) when both CS and WL are both "0". The floating node causes the pass-gates to leak during the time the cell is not selected. This will interfere with selected cell sensing signal. Power consumption of SRAM account for a significant portion of the overall chip power consumption and due to high density, low power operation is a feature that has become a necessity in today’s microprocessors. This design is mainly for the ultra-low power. In [12] a new SRAM Cell that is amenable to small feature sizes such as encountered in the deep sub-micron/nano CMOS range is proposed. The write/read delay increases significantly when the power supply voltage drops below 0.6V, about three times larger than the previous power supply voltage level. Therefore, performance of SRAM array will drop if SRAM array operated at ultra-low power. In [13] cross coupled inverter pair that forms the bit cell is inserted with a pass transistor, with additional word lines for bit interleaving in 9T bit cell. In [14] energy efficient SRAM cell with bitline leakage reduction in 9T bit cell is presented. The design achieves low power with minimizing leakage, the maximum operating frequency is 80MHz at 0.8 V power supply and requires additional hardware. In SRAM circuits, more than 40% of the total active mode energy is consumed due to leakage currents. SRAM arrays are important sources of leakage since majority of transistors are utilized for on-chip memory in today’s high performance microprocessors and systems-on-chips (SoCs). The SRAM cell stability is further degraded due to process variations in deeply scaled CMOS technologies.

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In this work 9T SRAM cell is designed enhancing the data stability and reducing leakage power, thus contributing overall reduction in power consumption. Memory bank of 256Kb is designed with two 128 Kb bank memory designed using proposed 9T SRAM cell with its periphery circuitry reducing transistor counts. In this work, 9T SRAM cell is designed along with periphery circuitry. The memory bank architecture that can store 256K bits designed is modeled and evaluated using NanoCYm (open source simulator developed by Sanarys Technologies).

II. 9T SRAM BIT CELL

The architecture of SRAM 1bit is shown in Figure 1. It consists of precharge circuit, enable circuit, sense amplifier and he basic circuit called 6T SRAM cell. During write operation the write enable signal should be high, and the word enable signal should be low. And in the read operation, the word line should be high. At a time only one operation can be performed that is write or read. The schematic of the 9T SRAM cell [10], with transistors sized for a 65-nm CMOS technology, is shown in Figure 2. The 6T memory cell is minimum sized devices (composed of N1, N2, N3, N4, P1, and P2 with $W=W_{min}$ and $L=L_{min}$). Write signal (WR) controls the write access transistors (N3 and N4). Additional two transistors (N5 and N6) are for bit-line access and transistor N7 is for read access. The data stored in the memory cell controls the two bit line access transistors. Additional read signal (RD) is introduced to control the transistor N7. To write '0' into the bit cell at Node1, WR signal is set to '1' turning on N3 and N4. RD is set to '0' switching off N7. The bitlines BL and BLB are set to '0' and '1' respectively. Thus a '0' is forced into the SRAM cell through transistor N3. For writing '0' at Node2, BL and BLB are set to '1' and '0' respectively. If Node1 is storing '0', during read operation N3, N4 and N5 are cutoff, N6 is on. During read RD is set '1', turning on N7, thus isolating N3, N4 and N5 from BL and BLB, with N6 on driving BLB. The node voltage at Node1 is maintained at '0' thus improving read stability of the SRAM cell. As the bit cell storing '0' and '1' are isolated from BL and BLB during read '0' and read '1' operation, data stability of the 9T cell is increased during read operation. Leakage power is also reduced in 9T SRAM, as the transistors need to be designed with minimum width [10]. It is reported in [10] that the leakage power is 7.7% low compared with 6T SRAM cell. In order to further reduce the leakage power super cut off scheme is presented in [15], in this approach negative gate to source voltage (Vgs) is applied to nMOS transistor to minimize subthreshold leakage current, however with negative Vgs tunneling current increases due to high gate-oxide voltage.

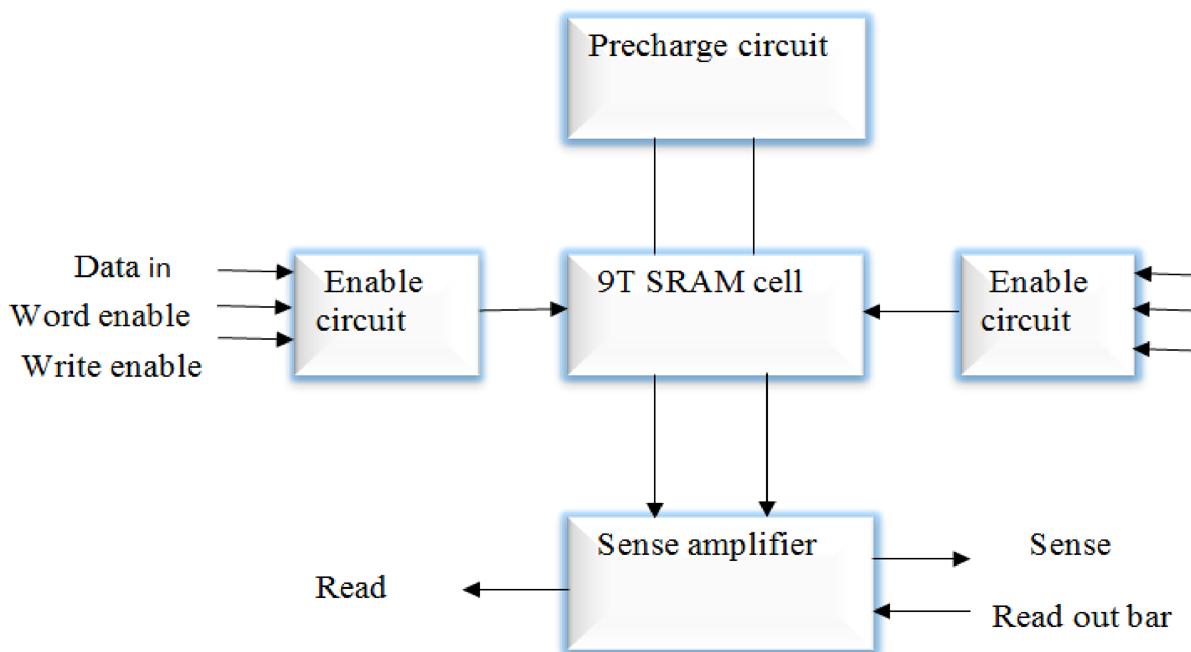

Fig. 1 Memory Cell architecture

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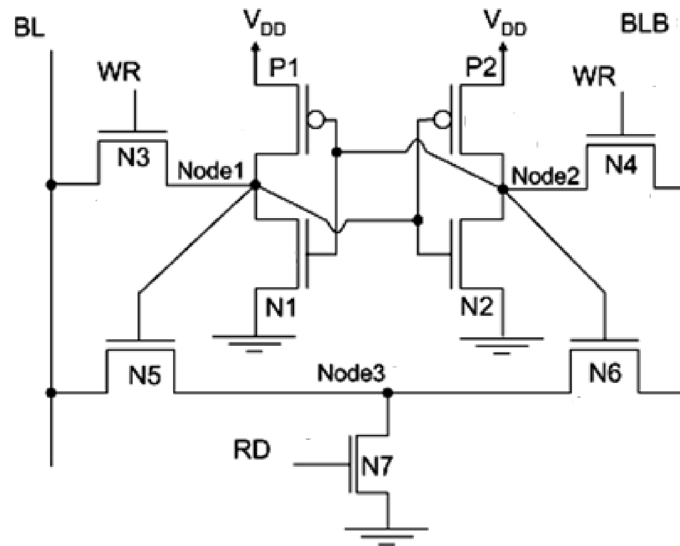

Fig. 2 9T SRAM cell in the active mode

During standby mode the leakage current in 9T SRAM cell is due to gate oxide leakage and sub threshold leakage. Figure 3 shows the current leakage in the standby mode of the 9 T SRAM cell. Gate oxide leakage is constituted by the transistors N3, N4 and N7; subthreshold leakage is constituted by the transistors N1, P2 N5, N6 and N7. In [10], it has been discussed that the leakage current varies with VRD and VWR. With VRD equal to VWR set to -50mV, the leakage power is 31.9nW. It is recommended that WR and RD signal voltages are set to lower than zero volts to reduce leakage current. It is recommended to maintain 0.9VDD in standby mode for additional Node3 voltage to minimize leakage current. It is also recommended to resize the transistor geometries in the cross coupled inverters to minimize leakage current, achieve read stability, write stability and there by achieving enhanced SNM.

III. DESIGN OF 256KB 9T SRAM

In this work, 256Kb SRAM block is designed along with the periphery circuitry. The design is requires 2.36 million transistors in the core SRAM. The periphery logic is designed symmetrically to reduce memory area by eliminating column multiplexer and row decoders that increases the overall delay as well as transistor count. The proposed memory is designed using column decoder and switch logic instead of using column multiplexers. As the number of rows in the core is 1024, a novel technique is adopted for the design of the **10:1024 Row Decoder** which has immensely helped in reducing the transistor count. Traditional decoder challenges are that it requires a very large number of transistors. Long delays are added to the capacitance associated with long wires runs and high gate input count. In order to drive this huge capacitance load, the address inputs must also be buffered. The layout becomes more time-consuming and unnecessarily complex. Another problem is that such a decoder's power consumption will be very high due to the large number of gates, so the hierarchical technique is adopted to reduce the overall power consumption. The same has been described later with details of the row decoder block.The Split core architecture is selected according to which the complete core is divided into two parts each with the array of 1024x128, i.e. the column lines are divided into equal half's of 128 columns on each side. The 10:1024 row decoder is designed in the hierarchical way using the bus architecture which had reduced the complexity in connecting the 1024 wordlines to the core. Figure 3 presents the complete 256Kb SRAM Memory architecture.The Control Block comprises of 2:4 decoder and 3:8 decoder along with some driving buffers. All the write/read enable signals, clock signal, precharge enable and sense amplifier enable signals are buffered by this block. The IO block comprises of two switch boxes in which the selection of <7:0> BL and <7:0> BLB signals is controlled by the column decoder output. Other than this IO consists of sense amplifier, precharge and write logic. The sense amplifier circuit designed in this work replaces the traditional voltage sensing to current sensing. One of the drawbacks of current sense amplifier is the power dissipation as all the four transistors operate in saturation. To reduce power dissipation, transistors M5 and M6 are introduced that are drain biased thus restricting transistors M3 and M4 in linear region. The insertion of transistors M5 and M6 reduces power dissipation by 12% as obtained from the SPICE simulation results. The control unit allows either the data to be written into the memory cell or the data from the bitlines to be transferred to the sense amplifier. The control block is designed to optimize the use of the area. It consists of 2:4 decoder, 3:8 decoder and the buffers to drive the signals to the memory and IO Block. The read/write control signals, precharge, sense amplifier signals are fed to the buffers (chain of inverters) in order to drive the signals to the other circuitry. As discussed in architectural specifications there are in total 13 address lines, out of which three are for the 3:8 column decoder and remaining 10 for the row decoder. The address bus ADD<12:5> is fed to the circuitry named row main. Row main the cascade of four 2:4 decoder in series thus giving 16 outputs named as K, L, M and N. These all signals are the bus <3:0> of 4 bits.

The other two address buses ADD<4> and ADD<3> are sent to the buffers to drive the inputs of the 10:1024 row decoder. The rest three ADD<2:0> are fed to the 3:8 decoder. The clock, read and write along with the ADD<12:0> are inputs to the control block. The read/write control signals and clock after being fed to the buffers are connected to the row decoder. The 256 Kb memories is divided into two groups each with the memory size of 128Kb. The 10:1024 row decoder is in centre of the two core blocks. The IO blocks are at the bottom of the core at each side and the control block is at the middle below the row decoder.

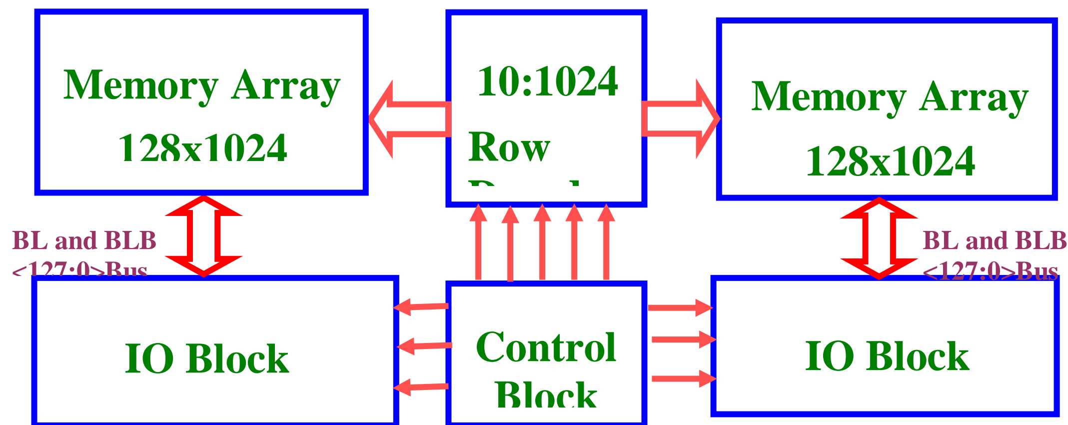

Fig. 3 256 Kb 9T SRAM

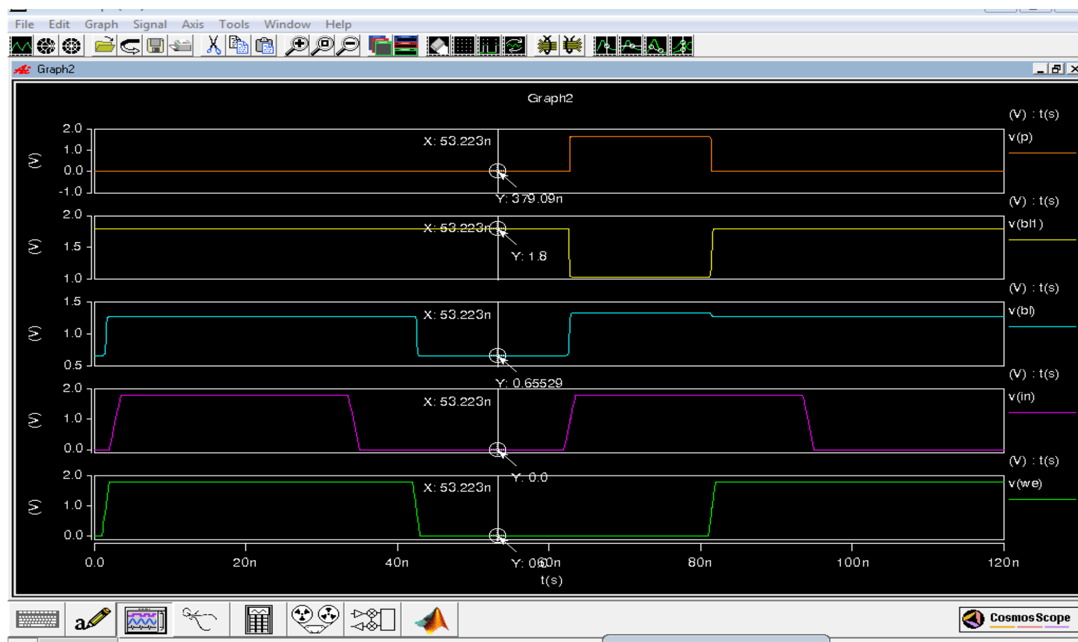

Fig. 4 SRAM cell results

Table. 1 Results of SRAM cell and periphery circuits

	Frequency	Power	Area
SRAM 9T cell	50 MHz	0.01203mW	12 sq. units
Decoder	25MHz	0.014499mW	56 sq. units
SRAM 1bit	16.353MHz	4.9594mW	50 sq. units
SRAM 1*8 bit	16.667MHz	28.963mW	50 sq. units
SRAM 4bit	16.3MHz	4.343mW	200 sq. units

Table. 2 Comparison with MOSFET memory

Time domain	Parameter	MOSFET	CNTFET
Fall time Rise time	Inverter	20.381ps 30.022ps	33.26ps 71.676ps
Fall time Rise time	Decoder	161.18ps 138.66ps	759.28ps 143.07ps
Fall time Rise time	SRAM 1-bit	50.12ps 25.187ps	72.25ps 17.021ps
Fall time Rise time	SRAM 4-bit	57.376ps 40.265ns	70.25ps 80.25ps

IV. RESULTS AND DISCUSSION

The 9T SRAM cell designed is modeled using SPICE and simulated using NanoCYm. Figure 4 display the SRAM cell simulation results shown in Figure 1. The rise and fall time of 17.021ps and Fall time is 72.258ps, operating a frequency of 50MHz with power consumption less than 12micro W. The signal-to-noise margin (SNM) of SRAM 9T cell is 2.6875E-01 and the circuit took 4.09 seconds to complete the simulation. Table 1 summarizes the results of SRAM design. Table 2 summarizes the results of 4 x 4 memory cell. The waveforms obtained when writing a '1' and '0' into the memory cell are shown in Figure 5. As seen when data '1' is written, the Q node begins to rise to Vdd when the Q nod starts dropping down to Gnd when the write signal is asserted and the word line is pulled high. The write access time is the time between a write request and the final writing into the memory of the input data. The primary reason why the write cycle is greater than the write access time is because once the write signal is de-asserted the bitlines have to be pulled back to Vdd by the bitline load circuits. The bitlines have large capacitances and this adds to the delay.

The data present in the memory array must be read out by the circuits of the sense amplifier that the replica bitline circuit must enable. There are chances that the data will be destroyed during the reading operation. Figure 6 shows pre layout simulation results of single bank single bit read operation. Power dissipation of various process corners of pre-layout 256Kb SRAM is shown in Table 3. SNSP (slow NMOS slow PMOS), TNTP (Typical NMOS Typical PMOS) and FNFP (Fast NMOS Fast PMOS) process corners are shown in Table 3. Simulated each block of the 256Kb9 T SRAM and obtained the desired results. The designs of 4x8 array was simulated in order to check the working of control block, IO and row decoder when combined with the memory array. Finally the delay, power and area was estimated for the entire memory by calculating the same for individual block using specific tools and the pre-layout and the estimated post- layout parameters. Based on these calculated values for the array the pre –layout and the post- layout values for the entire 256Kb SRAM memory is evaluated and compared with reference design is shown in Table 4.

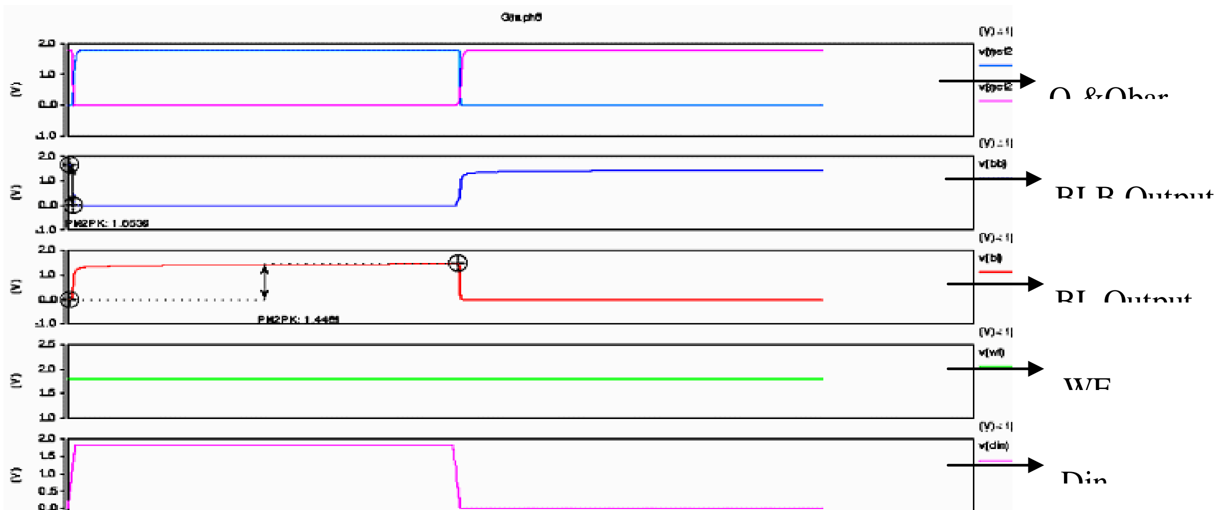

Fig. 5 Pre-layout Simulation of 8Kb SRAM Write Operation

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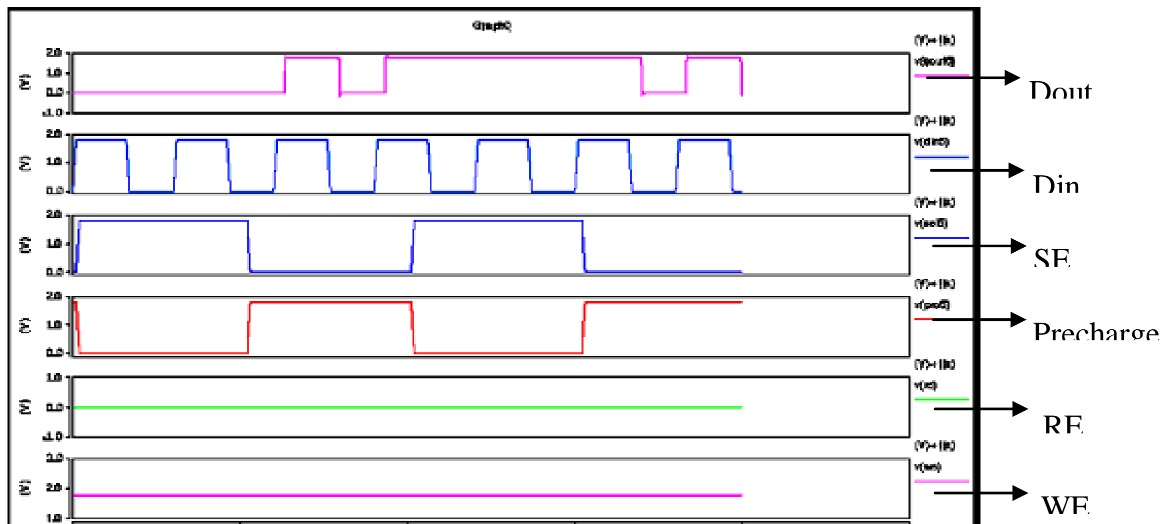

Fig. 6 Pre-layout Simulation of Single Bank Single Bit Read Operation

Table. 3 Power dissipation in process corners

Process corner	Power dissipation, nW
SNSP	21.167
TNTP	30.673
FNFP	42.728

Table. 4 Comparison of memory bank designs

	[15]	[16]	[13]	Present work
Memory size	256kb	64kb	1kb	256kb
Operating Voltage	0.35V	0.23V	0.3V	0.6V
Frequency	25kHz	100kHz	909kHz	3.3 GHz
Active power	3.39 μW	0.989 μW	3.51 μW	41.72mW
Leakage power	-	-	-	22.9nW
Power/frequency	135.6 $\mu W / MHz$	9.89 $\mu W / MHz$	3.86 $\mu W / MHz$	0.01303 $\mu W / MHz$

In the above Table 4 the area for individual blocks was calculated by calculating the width and height of each block individually. The total chip area was calculated in same manner. For power firstly the power dissipation for individual memcell was calculated in spectre than was summed, similarly was calculated for all individual sub-blocks during standby mode and added together to get the overall. All the blocks were simulated for the temperature variations from -40°C to 125°C. The leakage power for the 9T SRAM Cell is found to be 22.926 nW at an operating frequency of 3.33 GHz. The switching power during read is 41.728mW and during write is 20.674mW. The total transistor count for the complete 256 Kb 9T SRAM Memory is 2.4 million, in which the 23,59296 transistors comprises only of the memory array and the remaining 15166 transistors are used for the periphery circuitry. The 10:1024 Row Decoder is designed in the hierarchical manner in order to utilize the minimum area.

V. CONCLUSION

In this work a 9T-based SRAM, which addresses the critical issues in designing a low power static RAM in deep submicron technologies along with the design techniques used to overcome them is presented. The architecture consists of SRAM cell, sense amplifier, write driver, control unitprecharge, IO block and row decoder as the building blocks. Working operation of all basic blocks is explained clearly.Using Hierarchical technique for the row decoder has drastically reduced the transistor count as well as the overall area of the chip. Implementation of the 9T SRAM Cell has reduced the power consumption by half as compared to the conventional 6T.

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