CMOS Low Voltage LNA with Improved Noise Figure

Najeemulla Baig, Fazal Noorbasha

Abstract : ***In this research paper the designing of 1.5754GHz low Noise Amplifier integrated with a 90nm CMOS process using RF-spectre is presented. The intended circuit exhibits power gain of 19.82dB; S_{12} of -31.10dB, noise figure of 0.462mdB, 1-dB compression point of -14.57mdB and IIP3 equal to -12.557mdB at low power supply of 0.7 V.***

Keywords- Low Noise Amplifier (LNA), Global positioning system (GPS), Impedance matching, Noise figure (NF), 3rd order input intercept point (IIP_3) Gain.

I. INTRODUCTION

The available GPS receivers compel to design better performing, lesser cost receivers. The L_1 frequency of GPS signal is 1575.42 MHz. LNA is the key part of the GPS receiver. The important role of LNA is to give adequate power gain to trounce the noise of successive stages [1].
An LNA circuit using resistive feedback and gain peaking technique is used in [11] but results in high NF. In this research work, a low voltage CMOS RLC tuned LNA is planned.
This paper is prepared as follows: In Section2, a tuned *RLC* CMOS LNA circuit design is planned. Section3 shows the simulation results. Section4 describes the s-parameter study of the LNA design .lastly; some conclusions are given in Section5.

2. Design of the planned LNA circuit

The designed circuit is shown in Figure1. The inductors L_1 and L_2 are selected to give the chosen input resistance (Rs). L_3, R_1, and C_1 form a resonant circuit to refrain the LNA to 1575.4MHz.

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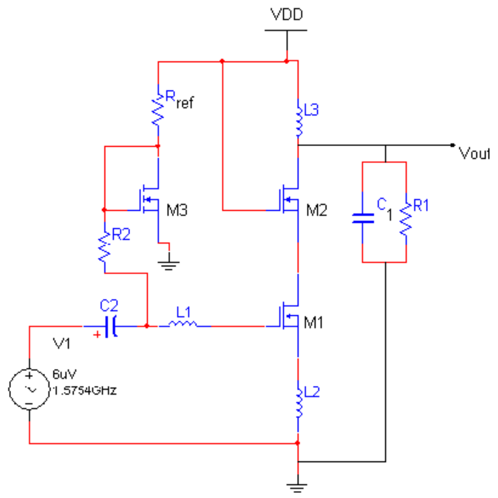

Fig.1.The circuit of CS LNA [12]

A current mirror is formed with M_1 using transistor M_3. The width of M_3 is little part of the width of M_1. This will decrease the extra power consumption by the bias circuit.

Resistor R_{ref}, selected to provide low NF and small power dissipation in combination with the V_{gs} of M_3. Equivalent noise current of R_2 is negligible if larger value is selected for R_2.

2.1. Calculating circuit components values

Step 1: Designing $L_2(L_s)$ by real part toning condition, presume that Rs =50 Ω
Input matching state gives

$$R_s = \frac{g_m}{C_{gs}} L_2 = \omega_T L_2 = 2\Pi f_T L_2 \qquad (1)$$

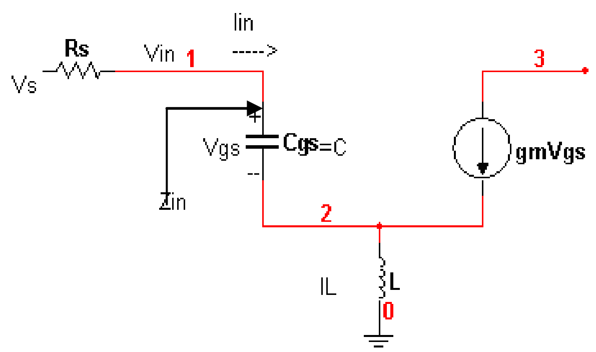

Fig.2. Small signal equivalent circuit of LNA [1]

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For a MOS transistor f_T is called as unity gain frequency there fore

$$2\Pi f_T = \frac{g_m}{C}$$

Therefore, $$L_2 = \frac{50\Omega}{2\Pi f_T} \qquad (2)$$

For 90nm technology, $f_T = 25\text{GHz}$ then inductor L_2 is 0.159 nH , taking into consideration a little higher value for L_2 than deliberate value in simulation, as the noise penalty of undue L_2 is a lot less severe than for deficient L_2 [5].

Step2: design $L_1(L_g)$ using NF condition

According to specification NF< 2dB, from the NF equation [4]

$$NF = 1 + \frac{2}{3}\frac{1}{1+\frac{L_1}{L_2}} < 2$$ Solving yields

$$\frac{L_1}{L_2} > \frac{1}{3} \Rightarrow L_1 > \frac{L_2}{3}$$

Let L_1=1nH.

Step3: Designing C=C_{gs} using imaginary part toning condition $$\omega_c(L_1 + L_2) = \frac{1}{\omega_c C}$$

$$C = \frac{1}{\omega^2{}_c(L_1 + L_2)} \qquad (4)$$

With $\omega_c = 2\Pi(1.5754)10^9\ rad/s$ and using L_1 and L_2 values the value of C is 7456.68fF we have that [4]

$$C = C_{gs} = \frac{2}{3}WLC_{ox} \qquad (5)$$

$$Cox = (\varepsilon ox / tox) = 13.466 \times 10^{-3}$$

From equation (5)

$$W_1 = \frac{C}{\frac{2}{3}C_{ox}L_1}$$

For ease consider $\left(W/L\right)_1 = \left(W/L\right)_2$

Here we got the M1 transistor width; for selecting M2 width following cases we can observe. When W_1=W_2 LNA gives superior NF when compared to the NF resulting by taking $\left(W/L\right)_1 = 2\left(W/L\right)_2$, but this gives better gain. If we take $\left(W/L\right)_1 = \frac{1}{2}\left(W/L\right)_2$ noise figure and gain both degrades.

Step 4: Finding L_3, C_1, R_1 by using parallel toned circuit equations

This is given by: $\omega_0 = \frac{1}{\sqrt{LC}}$

where $\omega_0 = 2\pi f_0$

Assuming L_3 and finding C_1 for optimum results.

L_3=10.2nH, C_1=46.2fF and using R$= 2\Pi\sqrt{\frac{L}{C}}$ to get R_1=4.6Kohms (after optimizing for gain).

3. Results and discussions

The planned LNA is simulated using the RF-spectre simulator. For a range of L_g and Ls values S-parameters and NF analysis is perfomed, at the designed frequency.

To bias transistor M_1 current mirror circuit is used, with different widths (W_3) for current mirror transistor M3. S-parameters, NF, VG and power dissipation (PD) variations with different widths for transistor M_3 are shown in the table no.2. A better NF results without current mirror circuit but the additional supply is essential for biasing M1.

3.1. Noise Figure (NF)

In figure 3 NF variations with respect to frequency are shown. Initial simulating noise figure (NF) Vs frequency gives a NF of 633.8mdB at 1.5754GHz shown in Figure.3.

L_g Vs NF gives the subsequent results, at L_g=10.3nH which is higher than the planned value (L_g=7nH) NF=461.85mdB, an additional increase in L_g results in improved NF but the setback is the area in use by the inductor is very large this is shown in figure 4.

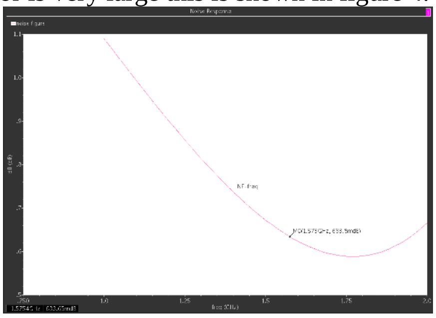

Fig.3. NF Vs frequency

Also, L_s Vs NF analysis results that Ls decreased NF better, Ls less than 160pH; NF is almost constant at 628mdB.

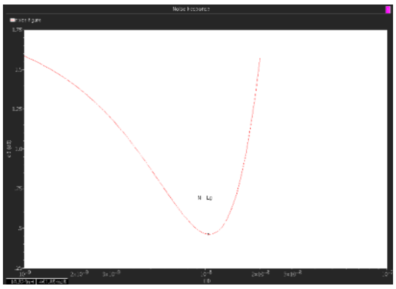

Fig.4. NF Vs Lg

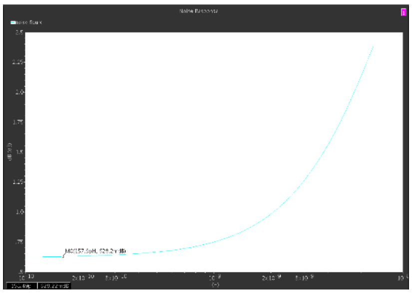

Fig.5. NF Vs Ls

3.2. S-parameters

Simulating S-parameters Vs frequency the results are shown in figure.6 and specified in Table .1.

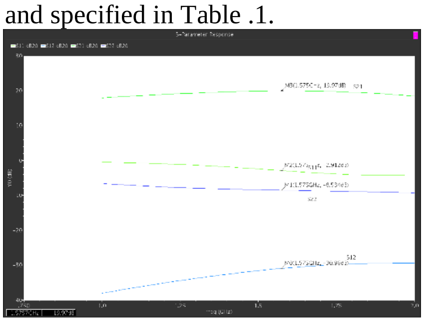

Fig.6. S-parameters Vs Frequency

When L_s Vs S-parameter analysis is performed, for L_s = 623.38pH S_{11} value is best and above or below this value S_{11} is corrupting, similarly S_{12} is degrading above 227pH and as L_s is decreased S_{21} and S_{22} are improving. This two component analysis is shown in figure.7 and figure.8.

Similarly L_g Vs S-parameters analysis gives that S_{11} is -3.88dB at Lg=9.5nH and corrupting for above or below this value.

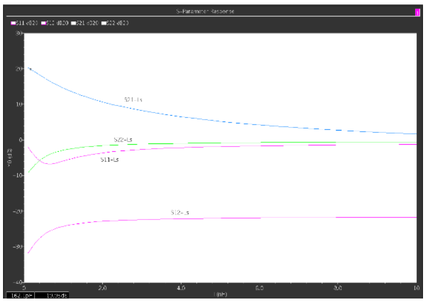

Fig.7. S-parameters Vs Ls

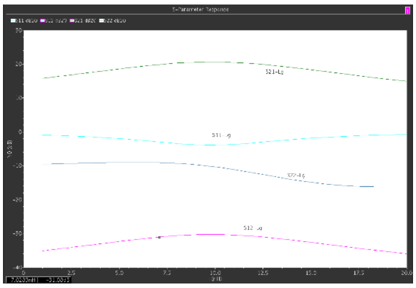

Fig.8. S-parameters Vs L_g

Table.1. Simulating S-parameters Vs frequency

f=1.5754GHz	S_{11}(dB)	S_{12}(dB)	S_{21}(dB)	S_{22}(dB)
	-2.912	-30.96	19.97	-8.534

3.3. Linearity

Non-linear behavior of the active devices operating at RF frequency should be considered. For large RF signals used as input these devices produce spurious signals. 1-dB compression point and IIP_3 are used to verify the linearity of LNA [1].

3.3.1-dB Compression Point:

For the LNA designed 1-dB compression point is equal to -14.57mdB, and meets to the specification. We can observe that in figure 9.

3.3.2 IIP3: Better the IIP3 of LNA, the healthier its linearity. IIP3 obtained was-12.5477mdB we can observe it in figure10.

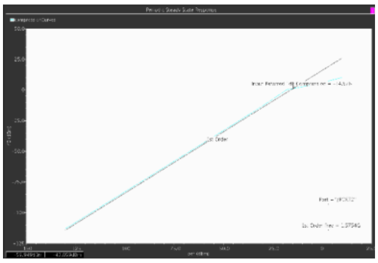

Fig.9. 1-dB Compression point

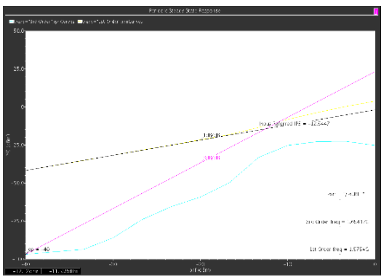

Fig.10. IIP3 measurement

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Simulated schematic of cascode LNA using a current mirror is shown in figure 11 and the Layout of LNA with a current mirror is shown in figure12.

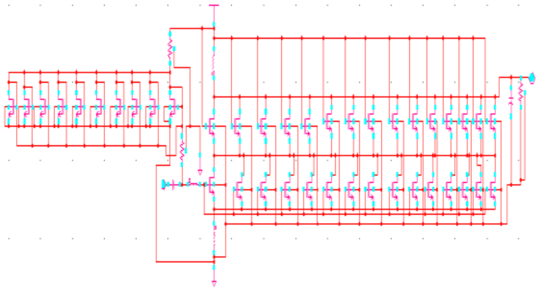

Fig.11. simulated schematic of LNA with current mirror.

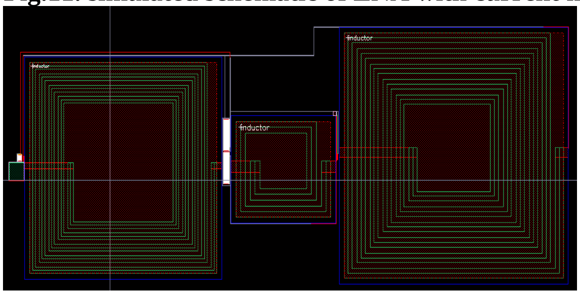

Fig.12. Layout of LNA with current mirror

Table 2. Performance of the proposed LNA

with different widths of biasing transistor M_3

W_3	$W_1/5$	$W_1/10$	$W_1/20$
NF(dB)	1.3	0.88	0.63
S11(dB)	-1.91	-2.37	-2.92
S12(dB)	-30.32	-30.84	-31.1
S21(dB)	15.52	17.96	19.82
S22(dB)	-4.84	-6.66	-9
VG(dB)	16.37	17.82	19.73
I (mA)	21.79	26.46	33.89
PD(mW)	15.25	18.5	23.72

PD: POWER DISSIPATION VG: VOLTAGE GAIN

II. CONCLUSION

A low voltage CMOS LNA with operating frequency of 1575.4MHz was designed using the CMOS 90nm process with an RF-spectre circuit simulator. The intended LNA exhibits power gain of 19.82db, S_{12} of -31.10dB, 1-dB compression point of -14.57mdB and IIP3 equal to -12.557mdB.The computer-generated results for the LNA show high VG, low NF, and low power dissipation at a low power supply voltage of 0.7v.

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