

PV Variations of Pulsed Latch Circuits

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Abstract: In this paper we studied the change in the result or action of different PV variations on the behaviour of Pulsed Latches by taking the reaction on both the Pulser and the Latch. Pulsed Latches are gaining reduced delay and power consumption in low power ASIC design technology. They provide another sequential element with high performance and low area and power consumption, taking advantage of both latches and flip-flop features. This process implements the pulser by using MUX based pulser design. This design approaches are presented to improve the quality of Pulsed Latches circuits by using their main importance of high performance, low power, and small area. The proposed design has low power variation when operating at normal supply voltage.

Index Terms: Pulsed latches, variability, process variation, scaling of voltage, less power.

I. INTRODUCTION

Flipflops are considered as the sequential elements used in most of the ASIC flow design technologies. There are used mostly because of they are easy to understand and are also easy to understand their performance in the timing diagrams, which verifies of the design and timing performance process is very easy. But the specific designs which we want high performance can regularly use latches due to their lower timing variations in some of the designs. Even latch based circuits are usually strong to clock skew, latches have a complex timing process, which will be complexes the circuit design and the process of verification.

Pulsed latches are one which is operated by short pulses, which are attained by the clock signal uses a pulse generator circuit called pulser. It is either embedded in the latch or can be move apart as an independent circuit. Many numbers of latches more than one are being shared by using only one pulser. So, it has the main favour of saving the power and area. The usage of the pulser can removes some of the clock buffers which is used in the clocks, for which it requires an extra power and area saving. [1]A pulsed-latch, which is a latch operated by a narrow clock pulse, is a promising alternative to the conventional flip-flop to reduce the power consumption.

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A pulsed-latch can be built from any transparent latch by supplying a clock pulse. Pulsed Latches which is always used to decrease power consumption and increase quality of being performing well [2]. A pulsed-latch-based design style was adopted for dynamic power reduction. A pulsed-latch can be modeled as a fast flip-flop. This allows conventional flip-flop designs to be migrated to pulsed-latch versions by simple replacement to reduce the clocking power

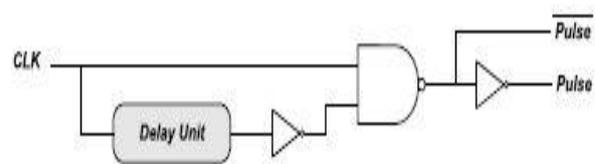


Fig 1.simple diagram of a pulser

The main block diagram of a pulser has been shown in Fig.1, where the pulser circuit will always have an odd number of inverters because it is responsible for containing the width of output pulses which is to be needed. To undertake the correct method, the pulser is created to achieve a pulse width which is greater than the latch write time. when the supply voltage is decreased the circuit become less stable with much failure rates. The quality which is to be required, so that it can perform well that will be attain at the lower voltage that should be given by increasing the width of the attained pulse. Here we have implemented the design approach that depends on the control for the delay path which contains delay unit and inverter by placing the inverter after the delay unit of the pulser circuit. Here we will use an outer control signal that is CTRL which is used to achieve a pulse width that can be controllable. The CTRL will be discussed in the design methodology part. The approach which we are doing had an importance of keeping the required level of quality of being performing well at various supply circumstances with low power and area variations when it was compared to the static conventional Pulsed Latches. The circuit which we are doing in this paper will help the Pulsed Latches to accurately achieve with the required timing margins at various supply voltages. The NAND gate and the inverter that are used after the delay unit and the odd number of inverters used because the NAND gate and inverter are used for the better output which can load the pulse into the proper sharp edges. This paper presents a study of reactions of process and the power variations at different supply voltages on the quality of being performing well of the conventional transmission gate pulsed latches.

This study includes the reaction on both the pulser and the latch which tells about the relation between them.

II. PROPOSED SYSTEM

Pulsed Latches will regularly reduce the power usage and increase work stability because of this stability we use Pulsed Latches. To be probably achieve the required nature of being performing to the good level, the pulser circuit must be redesigned at the run time to accomplish an output pulse and width is controlled based on the working condition.

Pulsed latch circuit is to be created to work correctly at low supply voltage with high level of quality of being performing well. Though when we reduce the given input voltage the circuit will be balanced low with the higher chance of failure rate. The required level of quality of being performing well at various supply voltages can be achieved at the low given input voltage by rising the width of the attained pulse.

Comparably by moving the pulser probability distribution to the right, we should adjust for the expandable change at low voltages and when we reduce the probability it may leads to the failure of the entire design. The approach which we discuss in this paper will depend upon the controlling of the delay unit which means delay unit and the inverter which is placed side by side of the Pulser circuit which is controlled by an external signal that is control CTRL which we discussed in circuit design which is to achieve a controllable pulse width.

There is also another approach for the Pulsed Latches in that it contains the supply rail that is separated which belongs to the pulser circuit and we must apply an extra controllable voltage which we measure the delay path when it should be needed.

The approach which we used in this paper is to use a different and a greater number of times taking units in the circuit diagram by selecting a delay unit at run time based upon the operation which we have used. The entire discussion of the proposed approach is discussed in the next chapter. The circuit which we have proposed in this paper will help in working the Pulsed Latches to work accurately which operates that what we needed in the timing margins at various input voltages.

Therefore, this will satisfy of getting the more help of Pulsed Latches at various functioning modes and architecture is very high in performance. The PL-MUX is very simple to design and easier to understand. But the power variations are more because of increase in the dynamic power because there will be an extra inverter. By this process the power and area will also be increases firstly when there is an addition of voltage, because of an more delay units and the greater multiplexer.

If the area is lesser it requires very less power based on the circuit area. So, if the area is lesser the implementation of the power switches is very difficult mainly it requires more control units for the circuit. To this process when all the connections are on it will run at low given input voltage but there is still a bit low in voltage is present on the power switches. Because of this the delay unit and the inverter which is beside the delay unit will be able to run at a low voltage than the remaining pulse circuit, generates a pulsed width slightly more than we expected.

III. METHODOLOGY

Pulsed-latch approach reduces dynamic power and used to decrease the power consumption and increase performance. We use latches instead of flip-flops without altering design style. Pulsed Latches will also take the data during sensitive time that is controlled by the width of clock waveform. If the pulse clock waveform triggers a latch, then latch is synchronized with the clock similarly to edge-triggered flip-flop because the rising falling edges of the pulse clock are almost identical in terms of timing. Basically, pulsed latches are level-triggered.

Pulsed Latches design of the pulser output width is so short may not be enough for the latches to store the information effectively, if the pulse width is too big then it will result in a large latch transparency window which, in turn increases the timing overhead or it can also violate the hold time requirements [3].

We know that Pulsed Latches are very time sensitive, so they must be considered while studying the reactions on various variations of the sources that is available. only D-Latch only produce same output, we given as input, so we use D-Latch to get output as same as input.

In this paper we show the variation reaction of Pulsed Latches during the design process. For example, if we see that Pulsed Latches are created to work at certain voltages which means that some voltage corner may or may not works at other voltage corner without breakdown in either execution or quality of being performing well. since we use the sequential elements such as Pulsed Latches we should be used within the die. any degradation in their execution or dependability can essentially influence the execution of the whole chip. Furthermore, since designing a chip that can consummately work at only a single voltage corner isn't a satisfactory solution these days.

In this paper, we are showing the different study of one of the important topology of Pulsed Latches, while we study the reaction of process voltage variations and proposed design changes that might be useful in reducing the possibility of design failure at various voltage constants. the proposed methodologies which are discussed, Pulsed Latches present a considerable option to MSFFs, giving higher execution, lower region and power utilization, and higher quality of being performing well and strongness to various kinds of modifications.

The main areas which we discussed in this paper are:

- The study which we done on the reaction of PV variations on the working of Pulsed Latches in high level technological nodes that will consider the reactions on both the pulser and the latches.
- Two epic pulse generator structures for the Pulsed Latches that can be used to expand the unwavering quality of Pulsed Latch designs, while keeping its fundamental preferences of high execution and less power utilization.



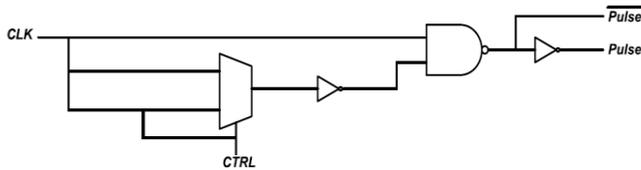


Fig 2. The proposed MUX-based pulser design

In this paper we use PL MUX which produces less delay. Mainly we use pulsed latch because pulsed latch allows capturing data in active state (high or low) of a clock signal. The conventional PL is intended to have one inverter in its delay path to produce the required pulse width [4]. The NAND gate and the inverter that are used after the delay unit and the odd number of inverters used because the NAND gate and inverter are used for the better output which can load the pulse into the proper sharp edges.

For proposed design PL-MUX, the require quality of being performing well levels can be accomplished at various supply voltages, with the additional reconfiguration capacity, design was unconventional distinguish to function properly at two different supply voltages. Since power utilization is a major measurement for such circuits, any power overhead connected with the proposed method should be reduced.

The conventional PL register operates at different voltages to reduce the delay. During normal operation, when running at a minimum supply voltage, the PL-MUX are nearly consuming the same amount of energy. When scaling the supply voltage down the PL-MUX seem to consume more power. However, the conventional PL register has higher probability of failure at this lower voltage. During this process we calculated the overhead time at different voltages of PV variations.

IV. REACTIONS OF PV VARIATIONS ON PULSED LATCHES

PL operations mainly depends on validate the latch for short time pulse which is attained by pulsed circuit, the variations in PL operations results on both the latch and pulse width. The results for process variations for latch and pulsed is repeated for different voltages and overhead time is measured.

A. Process variations.

Due to the changes in parameters in voltage and technology in present day life, even small change in parameters cause damage to the circuit operations [5]. The main challenges in designing is to measure the reaction of complex circuit and to find appropriate solutions to the circuit to functional it properly under different voltage variations. process variation mainly depends on the length variations. To study the variations in PL includes latch time and pulse width time. To know about write time of latch calculated by CLK to Q delay and pulse width Pulse width is greater than the required transfer window for latch. The region where there is high possibility then width of the pulse is smaller than required time of the latch for a circuit failure, we need to determine the minimum adjustable values for which is

acceptable for circuit failure and dimensions of transistors can be adjusted to obtain the output.

B. Voltage Scaling

Voltage scaling is approved technique in run time used for reducing the consumption of power in circuits. Scaling depends upon mainly two factors dynamic power and leakage power. The main objective is to reduce the voltage to minimum value by some time constraints [6]. Some variations in PV are usually adding bound for condition reactions. When supply voltage is decreases the gaining voltage also decreases and components becomes more changes to other variations. Voltage scaling mainly combined with increasing in delay time for different components, and it can be handled by the designer for different components in circuit. In PL case it depends on pulser and latches for different architectures. PL circuit is created to operate at minimum supply voltage and gradually decrease for lower voltages at optimum temperature. To overcome this one solution is to design PL circuit to operate with low operating voltage, because micro controller units operates at input voltage for different operating modes. One of the main advantages of it's low in timing overhead, to enlarge the risk for hold time reactions. In this paper the circuit approaches help in PLs to operate with timing margins for minimum supply voltages, and this will gain the maximum advantage of pulsed latches at various supply voltages being unimportant waste in designing execution.

V. DESIGN APPROACHES

The main block diagram of a pulser has been shown in Fig.1, pulser is created to achieve a pulse width which is bigger than latch time. it's difficult to implement a non-configurable pulsed circuit which operates with timing diagrams for various voltages in process. The pulser circuit is to be created to achieve output at run time for an output pulse and its width can be lead by operating conditions. Pulsed latch is created to operate at minimum voltage with high quality of being performing well. When scaling voltage is down then the supply voltage becomes less in quality of performance. The quality of being performing well can be gained at low supply voltage augment the width of pulse. The design mainly depends on clock signal and input latch signal and inverter of the pulser by using an extra control signal to achieve a control pulse width. This approach depends on using many delay units in pulser in runtime accordingly to operating conditions.

The width of pulse depends on delay, the switch is used as on/off button, output of multiplexer is used to connect odd number of inverters and final output is connected to NAND gate, the shortest delay is created at a minimum supply voltage and circuit is verified for different voltages and run at voltage variations.

VI. RESULTS

The implementation consists of one pulser and mux followed by NAND gate and output is connected to latch circuit, from the latch operated final output is taken. Basic .PL is proposed with three inverters to delay for generation of pulse width. The components are of minimum and its widths are varied. The inverter is of small size to decrease load on clock networks.

The NAND gate and its inverter are used to achieve sharp edges for output pulse.

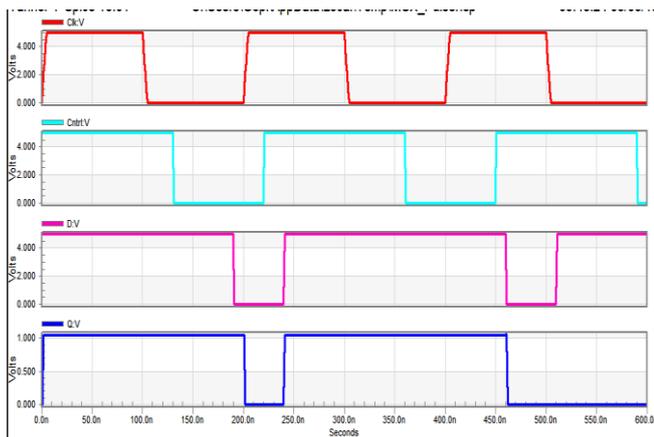
control is used to turn ON or OFF by the input control signal. In PL-MUX design a pulsar with two delay paths was assigned in odd number of inverters. After the output of MUX, we can connect odd number of not gates either three or five, but output doesn't change. The size of the inverters at the input to ensure same stable operation when voltage scales down.

This experiment was done in T-SPICE simulation tool using the synopsis 28nm, and input clock signal was given to 50ps. The minimum supply voltage we used was 1.05V and scaling voltage to 0.7V was applied to measure the overhead.

VII. POWER AND AREA COMPARISON

The power consumption is important aspect for all circuits and created approached was minimized. Average energy for each PL register is 1.05 V and PL-MUX also consumes same amount of power, but when power scales from 1.05V to 0.7V PL-MUX consumes more power. PL-mux consumes 9% to 14% of more power due to switching delay.

The area overhead has added some transistor to pulser circuit and added circuits is small and for PL-MUX register is 3%. PL-MUX is easy to design and few voltage scaling levels are measured, it is mainly used for minimum area and power overhead this design is prominent



VIII. CONCLUSION

In this paper the detailed examination of reaction on PV variations on the pulsed latches and performance was measured. This approach had a minimum area of around 3% or less. This approach is to measure different voltage levels of scaling, in addition it can be applied to any pulsed latches depends upon delay path to output pulse.

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