Design of FIR Filter using Wallace tree multiplier with Kogge-Stone adder

S.Rooban, Shaik. Saifuddin, S. Leelamadhuri, Shaik. Waajeed

Abstract: ***In present day scenario the need of high-speed applications and computational Systems in Digital Signal processing applications is drastically increased with increased mobile computing and multimedia applications. Whereas the FIR filter is a basic building block of any communication system. The previous works for the implementation of FIR filters using different multipliers overcomes the problems raised like optimization of area, delay and power. And the previous works comparison of various multipliers and adders has been carried out to find the best method to overcome the problems using the combination of Wallace tree and Kogge Stone***

Index Terms:- Wallace tree multiplier, Kogge-Stone adder, delay, adder, multiplier.

I. INTRODUCTION

Filters are the basic block of communication system. Filters are used to remove noise and interference from the signal and are also used to modify various characteristics of the signal. Among analog and digital filters, digital filters are more accurate and stable. There are two types of filters in communication systems, 1.Finite Impulse Response Filter 2.Infinite Impulse Response Filter.

A. FINITE IMPLUSE RESPONSE FILTERS

A filter whose impulse response is of finite duration is defined as FIR filter. It can be analog or digital with discrete time or continuous time. Digital filter works with the help of digital inputs also, called as non-recursive filters because it does not require feedback and it is shown in fig 1. Properties of FIR filters are they do not require feedback, they are stable and easy to design. Output of filter is Y[n] = X[n] * H[n]. Whereas the output for the M order FIR filter is in form $\sum_{k=0}^{M-1} x(k)h(n-K) = \sum_{k=0}^{M-1} x(k)h(n-k)$.

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S. Rooban, ECE, Koneru Lakshmaiah Educational Foundation, Guntur, India.

Shaik. Saifuddin, ECE, Koneru Lakshmaiah Educational Foundation, Guntur, India.

S. Leelamadhuri, ECE, Koneru Lakshmaiah Educational Foundation, Guntur, India.

Shaik. Waajeed, ECE, Koneru Lakshmaiah Educational Foundation, Guntur, India.

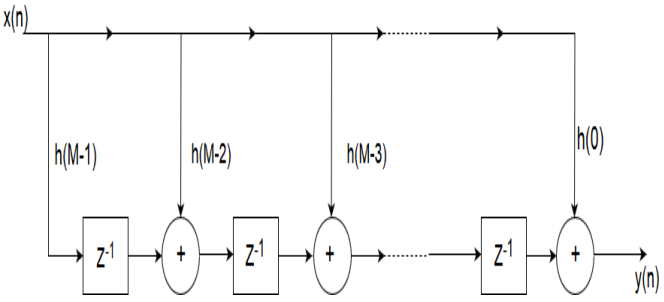

Fig 1 Finite Impulse Response Filter

B. INFINITE IMPULSE RESPONSE FILTER

The filters with feedback are called as Infinite impulse response filters it is shown in fig 2. Linear time-invariant system is most analog and as well as digital filters. System with this property is known as IIR frameworks or IIR channels and are recognized by having a motivation reaction which does not turn out to be zero past a specific point, but rather proceeds inconclusively.

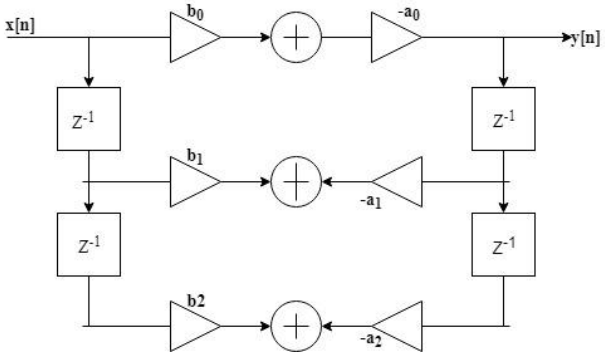

Fig 2 Infinite Impulse Response Filter

C. ADDERS

Addition is one of the four basic elementary operations, the other being subtraction, multiplication and division. Addition is one of the primary operations because we can perform other operations like subtraction, multiplication and division using the addition operation. Therefore, to design a fast, accurate and lesser power consumption adder, result in the increased speed of the devices. The basic form of addition is performed by half-adder and it is improvised by full-adder. In adders the carry bit plays a key role and the speed of the adder is definite to a great extent by the help of carry propagation. To reduce the carry propagation-delay various adders are designed.

Some of the most commonly used adders are carry-lookahead adder, carry-skip adder, carry-select adder, carry-save adder and parallel prefix adders. While designing an adder, lot of limitations comes into picture. The most basic adder has a very less area and is very easy to implement but the delay involved in getting the output is very huge. Hence different designs to overcome area and delay problems have come into picture. The power consumed is also an important constraint. Therefore, designing an adder with all these requirements is very important. The technology required for designing an adder plays a key role. In normal implementations CMOS logic is used. Additionally, Static CMOS technology, Differential Pass Transistor logic and complementary pass transistor logic technologies are used. These technologies help in increasing the strength of the signal at each level.

D. MULTIPLIERS

Multiplication is one of the important arithmetic operations and requires significantly more hardware resources and processing time than addition, subtraction and division. Multipliers are very important in the VLSI design of high-speed processors. Most of the multipliers were designed using Pass-transistor logic. The important objective of good multiplier is to provide a physically compact high speed and low power consumption unit.

II. METHODOLOGY

There are many techniques to overcome the problems in mobile computing and portable multimedia applications. As technology is evolving the size of the transistor is goes on decreasing. In our paper we choose the complex algorithm like Wallace tree to overcome the problems and further enhance to effective communication. FIR filter is one of the basic building block of communication system and we can use this filter to overcome area and delay problems. To optimise delay and filter area the multiplication technique is replaced by add and shift method. For addition operation we are using Kogge-stone adder and for multiplication technique we are using Wallace tree multiplier. In the proposed method parallel prefix adders are used because these are more flexible and faster than other adders like Ripple carry adder and to reduce delay parallel prefix adders are the best ones. In the proposed method we choose Kogge Stone adder as it occupies largest area compared to all parallel prefix adders but gives less delay than all the adders. Brent-Kung adder which occupies less area but gives more delay compared to Kogge stone adder. Han-Carlson adder which occupies less area but generates maximum delay among all the parallel prefix adders. The FIR filter with Wallace tree has three components namely WT, D flip-flop and RCA. For this filter WT is used because it is a high-speed multiplication technique which uses half adders and full adders are used for multiplication of two numbers. D flip flops are used to generate delay.

A. KOGGE-STONE ADDER

Kogge-stone adder is a parallel prefix (the output of the operation is based on the initial inputs) from carry look ahead adder and is shown in fig 3. It produces carry in time, and this is called as fastest adder, and this is mainly used in industries for high performance circuits. Kogge stone adder is known for its low depth and faster performance.

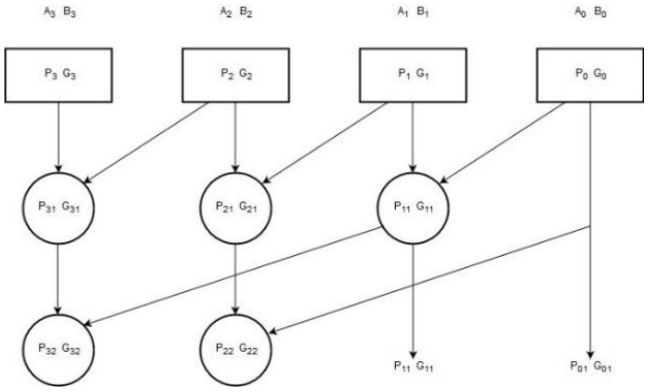

Fig 3 Kogge-Stone Adder

B. WALLACE TREE MULTIPLIER

It is an efficient hardware implementation of a digital circuit that multiplies two integers and it is shown in figure 4. The Wallace tree adder have three steps:-

- Multiplying each bit of the data with each bit of the other .
- Decrease the number of products to two by layers of full adders and half adders.
- Joining the wires in two numbers and add them with the adder .

The advantage of Wallace tree multiplier is it has less delay and it reduces the number of logic levels to perform the summation .The disadvantage of Wallace tree multiplier is its layout is complex and has irregular wires. The Wallace tree multiplier performs multiplication on any order of bits only in three steps which makes the computations to be performed to decrease. The input A of *n* bits and B of *m* bits are given as inputs to the Wallace tree multiplier it produces a product term of $n+m$ bits.

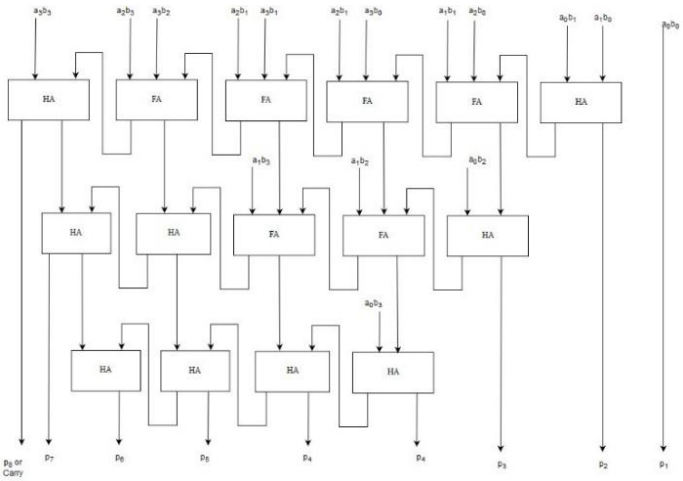

Fig 4 Wallace Tree Multiplier

III. EXPERIMENTAL RESULTS

A. VEDIC MULTIPLIER

Here we have chosen the Vedic multiplier as it is well known that the Vedic multiplier is faster than the conventional multiplier. A Vedic multiplier is one of the fast multipliers. Our Vedic multiplier has two 4-bit are fed as the input to the multiplier and it generates a one 8-bit product term.

And it can be used as a multiplier block in the filter. If much more concern is given to the delay factor, we need much faster multipliers. From our references we found the Wallace tree multiplier is faster than the previous multipliers. The 8-bit product term from one multiplier and another 8-bit product from another multiplier are fed as the inputs to a conventional adder which gives an 8-bit sum as the output form the adder and a carry bit also form the adder. Which forms a basic unit for the FIR filter, and it is shown in fig 5 and 6.

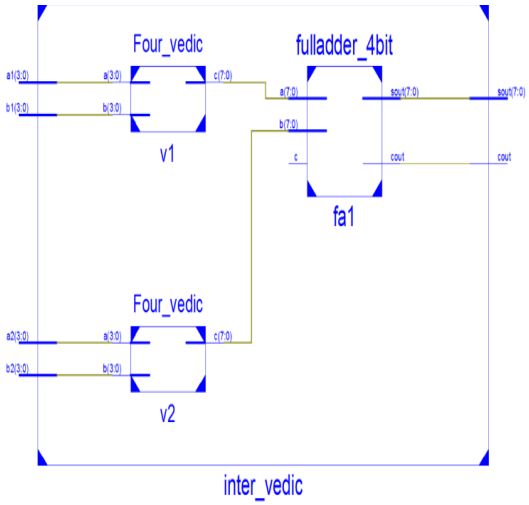

Fig 5 Fir Filter basic unit using Vedic multiplier and full adder

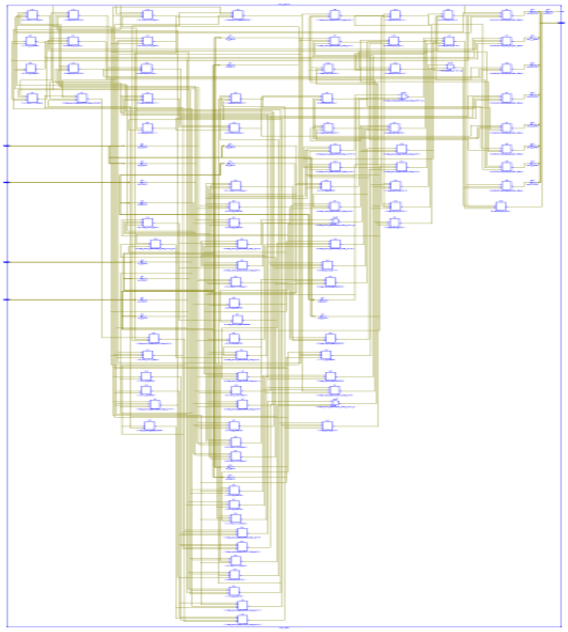

Fig 6 LUT structure of FIR filter using Vedic multiplier and full adder

B. WALLACE TREE MULTIPLIER

We have designed a basic MAC unit of the FIR filter which performs the operations of multiplication and addition. In order to use multiplication, we haven't used the conventional multiplier we have used a Wallace tree multiplier. Which uses only 3 stages to perform the multiplication operation. The main theme of using a Wallace tree multiplier is lower the delay of the circuit. As delay is the main concern of our project to perform faster operations. Which results in faster FIR filter. Here two 4-bit are fed as the inputs to the Wallace tree multiplier the resultant comes with a single 8-bit product term. Wallace tree multiplier performs the operations faster than the Vedic multiplier. The RLT schematic is shown in fig 7 and using system generator is shown in fig 8, simulation results are shown in fig 9, LUT structure is shown in fig 10.

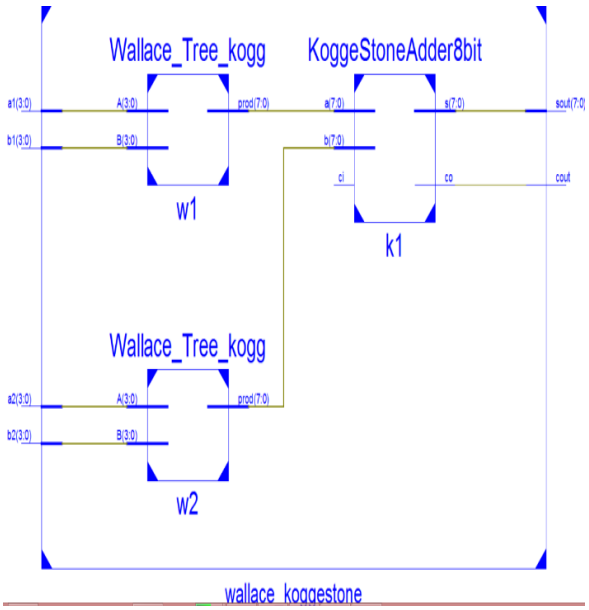

Fig 7 RTL schematic for a Wallace tree and Kogge stone adder

The RTL schematic and the LUT schematics are generated using the codes written in the ISE design suite using Verilog coding. We have also generated a basic structure of FIR filter using the MATLAB Simulink and Xilinx ISE design suite by using the System generator. We have dumped the Verilog code for the Wallace tree and the kogge stone adders individually into the black box elements of the Simulink. We have seen the outputs and verified it's working.

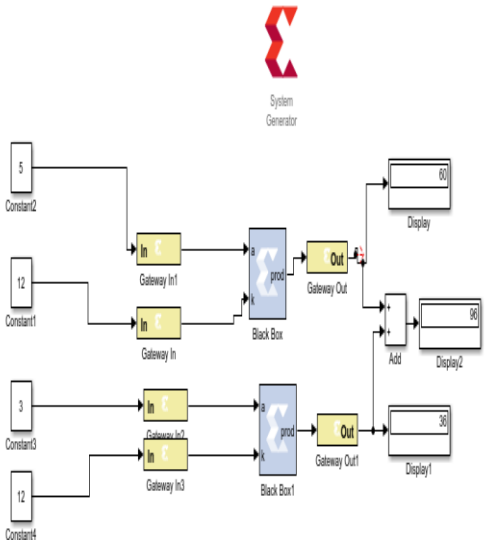

Fig 8 FIR filter design in system generator

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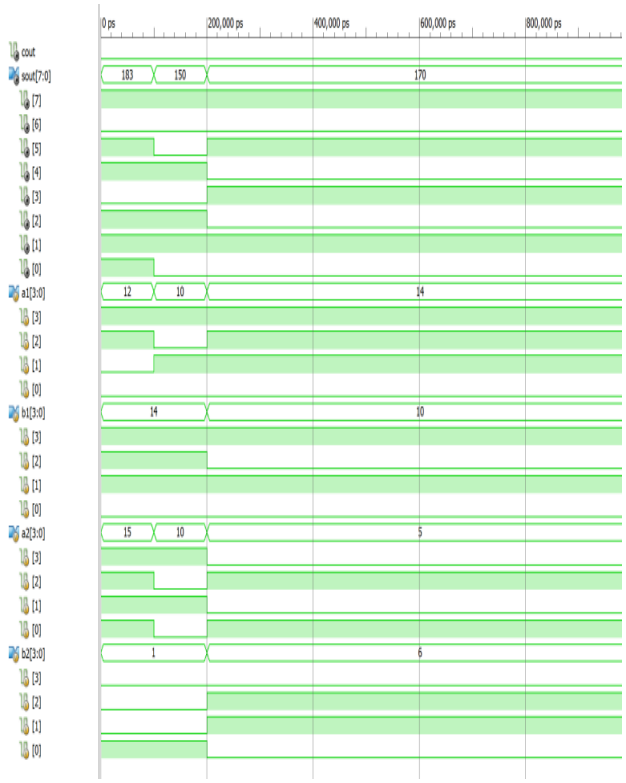

Fig 9 Simulation results for Wallace tree and Kogge Stone adder

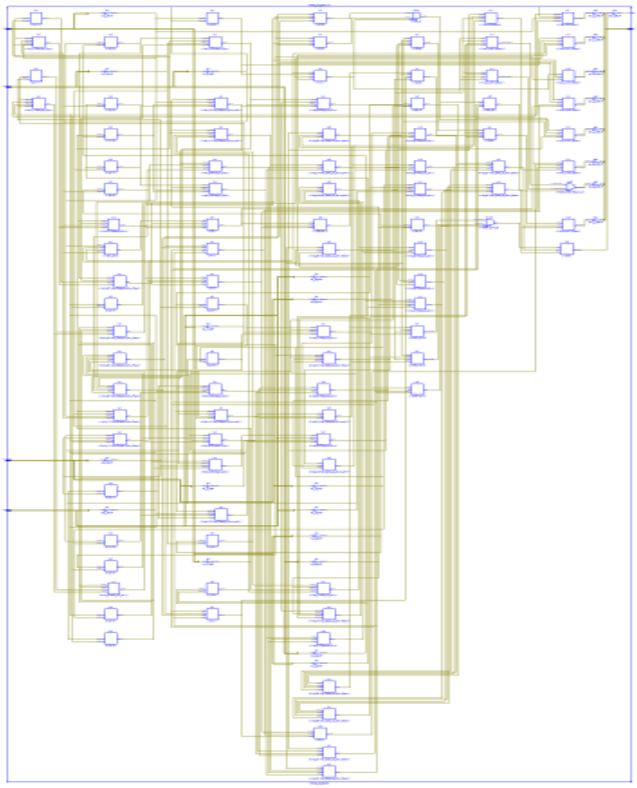

Fig 10 LUT structure for Wallace tree Kogge stone adder

IV. DISCUSSION OF RESULTS

We have found that the filter combination of the Wallace tree and the kogge stone adder has the faster response than the Vedic multiplier and the ripple carry adder. Whereas the combination of the Wallace tree has used less slices than that of the combination with the Vedic multiplier and the full adder.

Table I Simulation Results

Attributes	FIR filter with Vedic multiplier and ripple carry adder	FIR filter with Wallace tree multiplier and ripple carry adder	FIR filter with Wallace tree and kogge-stone adder
Logical Delay	10.826 ns	8.411 ns	5.421 ns
Routing Delay	6.193 ns	10.13 ns	8.155 ns
Total Delay	17.019 ns	18.541 ns	13.576 ns
No. of Slices	51	53	49
Bonded IOBs	25	25	25
No. of 4 input LUTs	94	98	87

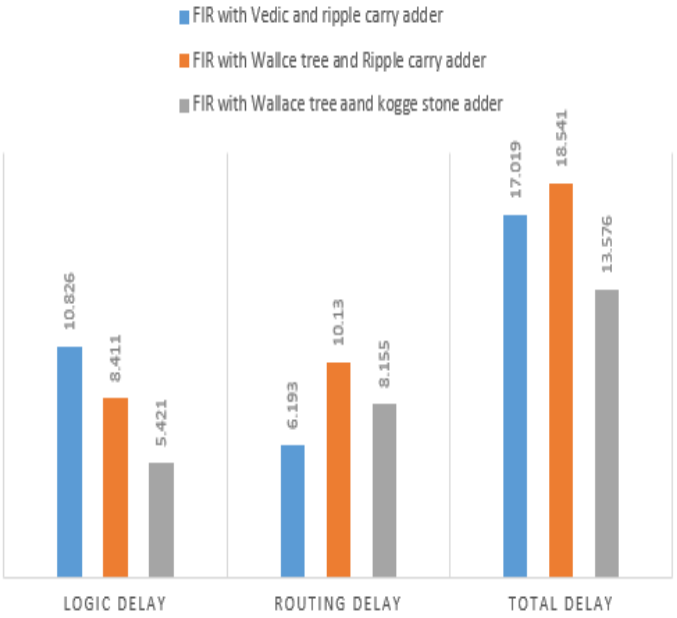

Fig 11 Delays for various Fir Filters

From the above Table I and the fig 11 we can observe that the no. of slices used by the basic unit with Wallace tree multiplier and kogge stone are less than the slices used by the Vedic multiplier and an 8-bit full adder. When the no. of bits dealing with are goes on increasing the no. of slices using are increased but the difference will be more. The delay when the order of the bits goes on increasing. The 4-input LUTs used by the basic unit from the Wallace tree multiplier and kogge stone adder are very less when compared to the basic unit from the Vedic multiplier and the full adder.

V. CONCLUSION

Number of slices, LUTs, and delay are very less for the FIR filter designed with Wallace tree and kogge stone model when compared to the FIR filter design with Vedic multiplier and a ripple carry adder. Even though we have got very less difference for smaller order of bits used. But when the bits dealing with increases the difference can be much bigger. And results in faster performing of filter operations.

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