# Performance Analysis of low power Dual Edge Triggered flip flop using power gating techniques

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***Abstract*: *Dual Edge Triggered flip flop is a sequential element that works on both positive (rising) as well as negative (falling) edges of clock signal. This flip flop exhibits some unique behavior which reduces leakage power when Muller C element is used to design the circuit. Hence five novel designs of DET are obtained by using sleep signals that bears some resemblance to common latch-mux DET flip flop but differs on operation. Along with these new DET design, such as Latch-Mux DET flip flop, True Single Phased DET flip flop, Conditional Precharge DET flip flop and Latch-Mux design that uses C element (for the function of multiplexer) are considered here. Performances of these designs are improved in the proposed method by using power gating technique. Power Gating is a technique which is used in the circuit to deliver the power, only when the circuit is in active mode. Power Gating Techniques such as Sleep Transistor logic and Lector stack are employed separately in the circuit. The former method uses sleep signals while effective stacking of transistors is incorporated in latter one in order to reduce the leakage power in the circuit. Performance analysis is carried out using TANNER simulation software tool.***

***Index Terms*: *C Element, Dual Edge Triggered (DET) flipflop, Lector Stack,Power Gating Technique, Sleep Transistor Logic*.

## I. INTRODUCTION

In digital systems, flip flop is used mainly for the purpose of storing the data for additional processing in registers and computational circuits. By cascading two oppositely phased latches, Single Edge Triggered flip flop can be designed that becomes active only on the rising edge or on the falling edge. This results in usage of anyone of clock edges, while remaining becomes idle.

Hence Dual Edge Triggered Flip Flop has been designed that incorporates both the clock edges for operation. While operating at half the clock frequency, data throughput of DETFF which is as same of SETFF's is maintained. Thus increases the performance by working at half the clock frequencies. Power dissipation of synchronous logic circuits is reduced due to the achievement of same data rate at half the clock frequency [1].However reduction of power dissipation has its impact on circuit complexity that increases the transistor count in circuit.

Latch-Mux design is common dual edge triggered flip flop design that performs better than single edge triggered design in terms of power consumed [2] only when unwanted switching transitions are rare. Hence DET Flip Flop can be designed using C Element which reflects its input value to output value only when both of it input are at same logic level otherwise it returns the previous state of the circuit.

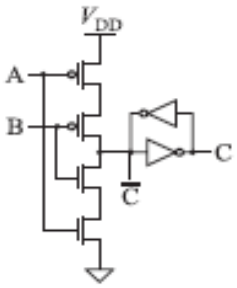


Fig.1. Transistor Diagram of Two input C Element

Fig.1 shows the transistor level implementation of two input C element. Using topology and variations of the C Element, new double edge triggered flip flops are designed that involves C Element as its main building block. The paper is structured as follows. Section II gives earlier works done in dual edge triggered flip flops. Section III includes design and analysis of newly designed double edge triggered flip flop using Muller C element. Section IV describes the proposed method used to elevate the performance of DET circuits. Section V involves simulation performed for designed circuits and comparison of new DET flip flop designs with its previously reported DET designs. Performance parameters such as area required for design (number of transistors used), average power consumed and delay metrics are added in the comparison table. Conclusion of this paper is presented in Section VI.

## II. RELATED WORKS

D type double edge triggered flip flop is introduced in order to avoid the wastage of power in idle clock frequency. It is implemented with few numbers of transistors and registers. When registers consisting of DET flip flops are used, it results in possibility of system level energy savings.

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In this paper, double edge triggered design involves parallel arrangement of D type latches, while serial fashion is followed for single edge triggered flip flop. Dual edge flip-flop that incorporates C-element to achieve the robust performance is presented [6] for the purpose of reducing energy required for its operation. There is no need to generate pulse separately for the operation, since direct clock pulses are provided to store the data. It minimizes dynamic power consumed by the clock signal. These results in better performing double data rate flip flops with simple configuration and small area.Special registers are required for sampling information at rising and falling clock edges. Complexity is high for these registers. Clock overlapping occurs in between the main clock signal and inverted pulse that is generated internally. Thus results in logical failures due to occurrence of cell contention. It is vulnerable during process variations and power supply scaling. True single phase clock [7] is used in double edge flip flops to eradicate the hazards due to overlapping of clock signals. It is done by avoiding inverted clock edge required for its functioning.Transparency windowing technique can be used to achieve the design of double edge triggered flip flop. After each clock (or) pulse edge, transparency window is generated. It can be provided by performing AND operation of signal CKD and pulse. It is done after the clock signal's positive edge. Performing Boolean AND operation of CK4 with CKD after negative edge of the pulse results in transparency window. By using this technique in SET CPFF, Conditional Precharge Dual Edge Triggered flip flop is achieved.In our work, performances of these designs and lector stack incorporated designs are analyzed and compared with one another in order to determine the improved performance of DET design by taking the average power consumed required for the flip flop's operation.

## III. ANALYSIS OF DET FLIP FLOP

Muller C Element can be used as a building block of double edge triggered design. It included here to reduce the switching of values thus reducing dissipation of power by the circuit.

*A. Low Glitch Power Flip Flop*

Low Glitch Power Flip Flop [3] consists of three inverting C elements because transistor level implementation of inverting topology is faster compared to non-inverting configuration of C element. This design bears some resemblance to commonly used design named Latch-Mux [5] flip flop but differs in the configuration. The input D in the circuit only determines whether to switch latch A or B at the next clock transition. Fig.2. shows the LG_C design that modifies the state of internal node with change at its first signal of input.

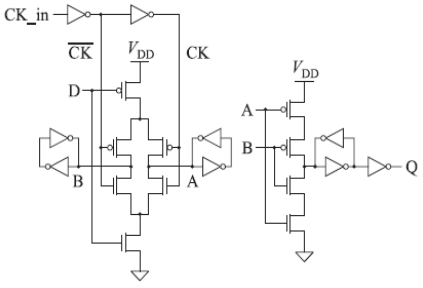


Fig.2.Transistor Diagram of LG_C Flip Flop

*B. In*

Implicit pulsed Flip Flop reduces the dynamic power dissipation occurring in LG_C flip flop but at the expense of increased dissipation due to clock signal transitions. Fig.3. shows IP_C design where merging of inner C elements is done with the two input C elements by sharing clocked transitions. Delay of this design is reduced and it has no static storage latches to store the values. This design does not have any weak feedback to overpower. Here node that is at D input toggles using strong transistor, while remaining node makes use of weak transistor. Behavior of overall circuit is static because of the cross connected inner C elements that reinforces the signal levels of the A and B nodes.

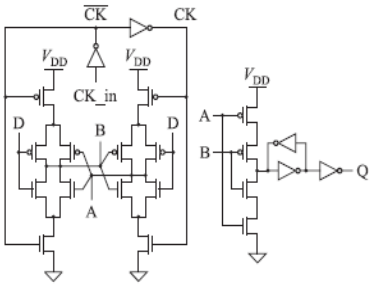


Fig.3. Transistor Diagram of IP_C Flip Flop

*C. Floating Node Flip Flop*

Power dissipation occurs in implicit pulsed due to toggling of signal levels at node A and B regardless of D and Q. Hence Floating node circuit shown in Fig.4 overcomes this problem by using two inputs and three input C element. Further output of this circuit is fed as feedback input to one of the terminal of three input C element. Here cross coupling of C elements ensures the signal levels of nodes are not same but opposite and one of them is at inversion of Q output. If value of D input and inverted clock signal are at same value, then node B is kept at logic high with the use of strong transistor.

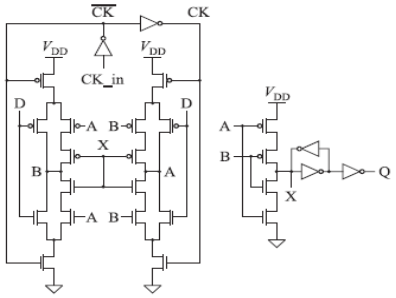


Fig.4. Transistor Diagram of FN_C Flip Flop

This makes node A, floating node. Similarly if values of D and clock signal CK are inverted, then it is the node B that starts to float. Reliability of the circuit is not affected by these nodes floating under the combinations of D and CK input signal.

*D. Conditional Toggle Flip Flop and its Modified Design*

A dynamic C element is placed at this design's output. Latch is used for maintaining the static behavior of the circuit.

Fig.5 design has less number of transistor count [4] compared to previous designs of double edge triggered flip flop that uses C element. It includes transistor for input, output signal and clock buffering. Latch part in this circuit consists of back to back connected inverter that toggles the node of X.

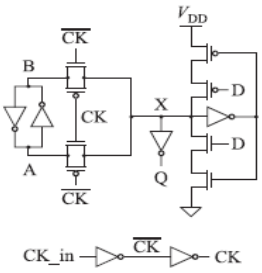


Fig.5. Transistor Diagram of CT_C Flip Flop

Toggling of stored values is performed only after the clock edge when input D is as same as its output Q. This conditional toggle flip flop performs better compared to previous designs but suffers from trade-offs. It is mainly between amounts of power dissipated and delay occurrence in circuit.

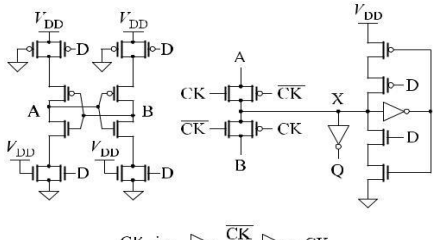


Fig.6.Transistor Diagram of CTF_C Flip Flop

Relaxing of trade-off is done so that faster switching and reduced energy dissipation is achieved [10] which is shown in Fig.6. Here both strong and weak transistors are used for proper working of circuit. Strength of signal levels depends on both transistor sizing and D input signal.

*E. Latch-Mux DET Flip Flop*

Common dual edge triggered flip flop consists of two latches and they are multiplexed to one output for proper operation. State of flip flop is changed by level triggering method [5].This result in a transparent latch following the changes that occurs in its input signal. It overpowers single edge flip flops performance in terms of power consumed by the circuit.Fig.7.shows Latch-Mux DET design.

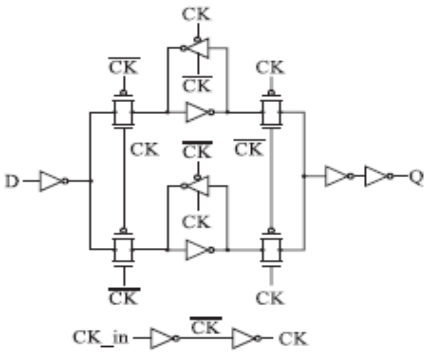


Fig.7. Transistor Diagram of LM Flip Flop

Here clocking activity results in more power dissipation when compared to transitions occurring in input signals. Circuit works based on the selection input clock signal. It involves transmission gate for transferring the value of D input to the output signal Q. It is similar to latch-mux single edge triggered flip flop. But they differ in arrangement of latches.

*F. Latch Mux Design using C Element*

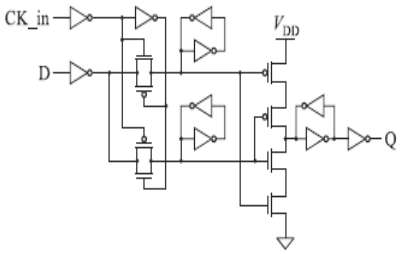


Fig.8. Transistor Diagram of LM_C Flip Flop

Fig.8 shows the Latch Mux flip flop designed using Muller C element. Here memory capable logic C element is mainly used for performing the function of multiplexer. Latches that are at higher and lower level receive the input for operation. C-element performs inverting operation when both of its inputs are at same logic level. The weak keeper structure used at the output has two functionalities. It retains the C element's output when PMOS and NMOS transistors are switched off [12]. State of output is refreshed even in the presence of large amount of leakage current. Charge sharing issues that occurs in circuit is eliminated by the back to back connected inverter circuit.

*G. True Single Phase Clock DET Flip Flop*

Design is similar to latch mux flip flop yet the usage of inverted clock signal is avoided. Overlapping of clock signals is solved by this design. Dual feedback mechanism [7] is achieved in circuit internally; it also assures the fixed operation of design. Performance of circuit is robust even under different scaled supply voltages and process variations. During one clock phase; writing of new data is performed into internal storage node. These data are latched and then driven to the output in the next clock transition.

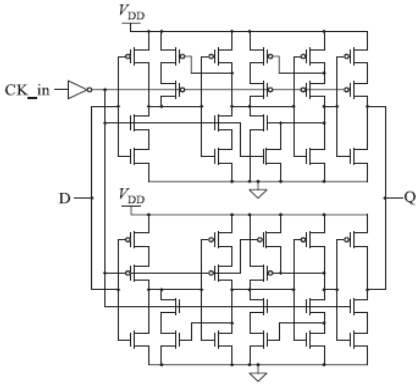


Fig.9. Transistor Level Schematic of TSP Flip Flop

The storage elements are implemented with a pair of TSPC latch-MUX branches thus eliminating the need for inverted pulse signal. Classic TSPC latch is included along with two internal feedback mechanisms for strong data levels. Thus fully-static operation is ensured in order to enable robust, low-voltage functionality.

*H. Conditional Precharge DET Flip Flop*

Conditional Precharge design is achieved by incorporating transparency window technique that is implemented after every clock edge. It is simpler configuration and easy one to implement. Generation of signal CKD is done that switches low when delayed CK2 is in rising edge. Falling edge of CK2 causes it to switch high. Main clock signal is logically ANDed with CKD to provide transparency window after the positive clock edge. Half of power consumed by network that distributes clock signal is saved when dual edge clock scheme is used. This benefit in relaxing the clock distribution system design, and avoids penalty occurrence in throughput.

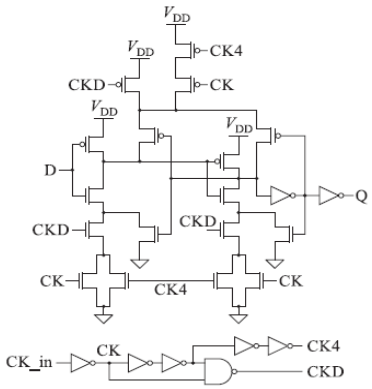


Fig.10. Transistor Diagram of CP Flip Flop

## IV. PROPOSED WORK

Power is the major factor in VLSI design field since every circuit depends on this parameter in order to perform its specific operation. Power may leak in the circuit when it is switched off, thus degrading circuit performance. Various techniques were introduced in order to reduce power consumed thereby minimizing the leakage power.

$$P_{leakage} = V_{DD} I_{leakage}$$

Static power dissipation is caused in CMOS circuits [11] because of scaling voltages that shows its effect by increasing sub threshold leakage current. In order to minimize leakage current without having any impact on dynamic power dissipation, power gating techniques such as Sleep Transistor and LECTOR methods are used. These techniques supply power only when circuit is active and shuts off power at idle states of the circuit.

Sleep transistor uses sleep signals at header and footer switch [13]. It works on two modes namely active and sleep mode in order to reduce leakage power in the circuit. **LE**akage **C**ontrol **T**ransist**OR**s (LECTOR/LCT) for both P type and N type were introduced [9]. Separate circuitries are not necessary in this technique for monitoring the circuit states. This approach was incorporated in high and low threshold voltage circuits. Two leakage control transistors are introduced such that anyone of LCTs is near its cut-off region of operation. Source terminal of one LCT controls the gate terminal of other LCT. Duplication of each transistor in the network is done with both transistors regard.

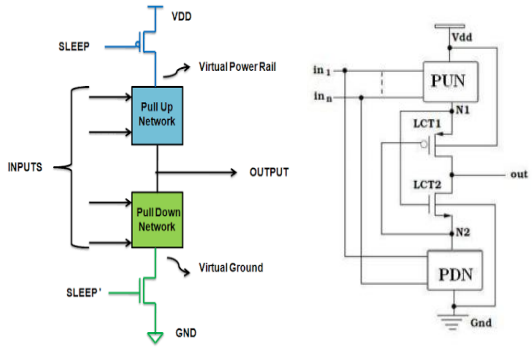


Fig.11. Transistor Level Schematic of Sleep Transistor and Lector Stack method

Leakage current is decreased significantly since one of transistor that controls leakage current is always near the sub threshold region which in turn increases resistance of path from $V_{dd}$ supply to ground terminal. LECTOR is vector independent and the required control signals are generated within the gate.Static power (leakage power) dissipation is the one that occurs when outputs of gate are not changing. Power gating technique turns of the device by cutting OFF the supply voltage. During standby mode, stack effect is created.

## V.SIMULATION RESULTS

*4.1. Low Glitch Power Flip-flop*

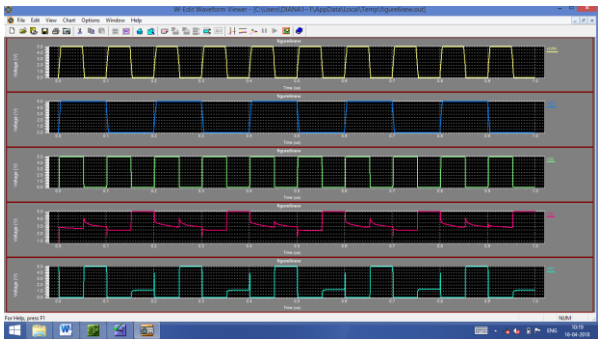

Fig.12.Output Waveform of LG_C Flip Flop

*4.2. Implicit Pulsed Flip-flop*

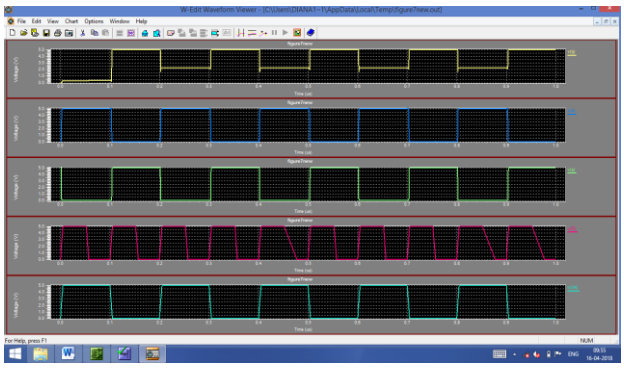

Fig.13.Output Waveform of IP_C Flip Flop

*4.3. Floating Node Flip-Flop*

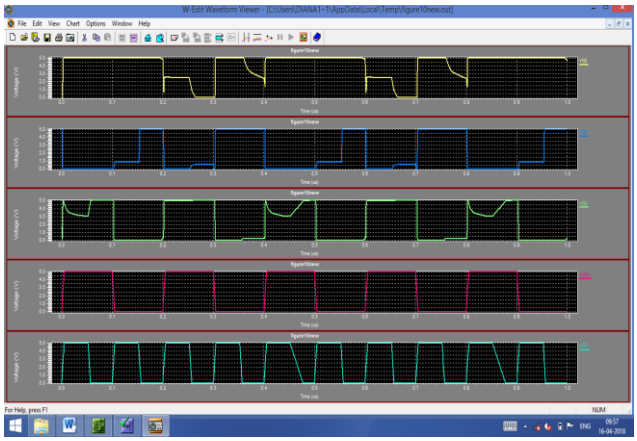

Fig.14.Output Waveform of FN_C Flip Flop

*4.4. Conditional Toggle Flip Flop (Modified design of Conditional Toggle Flip Flop)*

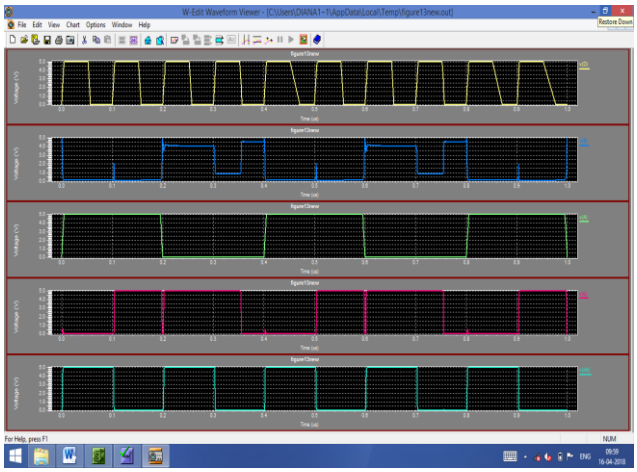

Fig.15.Output Waveform of CT_C Flip Flop

*4.5. Latch Mux DET Flip Flop*

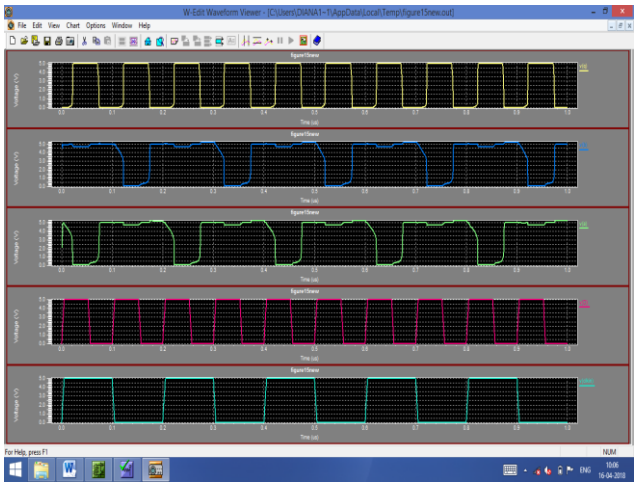

Fig.16.Output Waveform of CTF_C Flip Flop

*4.6. Latch Mux Design using C Element*

Fig.17.Output Waveform of LM Flip Flop

*4.7. True Single Phase Clock DET Flip Flop*

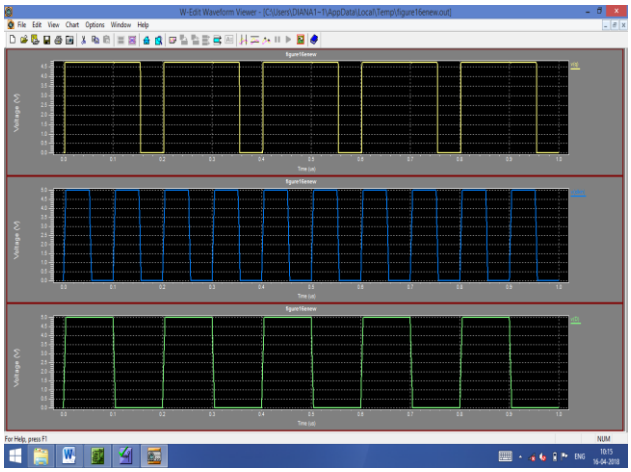

Fig.18.Output Waveform of LM_C Flip Flop

*4.8. Conditional Precharge DET Flip Flop*

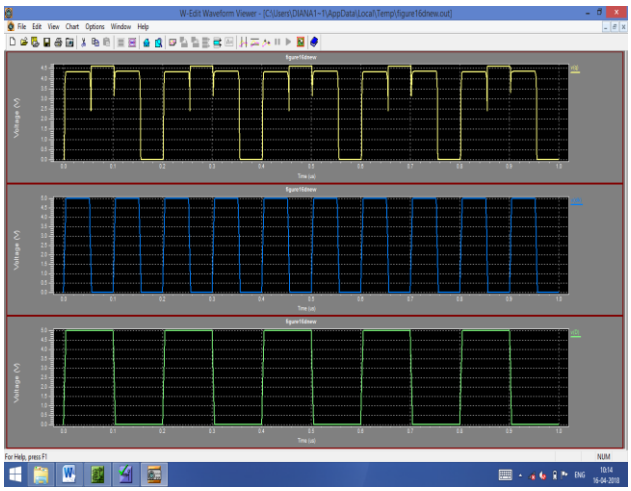

Fig.19.Output Waveform of TSP Flip Flop

Table.1. Table that shows the performance of circuits without any power gating techniques.

| FLIP FLOP | TRANSI -STOR COUNT | POWER (mW) | DELAY (ns) | POWER DELAY PRODUCT (nJ) |
|---|---|---|---|---|
| LG_C | 23 | 4.265 | 27.78 | 0.11848 |
| IP_C | 27 | 4.914 | 24.35 | 0.11965 |
| FN_C | 30 | 3.435 | 24.32 | 0.08353 |
| CT_C | 24 | 2.239 | 12.24 | 0.02740 |
| CTF_C | 32 | 2.932 | 19.15 | 0.05614 |
| LM | 30 | 10.43 | 26.73 | 0.27879 |
| LM_C | 28 | 9.768 | 52.55 | 0.51330 |
| TSP | 44 | 2.926 | 28.48 | 0.08333 |
| CP | 45 | 3.755 | 53.07 | 0.19927 |

Table.2. Table that shows the performance of circuits with sleep transistor technique.

| FLIP FLOP | TRANSI-STOR COUNT | POWER (mW) | DELAY (ns) | POWER DELAY PRODUCT (PDP) (nJ) |
|---|---|---|---|---|
| LG_C | 28 | 8.12 | 24.78 | 0.201 |
| IP_C | 26 | 8.96 | 24.30 | 0.217 |
| FN_C | 30 | 6.25 | 24.37 | 0.152 |
| CT_C | 20 | 5.19 | 12.16 | 0.063 |
| CTF_C | 28 | 5.45 | 18.40 | 0.1002 |
| LM | 26 | 17.76 | 26.31 | 0.467 |
| LM_C | 28 | 10.71 | 52.60 | 0.562 |
| TSP | 38 | 13.86 | 26.03 | 0.360 |
| CP | 35 | 6.82 | 26.18 | 0.178 |

Table.3. Table that shows the performance of circuits with lector stacks technique.

| FLIP FLOP | TRANSI-STOR COUNT | POWER (mW) | DELAY (ns) | POWER DELAY PRODUCT (nJ) |
|---|---|---|---|---|
| LG_C | 33 | 0.504 | 27.93 | 0.01407 |
| IP_C | 41 | 0.467 | 24.47 | 0.01142 |
| FN_C | 36 | 0.824 | 24.37 | 0.02008 |
| CT_C | 40 | 0.957 | 12.29 | 0.01176 |
| CTF_C | 40 | 0.342 | 18.49 | 0.00632 |
| LM | 46 | 8.44 | 26.62 | 0.22467 |
| LM_C | 46 | 7.69 | 29.90 | 0.22993 |
| TSP | 44 | 2.42 | 28.94 | 0.07003 |
| CP | 57 | 2.52 | 26.53 | 0.06685 |

The above table represents the enhanced performance achieved by DET circuits in terms of average power consumed, power delay product which is also called energy. Based on performance parameters, Bar charts are drawn for pictorial representation.

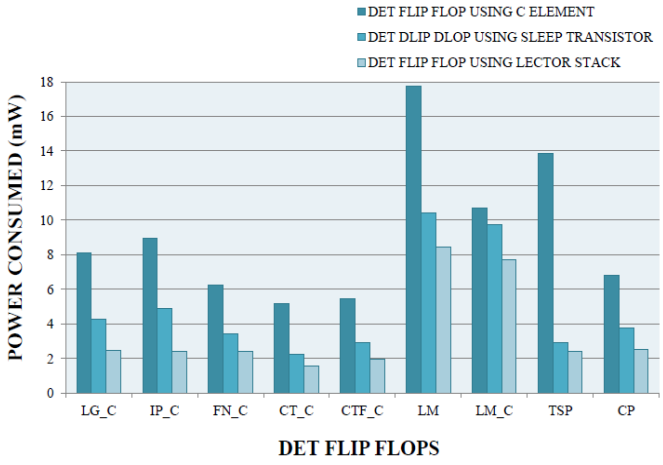


Fig.20.Bar chart showing the circuits' power comparisons

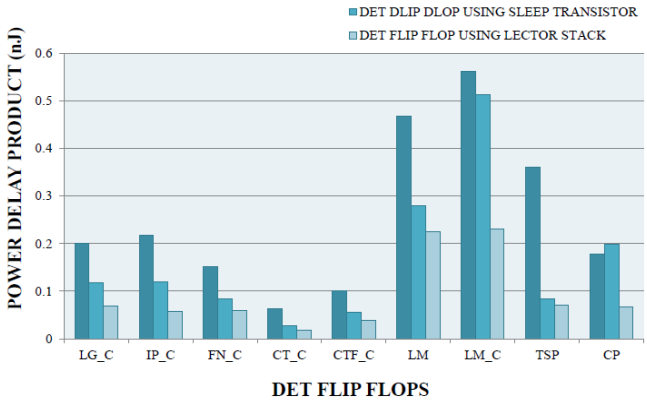


Fig.21.Bar chart showing the circuits' energy comparisons

## V. CONCLUSION

This work involves the five novel designs of dual edge (DET) triggered flip flop using Muller C element. Additionally previously reported DET designs are taken here for performance comparison. Proposed method involves incorporation of effective lector stack technique and sleepy logic separately in existing circuits to minimize the leakage power that occurs during circuit's standby mode. Proposed circuits show better performance in terms of power consumed and power delay products (energy). Among two power gating techniques considered here, LECTOR method is efficient in power reduction when compared to logic that uses sleep signals.

## REFERENCES

1. N. Nedovic and V. G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 5, pp. 577–590, May 2005.
2. A. G.M. Strollo, E. Napoli, and C. Cimino, "Analysis of power dissipation in double edge-triggered flip-flops," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 5, pp. 624–629, Oct. 2000.
3. Stepan Lapshev and S. M. RezaulHasan, "New Low Glitch Low Power DET Flip-Flops Using Multiple C-Elements," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 63, no. 10, pp. 1673–1681, Oct 2016.

4. S. V. Devarapalli, P. Zarkesh-Ha, and S. C. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using C-elements," in Proc. 11th Int.Symp. Quality Electron.Des. (ISQED), Mar. 22–24 2010, pp. 147–150.
5. A. Gago, R. Escano, and J. A. Hidalgo, "Reduced implementation of D-type DET flip-flops," IEEE J. Solid-State Circuits, vol. 28, no. 3,pp. 400–402, Mar. 1993.
6. R. Hossain, L. D. Wronski, and A. Albicki, "Low power design using double edge triggered flip-flops," IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 2, no. 2, pp. 261–265, Jun. 1994.
7. A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true single-phase clock dual-edge-triggered flip-flop," in Proc. IEEE Int.Symp. Circuits Syst. (ISCAS), May 24–27 2015, pp. 1850–1853.
8. Narendar Hanchante, Nagarajan Ranganathan, "LECTOR : A technique for leakage reduction in CMOS circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 2, pp. 196–205, Feb 2004.
9. M.Ramya, P.Shantha Devi, M.Jeyshri and P.Devi, "Reducing power, leakage and area of standard cell using lector stack, " International Jour.of Engg.and Tech., vol. 04, Issue - 05, May 2017.
10. M. Shams, J. C. Ebergen, and M. I. Elmasry, "Modeling and comparing CMOS implementations of the C-element," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 6, no. 4, pp. 563–567, Dec. 1998.
11. PreethiVerma, R.A. Mishra, "Leakage power and delay analysis of LECTOR based CMOS circuits," International Conference on Computer and Comm. Tech. (ICCCT)-2011.
12. Vinay Kumar Madasu, B Kedharnath, "Leakage Power Reduction by using Sleep Methods," International Journal of Engineering And Computer Science (IJECS), Volume 2, Issue 9, Page No. 2842-284, September 2013.
13. G. MareswaraRao, S. Rajendar, "Design of Low Power Pulsed Flip-Flop Using Sleep Transistor Scheme," International Conference on Advances in Electrical Engineering (ICAEE), December 2013.

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