Design and Completion of Asymmetric Single Phase 27 level Cascaded MLI for various PWM Scheme

D. Periyaazhagar, G. Irusapparajan

Abstract: ***Multilevel inverter is most fashionable due to bargain switching losses, short costs, minimum harmonic distortion and hug voltage capacity while compared with conventional PWM converters. A latest family of multilevel inverters that has decreased number of separated input DC sources had emerged named as asymmetric multilevel inverter. In this work, theories and use of a variety of PWM modulation schemes for twenty seven level asymmetric multilevel inverters are tested. The relative case study is offered to authenticate the tested modulation scheme through harmonic spectrum analysis, magnitude of output voltage, Total harmonic distortion (THD), and distortion factor (DF). The demonstration of chosen single phase trinary DC source multilevel inverter is established through MATLAB-SIMULINK based simulation. Finally then the experimental result shows that APOD PWM offers AC output with relatively low harmonic distortion. It's also realized that COPWM strategy is originate to perform superior since it delivers relatively higher fundamental RMS AC output voltage.***

Keywords: ***Single phase multilevel inverter, Multi carriers, Sixty Degree PWM, Twenty seven levels, Cascaded multilevel inverter, and Distortion Factor.***

I. INTRODUCTION

Multilevel inverters are usually worn to create a close to sinusoidal voltage since dissimilar levels of DC input source voltages and this projected single phase Trinary cascaded H-bridge inverter is worn to reduce the numeral semiconductor switches. This recommended 27 level single phase cascaded asymmetric H- bridge multilevel inverters have to a smaller number of switching component to get the equal number of ac output voltage levels once equated to FCMLI and DCMLI kind inverter topology. The research requires less significant switching devices as compared by means of expected cascaded H-bridge inverter topology. Furthermore, it frequently regularizes the AC staircase waveform of output voltage from several input DC sources which has minimized total harmonic contents. A trinary base cascade one phase asymmetric MLI with various kind of load [1]. Multilevel inverter topology by using a Flip flop and suggested control techniques for several bipolar PWM approaches of a 3-phase 5-level cascaded inverters [2].

The minor voltage stepladder leads to the formation of advanced power quality ac output waveforms and also reduces voltage stress at point of load terminal and the EMI compatibility concern [3]. Drawback of MLIs are miniature voltage stepladder is usually formed by isolated input voltage sources. Isolated input voltage sources could not always be freely available, and string capacitors need for balancing voltage [4]. MLIs such as stacked multi unit (SM), cascaded MLI (CM), flying capacitor multilevel (FC) and double flying capacitor multi cell (DFCM) have significant advantage of calming output voltage worth of inverters, but they want frequent isolated dc source input power. Considering the benefit of adapted stacked multi cell (SM) inverter over flying capacitor (FC) and stacked multi unit (SM) inverter, and noting that transmission and switching loss examination can be gainful in plan of MLI, a systematic practice to evaluate and inspect the transmission and switching losses in modified stacked multi unit (SM) converter is offered [5]. In [6], a new arrangement of stationary ground power part based on a latest twenty five level hybrid neutral clamping multi level inverter with less number of device is projected. In [7], a novel three-phase MLI is projected. Construction of projected inverter has frequent modular primary units that are coupled in series arrangement. A novel flying capacitor clamped (FC) 5-level inverter based on modular bridge capacitor switched topologies is projected in [8].Voltage regulation of DC link in multilevel inverter preserves a key role in the recent power conversion method for changeable voltage and changeable frequency purpose like industrial motor drives, traction system, hybrid electric and electric vehicles [9–11] etc. Different industrial application comprise begun to necessitate huge power equipment in latest years with average voltage and huge power [12]. For huge power use, multilevel inverter appear to suitable result due to the reality that the MLI generates improved quality of voltage by means of raise in quantity of level with usual semiconductor switches while compared among two-level inverter [13, 14].

II. PROPOSED ASYMMETRICAL INVERTER CONFIGURATION

The most important thoughts to spring up by means of a common arrangement for an uneven dc source single-phase asymmetrical cascaded MLI right to offer variable levels of output ac voltage.

Revised Manuscript Received on April 07, 2019.

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This practice rejects the especially huge number of bulky transformers important by surprising multi pulse inverters structure; the diode clamped type inverters require clamping diodes and the flying capacitors important for flying capacitor type MLIs. This system consists of a sequence arrangement of several numbers of H-bridge inverters. Each H-bridge inverters have the similar bargain as a traditional single phase full bridge inverter. This method introduces the novel thought of using unlike DC input sources to yield an output AC voltage waveform. Each H-bridge inverter is joined to its hold DC input source. By cascading the AC output voltage of each H-bridge inverter a stepped output AC voltage waveforms to be generated. If the numeral of partly is M, after that the output AC voltages are achieved by accumulation the output AC voltage of every part of bridges as shown in equation.Fig.1. Protest a circuit configuration of a cascaded asymmetrical H-bridge MLIs attractive input Trinary DC source.

It similar to a traditional H-bridge cascaded MLI apart from input DC sources. Through $9V_{DC}$, $3V_{DC}$ and $1V_{DC}$ it can create 27 output levels;

$$0, \pm 1V_{DC}, \pm 2V_{DC}, \pm 3V_{DC}, \pm 4V_{DC}, \pm 5V_{DC}, \pm 6V_{DC}, \pm 7V_{DC},$$
$$\pm 8V_{DC}, \pm 9V_{DC}, \pm 10V_{DC}, \pm 11V_{DC,} \pm 12V_{DC}, \pm 13V_{DC}$$

The bottom inverter generate a basic output voltage with 9-levels, and then the center inverter generate a output voltage with 3-levels, and the top inverters subtracted or added one level starting the basic output wave to merge stepped output waves. Now, the first stage output AC voltage level becomes the arithmetic sum of every terminal output of H-bridge, and it is exposed as equation 1.

$$V_{out} = V_{DC} + 3V_{DC} + 9V_{DC} \qquad (1)$$

Where, $9V_{DC}$, $3V_{DC}$, and V_{DC} are the output Voltage of bottom, center and top of individual H-bridge. In the projected 27-level inverter circuit design, if *K* number of cascaded H-Bridge part have different DC input sources in sort of the authority of 3, a expected output ac voltage levels are specified as

$$V_m = 3^K, \mathrm{K} = 1, 2, 3..... \qquad (2)$$

In ternary evolution the amplitude of DC input voltages strong ratio 27: 9: 3: 1. . : 3K and the greatest ac output voltage reach near $((3^K - 1)/2)$ V_{DC} and the ac output voltage levels will be (3^K). Extra irregular DC input voltage is corresponding intermission DC input voltage growth. The switching pattern and its output voltage are exposed in table 1.

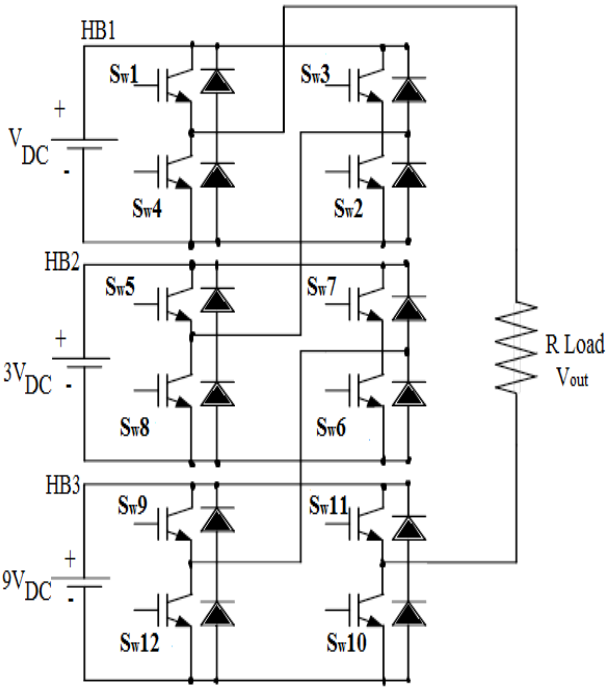


Fig. 1 Proposed Asymmetrical inverter configuration

Table. 1 Switching chain of Proposed MLI

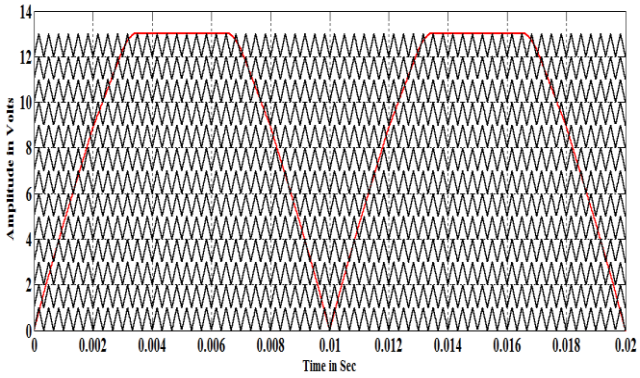
Top H-Bridge (HB1)	Center H-Bridge (HB2)	Bottom H-Bridge (HB3)	AC Voltages (V_{out})
P	P	P	+13 V_{DC}
Z	P	P	+12 V_{DC}
N	P	P	+11 V_{DC}
P	Z	P	+10 V_{DC}
Z	Z	P	+9 V_{DC}
N	Z	P	+8 V_{DC}
P	N	P	+7 V_{DC}
Z	N	P	+6 V_{DC}
N	N	P	+5 V_{DC}
P	P	Z	+4 V_{DC}
Z	P	Z	+3 V_{DC}
N	P	Z	+2 V_{DC}
P	Z	Z	+1 V_{DC}
Z	Z	Z	0V_{DC}
N	Z	Z	-1 V_{DC}
P	N	Z	-2 V_{DC}
Z	N	Z	-3 V_{DC}
N	N	Z	-4 V_{DC}
P	P	N	-5 V_{DC}
Z	P	N	-6 V_{DC}
N	P	N	-7 V_{DC}
P	Z	N	-8 V_{DC}
Z	Z	N	-9 V_{DC}
N	Z	N	-10 V_{DC}
P	N	N	-11 V_{DC}
Z	N	N	-12 V_{DC}
N	N	N	-13 V_{DC}

III. PULSE WIDTH MODULATION CONTROL SCHEME

The most admired scheme of calculating the output AC voltage is to integrate MCPWM systematize contained by the inverters. In this technique, a fixed input DC voltage is given to the inverter and a variable output AC voltage is obtained by changing the on time and off time of the inverter semiconductor devices. It is usually accepted that raising the switching frequency of the MCPWM model decreasing the lesser frequency harmonics content by changing the switching frequency of triangular carrier harmonics and related sideband harmonics content more away from the basic frequency component. The modulating waves of MCPWM strategy engaged in this work are 60 degree PWM signals. The reference 60 degree PWM waveform is constantly coordinated with every carrier wave. If the reference 60 degree wave is extra than a carrier wave, then the energetic switching plans corresponding to that carrier are switched ON or else, the switching plans switched OFF.

In Phase Disposition PWM plan (IPD)

The In Phase Disposition PWM plan is to use the thirteen carriers with single sixty degree reference waveform. In Phase Disposition PWM plan all the thirteen carriers are in phase with every other and the thirteen carriers have equal amplitude. Fig.2 (i) Appearances of multicarrier agreement for IPDPWM plan for ma = 1 and modulating frequency is mf = 50.



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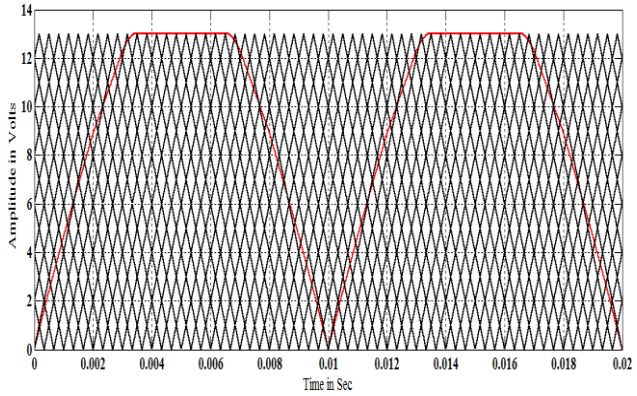
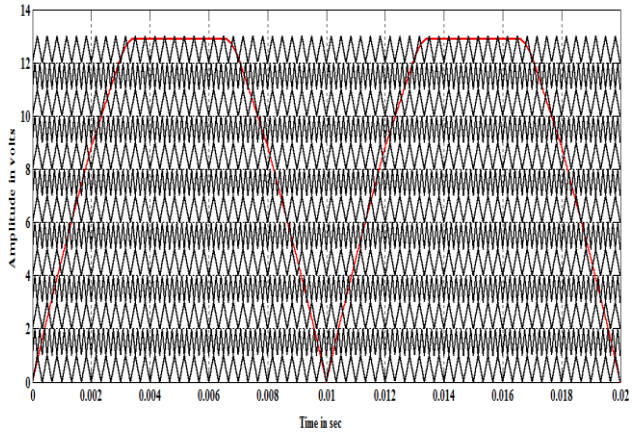


(ii)



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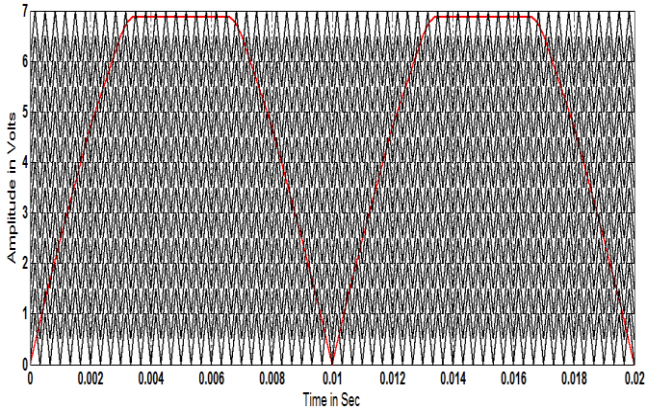


(iv)

Fig. 2 Carrier display :(i) IPD PWM method; (b) APOD PWM method; (iii) VF PWM method;(iv) COP PWM method

Alternative Phase Opposition Disposition PWM plan (APOD)

This plan need every of the thirteen carrier signals for a 27 level inverter to be phase displaced from each other carrier by 180° alternately. Fig.2 (ii) Description the multicarrier agreement for APODPWM plan for ma = 1 and mf = 50.

Carrier Overlapping (COP) PWM Scheme

The Carrier Overlapping PWM scheme, m-1/2 carrier signals are liable such that the carrier bands they engage overlap through each other carrier. The vertical equipoise of carrier wave signal for 27 level inverters with COP PWM design is shown in Fig.2 (iii).

Variable Frequency (VF) PWM Strategy

This category of PWM plan provides odd number of carrier has one value of frequency and even number of carrier has another value of frequency.Variable frequency pulse width modulation method is demonstrated in Fig.2 (iv). In Fig.2 (iv) Appearance of multicarrier conformity for VF PWM method for ma = 1 and mf = 50. Mf1=3000Hz and Mf2=6000Hz.

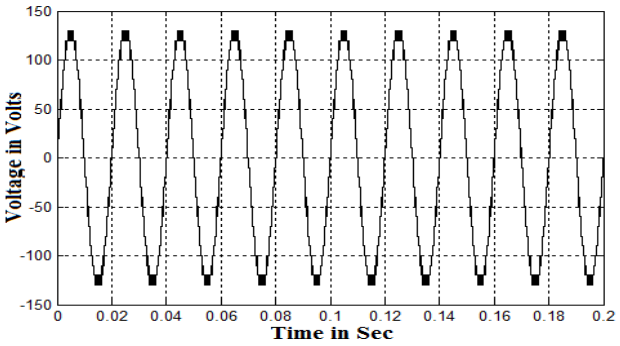
IV. SIMULATION RESULTS

The 27-level one phase asymmetrical cascaded multilevel inverter is established in MATLAB/SIMULINK. The firing signals for cascaded asymmetric multilevel inverter are recognized by using multicarrier sixty degree PWM methods. Simulations result are observed for a range of morals of modulation index ma extending from 0.85-1.Figs.3–6exposed simulated AC output voltage of one phase asymmetrical cascaded multilevel inverter among their correspondent FFT plots displayed for only one example value of modulation index ma = 1 for above said all PWM Methods.

The correspondent percentage THD of an amount of closeness in shape regarding a waveform and itsessential constituent is evaluated by means of FFT block and their mathematical values are registered in Table-III. Table-IV shows the essential V_{RMS} inverter output AC voltage of an amount of input DC bus utilization. Table-V presentation of corresponding Crest Factor worn to recognizes peak current estimation of power semiconductor devices. Table-VI shows the Distortion Factor of AC output voltage of preferred one phase asymmetrical cascaded MLI. Table -VII shows the consequential Form Factor related with power quality trouble. Table-II shows the consideration and its rate of simulation.

Table. 2 Simulation Circuit Parameters

Parameter	Rate
Top H-Bridge (HB1) DC supply: 1V_{DC}	10V
Center H-Bridge (HB2) DC supply: 3VDC	30V
Bottom H-Bridge (HB3) DC supply: 9VDC	90V
Loading Resistance (R_L)	100 ohms
Carrier Frequency (fc)	6000Hz
Modulation frequency mf1	50



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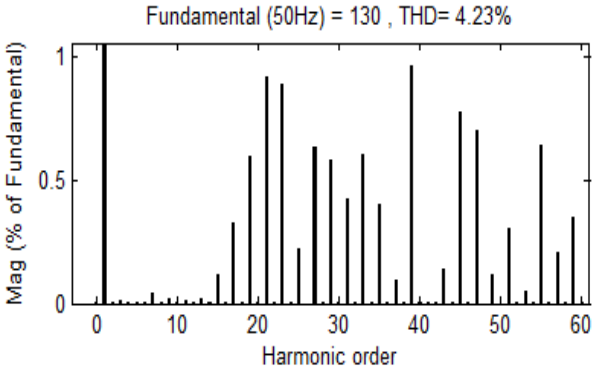
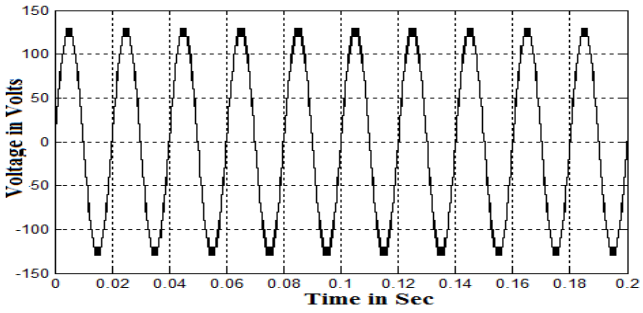


(ii)

Fig. 3 Output AC Voltage and corresponding FFT Plot of IPDPWM plan



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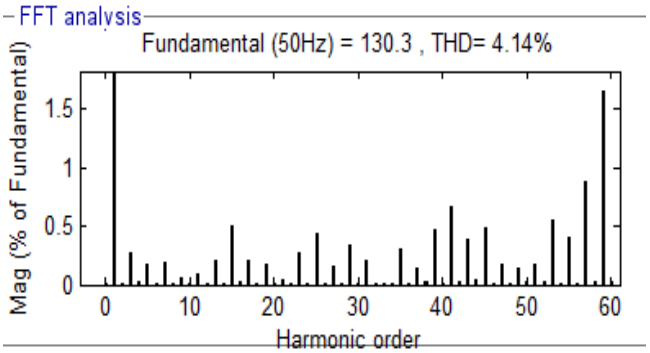

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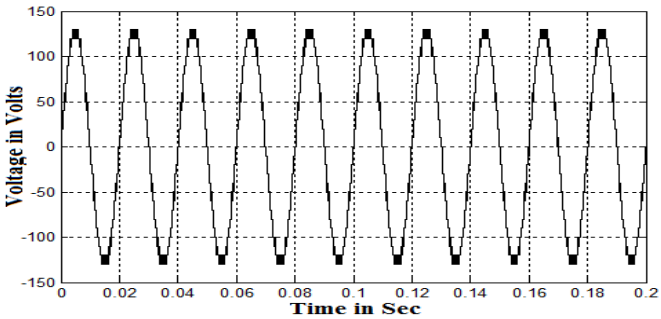
Fig. 4 Output Ac Voltage and corresponding FFT Plot of an APODPWM plan.



(i)

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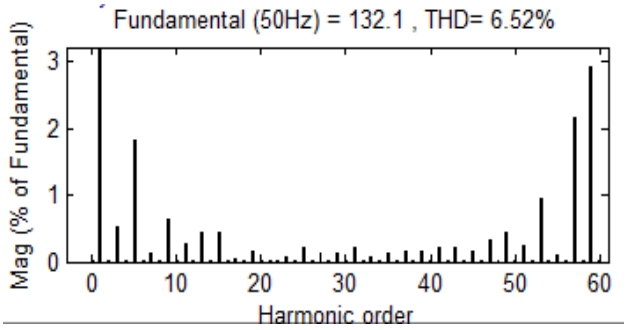
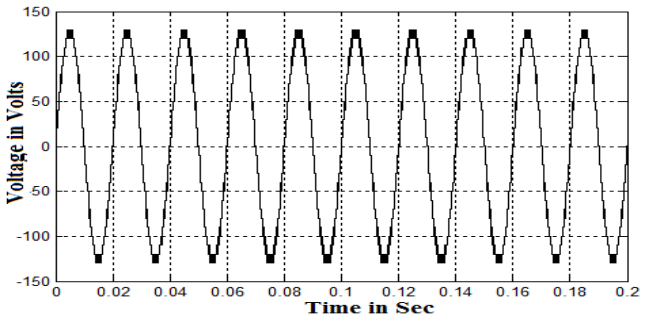


(ii)

Fig. 5 Output Ac Voltage and corresponding FFT Plot of COP PWM plan



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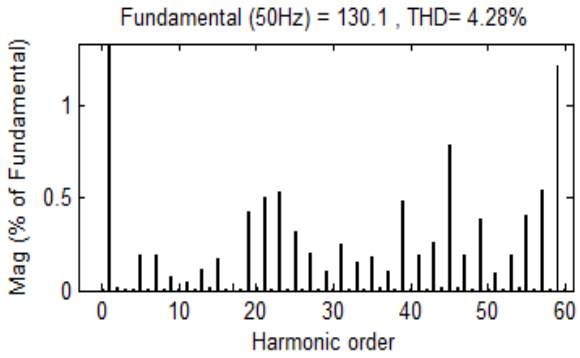

(ii)

Fig. 6 Output Ac Voltage and Corresponding FFT Plot for VF PWM plan

Table. 3 Percentage THD for a variety of modulation indexes

Ma	IPD	APOD	COP	VF
0.85	5.23	4.39	8.12	5.21
0.9	4.97	4.32	7.92	4.92
0.95	5.00	4.57	7.31	4.47
1	4.23	4.14	6.52	4.28

Table. 4 Fundamental V_{RMS} Output Voltage for a variety of modulation indexes

Ma	IPD	APOD	COP	VF
0.85	78.53	78.41	79.95	78.22
0.9	82.37	82.7	84.16	82.67
0.95	87.12	87.43	89.23	87.42
1	92.51	91.39	93.83	92

Table. 5 Crest Factor of a choice of modulation indexes

Ma	IPD	APOD	COP	VF
0.85	1.4146	1.4141	1.4147	1.4146
0.9	1.4142	1.4142	1.4147	1.4143
0.95	1.4149	1.4143	1.4125	1.4140
1	1.4148	1.4147	1.4141	1.4141

Table. 6 Distortion Factor of a choice of modulation indexes

Ma	IPD	APOD	COP	VF
0.85	1.20	2.60	3.01	1.21
0.9	1.03	2.01	3.03	1.04
0.95	1.02	2.03	3.07	1.07
1	1.07	2.06	3.02	1.03

Table. 7 Form Factor for Various modulation indexes

Ma	PD	APOD	COP	VF
0.85	33903.07	1.81E+09	11936.02	11575.1
0.9	35339.6	680.077	17266.08	19051.57
0.95	1.59E+06	3.2710	Inf	40125.78
1	39361.53	Inf	1.64E+09	2.23E+09

V. CONCLUSION

This paper proposes one phase asymmetric cascaded multilevel inverter using a input DC voltage ratio 9: 3: 1 with various pulse width modulation schemes.The per-formance parameter like V_{RMS} voltage, THD, Form Factor, Distortion Factor and Crest Factor compared for a variety of modulation technique ensures that the fundamental AC output voltage in each and every inverter is always bigger than or equivalent to zero. Thus, redevelopment in any individual input power cell is escaped and a lowest Total harmonic distortion (THD) in the consequential pulse width modulationvoltage signal is ensured. This proposed one phase asymmetric cascaded inverter is prolonged by use of AC motor drives and Speed control operation.

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