Design of D Flip-Flops with Pull up Scheme and Clock Gating for Input

Vinayak Misra, Shubham, Sakthivel R

Abstract—the following paper deals with a pulsed triggered flip-flop having a pull up control scheme. The flip-flop used is also incorporated with an embedded clock gating. The topology that has been used are the IPFF-CGPC Implicit Pulse Flip Flop with an embedded clock-gating and pull-up control scheme (IPFF-CGPC) and IPFF-ECGPC is the enhanced CGPC which arehaving XOR based gating clock .The main difference between the former and the latter is that it used a pass transistor based logic XOR for IPFF-CGPC and for latter XOR logic gating is based on the transmission gate. This topologies provide us with both novel approach and power efficiency is considerably high as in comparison to its other contemporary topologies The XOR gating in the pulse generation helps to disable the inverter chain during when the input is unchanged .Both the topologies helps to remove the redundant transistors of the internal node. Similarly the pull-up when transition is from D i.e from 0 to 1 saves the short-circuit power. In this paper further modification is done in the form of dynamic XOR gate used in the clock gating scheme which is further used to improve the performance of the Flip-Flop. The technology that we have used is 45nm feature size which function on a supply voltage of .8V and which further reducedthepowerandalsotheareaoftheFlip-Flop.

Index Terms—Clock gating, XOR GATE, pulse triggered, embedded clock, pulse triggered Flip- Flop,

I. INTRODUCTION

With the advent of the technology the scaling down of the device have become an indispensable part of the semiconductor- tor industry as the primary products such as SoC(System on Chip) and SiP (System in Package).These are quite extensively used in cell phones ,tablets etc. With the large integration of multiple functionality technology on a very limited space which results in an increased chip density and the frequency of the clock have actually revolutionized the VLSI industry from a paradigm shift from a design that used to be working in speed sensitive version to a design which now works on alowpowerdesign.Themaincauseofpowerdissipation.
Identify applicable funding agency here. If none, delete this.in a VLSI architecture are caused by the power dissipated by cock distribution and the power dissipated by thestoring devices (latches or Flip-Flops) .This power dissipation is generally accounted for 30 to 60the system power. The other important point that there is that the 90actually dissipated in the system by the flip- flops. This factor is of utmost importance and makes it considerable to reduce it in theVLSI systems. The switching power is the major part or component in a CMOS total power, the switching power in the CMOS is actuated when the circuit takes a transition from 0 to 1 or 1 to 0. In this what actually happens is that the capacitor charges ordischarges. Theswitchingpowerisgivenby

$$P = ACVdd^2f \qquad (1)$$

The Power is equivalent to the activity factor A (which is how much time the input changes in a clock cycle),the load capacitance(C), the rail to rail voltage (Vdd) and the frequency of the clock (F).The movement of charge per cycle is equivalent to CV whereas the movement of charge per second will be CVF. Then the power dissipated wouldbe CV2F. From the formula above it can be well seen that the power is dependent on Vdd by a factor of 2 .The other way is also by reducing the frequency which is by dual edge FFs which in actual cuts the frequency by half and saves power in clock network distribution .The other method is by using clock gating techniques for more efficiency as the elimination of the triggering which is unnecessary for the clock is also reduced and the redundant transition is also beingreduced. These transitions are actually in the internal nodes and can be easily blocked blocking clock when the input of the Flip-Flop
isunchanged.ThePulseTriggeredFFshaveawideapplicationas well are popular because of low power and very high speed applications.

II. LITERATURE SURVEY AND PREVIOUS WORK

A. implicit pulse-triggerded flip flops with pull up scheme and embeddedclock gating

In this section we will be discussing on the FFs which have a implicit pulse triggering through a embedded clock and with a pull-up scheme .These circuits will be realized with a clock gatingtechniqueoperatedwithaXORlogicconfiguration with a pass transistor logical along with a XOR transmission Gate the first one is the IPFF-CGPC and the second one is theIPFF- ECGPC. The problem of the power and speed is considerably reduced in these topologies. The schematic diagram is shown as IPFF-CGPC and enhanced version of it designated byIPFF- ECGPC[1]. The pulse enhancement scheme is used generally to design a implicit pulse triggered Flip Flop. The pulse generation logic use in the discharge path reduces the power of the circuit as the complexity is reduced and also reduces the size and the number of transistor which are used in the circuit. The method of clock gating is used generally for the reduction the dynamic power dissipation in the

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circuit. This technique is generally used for the synchronous circuits. The method is use by adding more circuit in the clock distribution logic so as to ramify the clock tree. This clock pruning leads to disabling part of the circuit and avoids the switching of certain flip flop and saves power.

B. IPFF-CGPC and IPFF-ECGPC

It generally uses two methods which can improve power efficiency The first is the clock gating which is embedded is implemented using a XOR comparator with a transistors N2 and P0 which are actually in pulse generated in the stage comparator actually applies the inputs D D bar and output Q Q fb which acts as a control signal to produce a signal of gating Y. This suppresses the redundant delay of the clock signal. And saves a large amount of dynamic power. This clock gating scheme separates the Z and node CLK whichultimately increases the skew tolerant capability. The second which is a pull up control scheme that employs the signal Z which is actually generated from pulse generator and also from the control PMOS transistor P1 which in turn , turns 0 for node X , during the evaluation phase of the circuit , which actually leads to glitch free node X. the pseudo NMOS logic which was used earlier is modified by the charged condition, whose size is kept minimum that is P1 The conditional discharge is cancelled from the dynamic latches left side . This shows that when transition from 0 to 1 is there it gives a great power reduction by avoiding the path of short circuit from Vddtothe ground duringsampling[1].

The clock gating for the IPFF-CGPC is done using pass transistor logic .The clock gating has a XOR based logic which generate output only when there is a difference in the input D and the output of Flip-Flop Q. This leads to reduction in power dissipation as the activity factor is reduced for only for transition when there is variation in D and Q.

This logic also reduces the power to delay product also known as PDP as the transistor size is also optimized in an iterative manner.

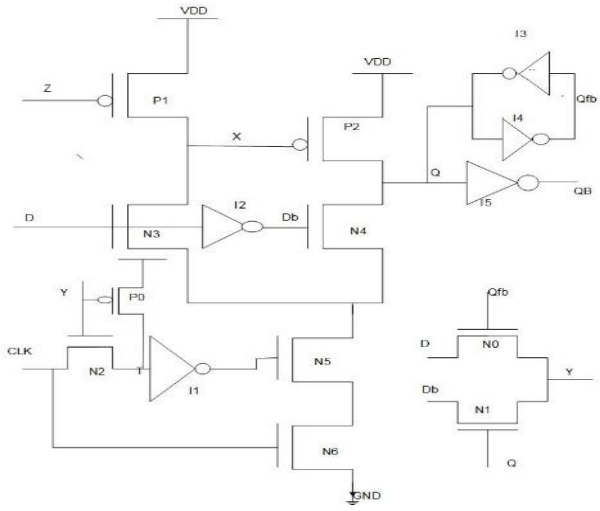
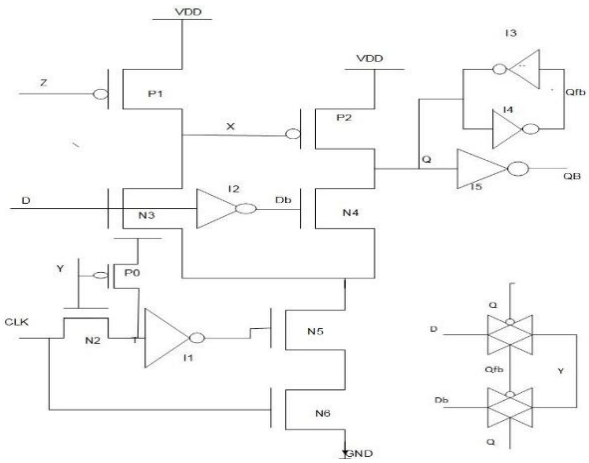


Figure 1.circuit for IPFF_CGPC

The Circuit of IPFF-ECGPC consist of the transmission gate logic at the clock gating circuit instead of a pass transistor logic at the clock gating. The use of the transmission gate logic improves the voltage drop by the pass transistor logic as the strong 1 and strong zero are passed by transmission gate as equal due to its structure whereas the pass transistor has some voltage drop when passing both 1 and 0 .The use of transmission gate as the gating logic further reduces the power dissipation of the circuit



C. Figure 2 .circuit for IPFF-ECGPC

D. WORKING

When values of the D and Q are not same, the comparator XOR generates a signal 1, which switches off to P0 and turns ontheN2nodeofthecircuit.Attherisingedgeoftheclock, theclkandnodeZisgoingtobehighforashortperiodof time . the results of it is actually turns on the clocking branch N6 and N5 hence resulting in the evaluation phase of the FF. after delay of one inverter cycle the node Z is going to be 0 which then shuts down to the discharged clocking branch . In that period if D transits from 0 to 1 then the internal node of the circuit X transits from 1 to 0 through the node N3 and along the clock branch with this Q becomes to 1 by P2, parallel when the node Z is high , the pull up transistor P1 is going to be shut down for some short time of period . It results in the shortening of data path propagation time and drastically decreases the short circuit power Similarly if D has to make a transition from 1 to 0 it results in the pull down of the Q to 0 via the clock branch and N4 but if the D stage of the circuit is unchained, The XOR based comparator will send a 0 which shuts down the N2 and turns on the P0, which eventually leads to charge node T and node Z will be pull to 0 which ultimately turns off the N5 . It can be seen as discharging clock is shut down and internal node X will be kept unchained The only problem which arises in this is the variation of tolerance for N0 and N2 . The transition power in node N2 and Y can be reduced due to the low voltage but it will give more leakage power hence to improve this performance and capability ofthe design, we are giving a enhance version to this structure of IPFF-CGPC by changing the Pass transistor logic XOR based comparator with a transmission gate which eventually over comes the problem of maintaining the full voltage swing in the clock generation stage and

the problem of threshold . If we consider that D is not changed then the delayed clock signal is going to be blocked and it finally shuts down the branches of clocks results in a no redundant transition at the node X, because X is high .

We can see that both designs have solved the problem of the short circuit path of the X node during the evaluation period but it actually solves the problem of no glitch on the output node when input transits from 0 to 1 .This shows that IPFF-CGPC and IPFF-ECGPC as a very better low power efficient circuits when the data has very transition activity and also solves the issue of race around.

III. PROPOSED LOGICDESIGN

In our design , we have divided it into two major parts :

a) Clock gating structure

b) Advanced D Flip- Flop structure

A. Clock Gating Structure

Here we have considered the XOR comparator based clock gating with the help of a dynamic XOR logic comparator. The logic consists of a novel approach for the XOR comparator[4] .The clock gating circuit uses a pass transistor logic concept .The inverter used in this case are used to provide a rail to rail voltage swing as the Mosfet 4 is connected to Vdd , whereas 3 and 5 is connected to the ground . The logic produces XOR as well as XNOR outputs but only the logic XOR is used as the input for the next Flip-Flop stage . The inputs of the mosfet 1 and 2 is provided as the D and Q . As for the XOR logic output will only be provided when there is a difference in both the input.

B. Advanced D Flip- Flop structure

The figure given in (4) shows the modified d flip-flop. The modified d flip flop is created using pass transistor logic , inverter[2]. It helps in the reduction in the number of transistor use and provide a better voltage swing at the output node with less glitch at the output node. This circuit has a better power rating for consumption and dissipation as in comparison to the conventional Flip-Flops.

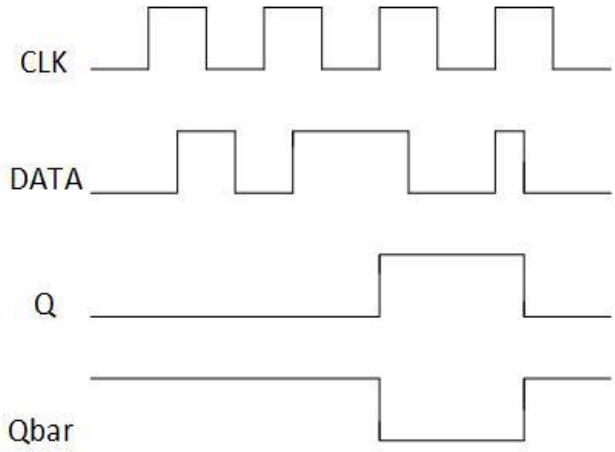


Figure 3.Output for D Flip-Flop

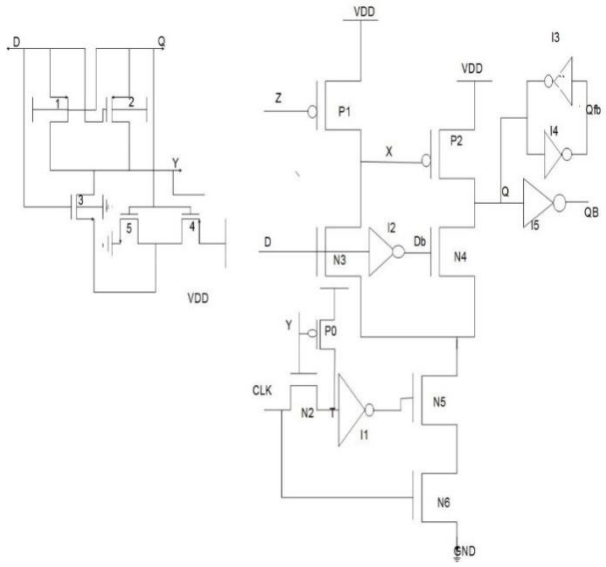


Figure 4.Circuit for proposed logic

IV. ANALYSIS AND RESULTS

The circuit is constructed at 45nm Technology node with a power supply of 1.2V .The analysis for the same is done for the power dissipation, rise delay transition and fall delay transition.

A. POWER DISSIPATION

The power dissipation for the different design is calculated by taking the average power and the peak power for the voltage and current. The comparative analysis is depicted in table 1

Table 1.Average power and Maximum power table

TOPOLOGY	DELAY	POWER	MAX.POWER
1.IPFF-CGPC	5.58nS	2.83 uW	227.831 uW
2.IPFF-ECGPC	4.53 ns	683 uW	457.97 uW
3.PROPOSED CIRCUIT	55.26 pS	17.3 uW	417.8 uW

B. RISE TRANSITION (0 to 1)

The data is checked in comparison to the clock pulse .When the data is moving from 0 to 1 or from low to high value w.r.t the clock pulse. This value is used for the proper timing characterization of the logic design as for setup and hold violations are calculated by this parameter.The rise delay for all the design are depicted in the following table 2

Table 2.Rise Transition Table

TOPOLOGY	D	Q	Qbar	Clk
1.IPFF-CGPC	0.21 ns	0.4ns	0.501ns	0.45 ns
2.IPFF-ECGPC	0.23ns	0.55 ns	0.13 ns	0.25 ns
3.PROPOSED CIRCUIT	0.08ns	0.15 ns	0.17 ns	0.5 ns

C. FALL TRANSITION (1 to 0)

The data is checked in comparison to the clock pulse .When the data is moving from 1 to 0 or from high to low value w.r.t the clock pulse. This value is used for the proper timing characterization of the logic design as for setup and hold violations are calculated by this parameter.The fall delay for all the design are depicted in the following table 3

Table 3.Fall Transition table

TOPOLOGY	D	Q	Qbar	clk
1.IPFF-CGPC	0.18 ns	0.09 ns	0.7ns	0.24ns
2.IPFF-ECGPC	0.19 ns	0.11 ns	0.07 ns	0.05ns
3.PROPOSED CIRCUIT	0.5ns	0.11 ns	0.73 ns	0.073 ns

V. CONCLUSION

HerewehavepresentedaNovelLowpowerFlip-Flops. The proposed IPFF CGPC and the IPFF-EGPC and the proposed model reduces the power and increases theefficiency of the Flip-flops. These topology overcome the problem of redundant transition in the internal nodes and reduces the overall total power in addition to that the pull up control scheme applies to the discharging path of the dynamic latch, which in results save the short circuit power . When the transition is from 0 to 1. We can also see that clock gating in allthethreemodelsprovidesaverynovelpowerandareafor thedecreasedelayperformance. Italsoshowsrobusttolerance forskewvariationorfullswingoperations.

The design based on the 45 nm technology , the results suggests that the propsed design exhibits outstanding power efficiency and power characterization and switching activity up to 10% of there counter rival designs and also an improvement for the CLK to Q delay for the D , which leads to an improvement in the setup and hold for the proposed design.

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