Implementation of BPSK, DSSS and DQPSK Modulators and their Performance Comparison in VHDL

Prof. P. Subba Rao, N. Durga Naga Lakshmi, V. Geetanjali

Abstract: ***Implementation of digital modulators is playing an important role in various fields in recent years. The design of BPSK modulator is presented using Direct Digital Synthesizer (DDS) with the aid of LUTs and Accumulators. For security enhancement and capacity improvement, Direct Sequence Spread Spectrum (DSSS) modulator is designed using a PN sequence generator and a simple BPSK Modulator. To overcome the problem of generating the coherent carrier at receiving end, the digital information is encoded as the phase change instead of absolute phase using a Differential QPSK Modulator. The performance of these three modulation techniques is compared in terms of area and power. The entire design is done in XILINX ISE 14.5 software using VHDL. The device used is VIRTEX4 starter kit.***

Index Terms: Binary Phase Shift Keying, Direct Digital Synthesizer (DDS), DQPSK, DSSS, PN sequence generator, VHDL.

I. INTRODUCTION

In the last few years, implementation of digital modulators on FPGAs has experienced numerous research contributions, but there is still significant work that needs to be done. Previously, work has focused on the implementation of simple digital modulators such as ASK, FSK, and PSK. Using Xilinx System Generator, Quadri and Tate presented a review of the main research papers in this area with some implementation examples [1]. Some of this research will be summarized here.A research work related to the implementation of BPSK modulator and demodulator on a SPARTAN-3 FPGA is done by Bhore and Sarde in 2014 [2]. Analog modulators have also been implemented on a variety of FPGA based implementation boards in addition to the digital modulators. Optimum solution in terms of efficiency, power consumption and resource utilization are also reached by some of these researches. Here, an innovative method of implementing BPSK modulator on FPGA using accumulators and LUTs is conferred. Direct Sequence Spread Spectrum is a modulation technique in which multiple signals occupy same frequency band, which are distinguished by using different spread codes. Digital Cellular telephone systems and personal communication systems utilize this type of communication. For all uplinks from mobile station to base station one frequency band is used and for all downlinks from base station to mobile station another frequency band is used[3]. In this paper, the design of DSSS transmitter is done using VHDL software. A VHDL design starts with describing interface of the design which is defined by the ENTITY block. To describe the internal operation of the design ARCHITECTURE block is used [4].

In any digital modulation technique, digital information is encoded as an absolute phase. But the problem in encoding the data with an absolute phase is carrier will not be recovered at the receiver end. So there comes the necessity for opting Differential modulation techniques where digital information is encoded as a phase change rather than absolute phase. DQPSK is an important modulation technique which provides many features such as strong anti-jamming ability and better spectrum utilization [5]. It is commonly used in cellular radio systems, such as LMDS. Here, the design of Differential QPSK modulator is also illustrated.The next section of this paper presents the design of BPSK modulator. The following section illustrates DSSS transmitter design using a simple BPSK modulator and a PN sequence generator. The latter section includes the design of DQPSK modulator followed by the implementation results of these three modulation techniques and their performance comparison.

II. BPSK MODULATOR

The simplest form of PSK modulation is BPSK. Two signals with a phase shift of 180-degree are used to generate its symbol. The constellation diagram of BPSK is shown in Fig.1. The mathematical equivalent of BPSK modulator is [6]:

$$S_n(t) = \sqrt{\frac{2E_s}{T_s}}\cos(2\pi f_c t + (1-n)\pi) \quad n=0,1 \ (1)$$

Where E_s is the energy per symbol, T_s is the symbol duration, and f_c is the carrier frequency. Two signals are generated based on the value of n. They are:

$$S_0(t) = -\sqrt{\frac{2E_s}{T_s}}\cos(2\pi f_c t) \quad \text{when n=0} \quad (2)$$

$$S_1(t) = \sqrt{\frac{2E_s}{T_s}}\cos(2\pi f_c t) \quad \text{when n=1} \quad (3)$$

In order to implement BPSK modulator in VHDL, two sinusoidal waveforms have to be generated. DDS technique was used for this purpose.

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In this method, a 24-bit accumulator which works on the rising edge of the clock and a LUT were used for sine wave generation. The 8 MSB bits of accumulator represent address to select particular amplitude of the sinusoidal signal from LUT. Corresponding to 8-bit width, the LUT has to have 256 sample values which cover one cycle of the sinusoidal signal. Only one signal is obtained by the accumulator and LUT. The other signal which is out of phase by 180-degree has to be obtained for a BPSK modulator. One possible solution is to multiply the first signal by -1 which gives a phase shift of 180 degrees. But in VHDL, due to high resource consumption, it is better to avoid multiplication. Another possible way is to reverse the MSB bit in the accumulator. This technique is explained in detail with a simple example. The accumulator starts with eight MSB bits from "00000000" to "11111111". The address "00000000" represents the first address with zero degree phase shift and "11111111"represents the 256th address with 360 degree phase shift. So, Corresponding to a phase shift of 180 degrees the address used to represent is "10000000". The only difference between the addresses of zero degree and 180-degree phase shift is MSB bit. To obtain 180-degree phase shift, it is sufficient if we reverse the MSB in the accumulator. This reversing operation is performed by logic gate EX-OR. The output BPSK signal is generated by giving two out of phase sinusoidal signals as inputs to the multiplexer as shown in the Fig 2.

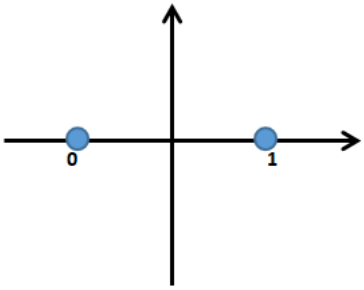

Fig. 1:Constellation diagram for BPSK modulator

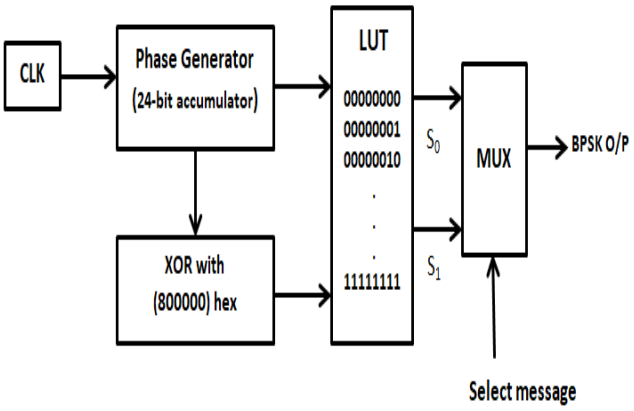

Fig. 2: BPSK modulator using DDS

III. DSSS MODULATOR

In DSSS transmitter data spread is done by using a PN sequence generator and this spread sequence is modulated using BPSK modulator where the carrier is generated by Digital Frequency Synthesizer principle. These modulated signals from different users are the combined and transmitted [7]. The basic building blocks of DSSS transmitter are flip-flops, shift registers, PN coder, Clock synchronizer, Parallel to Serial Converter and BPSK modulator as shown in Fig 3.

PN code generator: The PN code generator uses HASH function to assign codes which are unique to individual users. A HASH function is a mathematical function which converts a large variable sized amount of data into small datum.

Clock Synchronizer: A Clock Synchronizer is used to maintain the synchronization between the transmitted PN sequence and received PN sequence.

Parallel to Serial Converter: A Parallel to Serial Converter is used to convert incoming parallel byte sized data to single bit serial data. It includes a shift register in which several bytes of data are stored simultaneously and thereafter serially transmitted.

BPSK Modulator: A BPSK modulator uses two phases 0^o and 180^o . This modulation is robust of all PSK techniques since it is not much affected by noise, but it is able to modulate at 1bit/symbol. So this is unsuitable for high data rate applications when band width is limited.

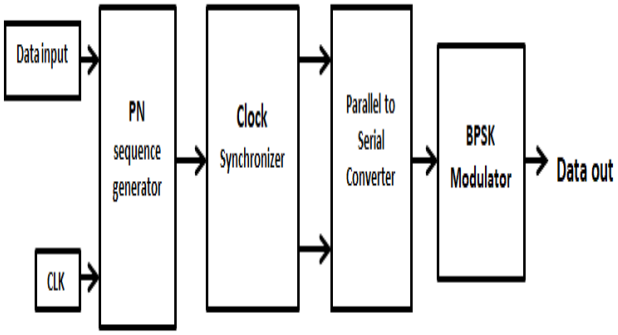

Fig. 3: Block Diagram of DSSS Transmitter

IV. DQPSK MODULATOR

DQPSK is an important digital modulation technique where differential encoding is used. It can overcome the problem of fuzziness in phase of the carrier in QPSK by making use of relative phase instead of absolute phase [8,9].

DQPSK can be implemented in two ways. One method is selection of phase by logic and the other one is by Quadrature modulation. The first method, Phase selection by logic is used here to achieve DQPSK modulation. The basic building blocks used in this method are S/P Conversion Circuit, Differential code, Four phase carrier generator, DDS as shown in fig 4.

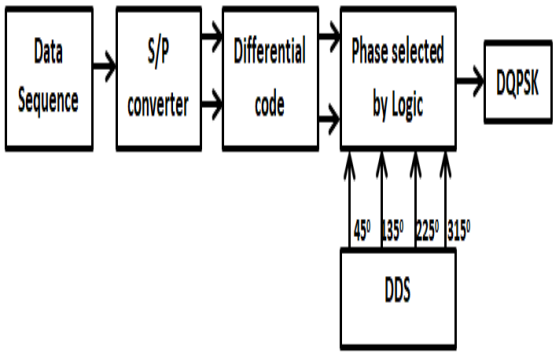

Fig. 4: DQPSK Modulator Block Diagram

Serial to Parallel Circuit:

In S/P Converter, the input bit sequence is separated into odd (I-Channel) and even (Q-channel) bit sequences.

Differential coder:

In differential encoder, the conversion of absolute code to relative code is done. It allows data transmitted to depend not only on current state, but also on previous state.

$$y_{i-1} \oplus x_i = y_i$$

Four Phase Carrier Generator:

In Four Phase Carrier Generator, a DDS is used to generate a waveform. A DDS works by storing points of wave form in digital format and then recalling them for the generation of waveform. It uses Phase Accumulator and LUT as shown in Fig. 5.

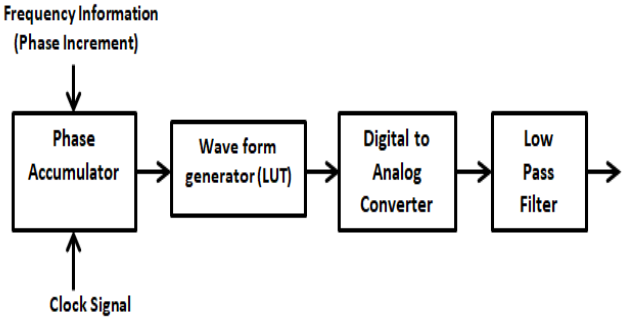

Fig. 5: Block Diagram of DDS

In Phase Accumulator, the digital number which represents phase is stored and the number is increased regularly at various instants of time. Its operation is similar to a counter where present value gets added to the previous value.

After determining phase using a Phase Accumulator, next step is to convert the information into the waveform. This can be achieved using a LUT which consists of a waveform map where each phase value of the wave form is stored. These stored values are converted into analog waveform using a DAC.

V. IMPLEMENTATION RESULTS

ISim is a tool used to visualize the output signals and XILINX ISE is the software used for implementing different modulation techniques in VHDL.

For DDS based BPSK modulator, a 16-bit signal is applied as input and output results are observed with respect to the applied clock.

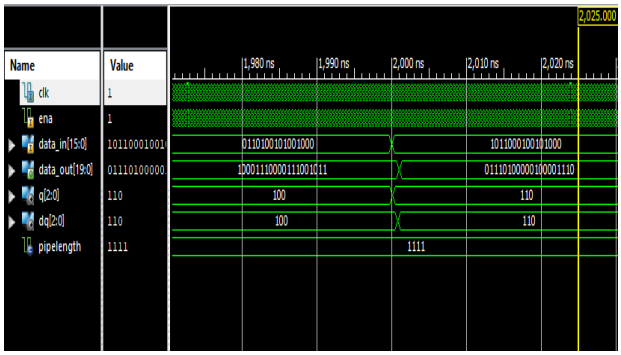

Fig. 6: Implementation Results for BPSK Modulator

In case of DSSS Modulator, an input signal is given and different outputs are observed corresponding to different spread sequences which are generated by means of a PN sequence generator.

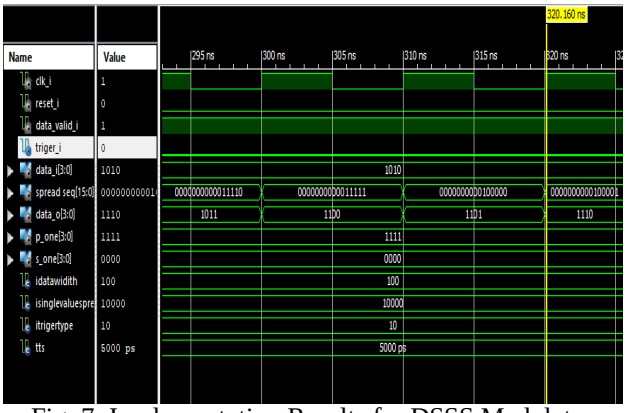

Fig. 7: Implementation Results for DSSS Modulator

For implementation of DQPSK modulator, a di-bit input sequence is applied as input and corresponding to the given input a 16-bit output is obtained.

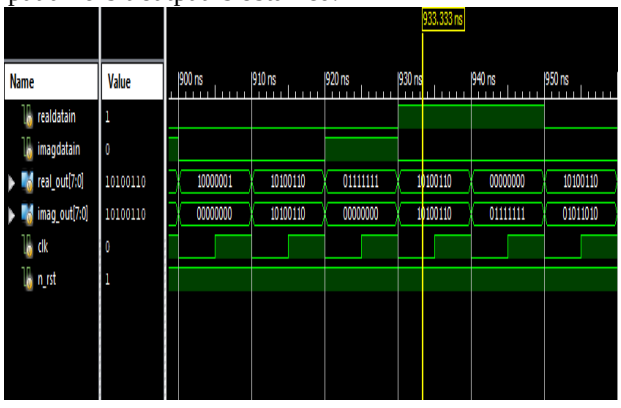

Fig. 8: Implementation Results for DQPSK Modulator

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VI. PERFORMANCE COMPARISON

The project was designed in Xilinx ISE design suite 1using VHDL. The device used was Virtex4 starter kit. The three modulation techniques proposed here are analyzed in terms of performance. The area reports are obtained in the design summary and power analysis is done using power analyzer generated by ISE Design Suite. The performance comparison of DDS based BPSK, DSSS and DQPSK modulators are summarized in table I.

A. Area Analysis:

For all the three implementations of BPSK, DSSS and DQPSK Modulation techniques, area utilization is estimated in Design Summary.

In DDS based BPSK Modulator, IOB utilization is found to be 31% and is reduced to 11% in DSSS Modulator which is further reduced to 7% in DQPSK.

B. Power Analysis:

The Power Analysis is done in Xilinx using Power Analyzer.

For all the three modulation techniques, the power consumed is about 0.081w which is reduced to a greater extent when compared to other conventional modulation techniques whose power is more than 0.083w.

Table I: Performance Comparison of BPSK, DSSS and DQPSK modulators.

IMPLEMENTATION	AREA	POWER
DDS based BPSK modulator	31%	0.081w
DSSS Modulator	11%	0.081w
DQPSK Modulator	7%	0.081w

VII. CONCLUSION

Digital Modulation Schemes provide high capacity to handle large amount of information and improved quality communication than Analog Modulation Schemes. In daily communication, different digital modulation techniques are used for different applications.

The project includes introduction of a direct method where the three modulation techniques are programmed in VHDL.

Using various methods and tools discussed in paper, all efficient and reliable communication systems can be employed for educational as well as research purpose.

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