A Novel Methodology for Single Phase Transformerless Inverter with Leakage Current Elimination for PV Systems Application

Injam Harshith, Bathula Prudhvi Raj, G G Raja Sekhar, T Vijay Muni

Abstract: ***This paper proposes the transformerless photovoltaic (PV) inverter topology to reduce leakage current Multilevel inverters are a source of high power, often used in industrial applications and can use either sine or modified sine waves. The topology has the advantages of simple structure, low weight and provides higher efficiency. However, the topology makes a path for leakage current to flow through parasitic capacitance formed between the photovoltaic (PV) module and the ground. A modulation technique has significant impact to reduce the leakage current without adding any extra component. This project proposes a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic (PV) systems. The proposed hybrid multicarrier pulse width modulation technique ensures low leakage current in the transformerless photovoltaic seven level inverter systems with simplicity in implementation of the modulation technique using lesser number of carriers .***

Index Terms**: *Cascaded H-bridge multilevel inverter, hybrid multicarrier pulse width modulation (H-MCPWM), leakage current reduction, transformerless photovoltaic (PV) system.***

I. INTRODUCTION

The combination electricity age from the photovoltaic (PV) gadget is relatively little when contrasted with other ordinary strength belongings because of its excessive institution cost. Decreasing the PV framework cost and increasing its productivity have done greater noteworthy research intrigue. One of the answers for reduce the cost of the PV manipulate framework is to expel transformer required in the yield of the PV inverter [1]. Most of the national energy administrative expert made it vital to make use of trans-previous over positive side manipulate in the framework due to the fact it ensures galvanic separation. In any case, the utilization of change much less builds weight, size, and fee of the PV framework and radices the electricity transformation proficiency. This has persuaded the examination group to work in the transformer much less PV framework. The headway of strength hardware innovation has made the utilization of transformer less PV inverter general in kilo watt (kW) run by means of forcing models, for example, DIN VDE 0126-1-1 [4]. The basic multicarrier adjustment techniques utilized as a section of the transformer less fell H-connect multilevel PV inverter topologies present fundamental mode voltage. This letter proposes a 1/2 breed multicarrier beat width stability (H-MCPWM) strategy to decrease spillage contemporary in transformer much less fell H-connect multilevel inverter for PV frameworks. At the point when the ordinary mode voltage adjustments in an expansive improve esteem, it prompts high spillage modern-day in the PV framework through the parasitic capacitance between the PV module and the ground. The decreased voltage development in the everyday mode voltage diminishes the spillage current . It is some thing but tough to actualize the proposed tweak procedure besides an awful lot intricacy and require a giant component of the extent of transporters as required in the usual MCPWM strategies.

II. CASCADED MULTILEVEL INVERTER AND HYBRID MULTI CARRIER MODULATION SCHEME FOR CONSTANT COMMON MODE VOLTAGE

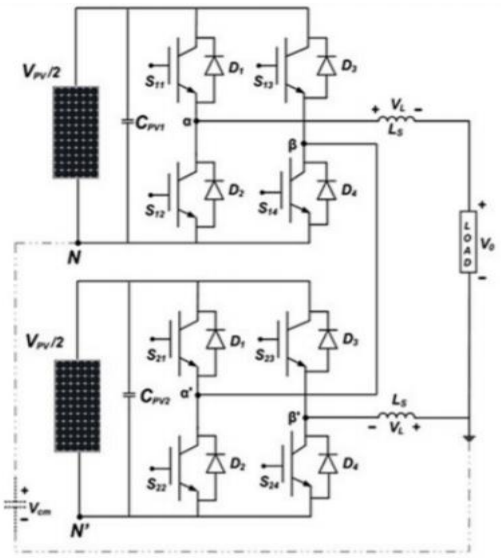

Fig. 1. PV-supported transformer less single-phase five-level cascaded multi-level inverter

Fig. 1 demonstrates the PV-bolstered single-stage five-level fell H-connect inverter topology, where Two H Bridges are associated in course and gives a ordinary yield.

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The arrangement of two fell H-spans consists of the yield voltage of the upper and decrease extensions to produce five-level ventured yield voltage at the air conditioner side, i.e., VP V , VP V/2, 0, −VP V/2, and −VP V . It is typical that the lattice does no longer contribute everyday mode voltage in the framework [9]. The converter topology and law method have big commitment in spillage modern age. Subsequently, the transformer much less fell multilevel inverter regarded in Fig. 1 is associated with a primary resistive load for Evaluation of the proposed tweak method. The spillage contemporary is created in the parasitic capacitance framed between the PV module and the ground, the place fundamental mode voltage is likewise actuated at an indistinguishable point from appeared in Fig. 1. The normal mode voltage of any electrical circuit is the imply estimation of voltage between the yields and a typical reference point. The terrible terminal of the dc transport, i.e., terminal N is referred to as here as everyday reference point for upper H-connect inverter. Thus, for deliver down H-connect inverter, N_ is the regular reference point. The parasitic capacitance shaped for the decrease H-extension and higher H-connect is thinking to be the same, be-cause each the H-spans are provided from the comparative appraised PV modules [11]. The everyday mode voltage (CMV) and spillage present day in the two H-spans are likewise same; consequently, the capacitive streams spill out of guide N toward floor and N_ to floor is seen as equivalent. The common mode voltage Vcm for the top full-bridge (H-bridge) inverter is defined as follows [3]:

$$\frac{V_{\alpha N} + V_{\beta N}}{2} \quad (1)$$

$$V_{cm} + V_{\alpha N} - V_L - V_O = 0$$

$$V_{cm} + V_{\beta N} + V_L - V_{\alpha\_\beta\_} = 0. \quad (2)$$

The yield voltage Vo has little have an effect on on parasitic capacitance and for that reason it is disregarded. It is universal that the channel inductance Lsis regarded the identical in the two H-spans for simplicity of the investigation and consequently the voltage drop VL because of the inductance Ls in the Two H Bridges is likewise expected equivalent [3]. The assertion of the regular mode voltage can be gotten in (4) by such as (2) and (3) as takes after:

$$2V_{cm} + V_{\beta N} + V_{\alpha N} - V_{\alpha\_\beta\_} = 0. \quad (4)$$

$$V_{cm} = \frac{V_{\alpha\_\beta\_} - V_{\alpha N} - V_{\beta N}}{2}. \quad (5)$$

Presently considering tradition that the spillage contemporary will spill out of PV module to floor or the other way around in accordance to the standards IEEE 80 [22], the indication of everyday mode voltage can be became around as Vcm _ = −Vcm and shortened now beforehand as CMV in this paper. Condition (5) is valuable for determining the basic mode voltage in exclusive interims of the reference time frame. To restrict the spillage present day direction through the parasitic capacitance, the everyday mode voltage is required to be stored up least amid the changing occasions . The base strengthen estimation of the regular mode voltage is characterised via VP V/(n− 1) in the MCPWM process [18]. In stage demeanor multicarrier beat width law (PD-MCPWM), the primary mode Vcm _ fluctuates in the band scope of ±VP V/2. Be that as it may, in this adjustment technique, add up to (n−1) wide variety of transporter alerts are utilized, where n is the inverter level.

TABLE I
SWITCHING INSTANTS OF THE H-MCPWM TECHNIQUE FOR CONSTANT COMMON MODE VOLTAGE

Logic conditions	*Switches on upper H-bridge*				*Switches on lower H-bridge*				*Common mode voltage*
Mode-1: (0 to T/2)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	V^{+}_{cm}
$V_{c1} > V_{ref} < V_{c2}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c1} > V_{ref} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{PV}/4$
$V_{c1} < V_{ref} > V_{c2}$	0	0	1	1	0	0	1	1	$2V_{PV}/4$
Mode-2: (T/2 to T)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	–
$V_{c2} > V_{ref} < V_{c1}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c2} > V_{ref} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{PV}/4$
$V_{c2} < V_{ref} > V_{c1}$	1	1	0	0	1	1	0	0	0

The proposed H-MCPWM is the modified model concerning the phase contrary characteristic (POD) twig cover modulation technique, the area the large range of carriers required is incompletely on that required among POD PWM and therefore computational encumbrance is reduced. In that modulation method, the provider indicators ancient are in-phase together with each and every other. The area involving complete the service is shifted thru 180° after every half-cycle. Table I indicates the extraordinary switching instants but theirs corresponding magnitude about CMV. It has vii switching instants, in which certain on the spot has naught CMV, three instants endure 2VP V/4, and then two instants have VP V/4, CMV . There is no voltage trade of kingdom in duck CMV. The CMV may additionally take the values depending above the inverter alternate states desire on the grounds that the voltage supply inverter cannot furnish honest sinusoidal volt-ages and has by using yield voltage degrees synthesized out of the yield voltage over the PV [10], [15-17]. The voltage transit relies upon over the route involving the modern-day of the inverter; hence, the proposed H-MCPWM modulation technique ensures the reduced customary anger voltage generation of the puttee electricity on most ±VP V /4. The switching sample over the proposed H-MCPWM approach because of five-level cascaded multilevel inverter is illustrated among Fig. 2. The operation about the proposed H-MCPWM is broken within twins' modes about operation, i.e., mode-1 and mode-2, so described next .

Mode-1 (0 to T/2)

In that mode, complete the carrier alerts are in-phase with every other, the three-level voltages, i.e., 0, −VP V/2, then −VP V , are generated the use of comparable switching scheme: 1) When the reference sign Vref is smaller than the provider alerts Vc1 but Vc2 , afterwards the switches S11 , S14 , S23 , then S22 are grew to grow to be ON or the complimentary switches, S13, S12, S21, and S24, are turned OFF. In this state of affairs Vα N= VP V/2, VβN= 0, or the output voltage is Vα β=+VP V/2. 2) When the allusion signal Vref is larger the carrier sign Vc2,

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or lesser than the carrier signal Vc1, in a while the switches S14, S12, S23, or S22 are grew to become ON then the complimentary switches S11, S13, S21, then S24 are grew to come to be OFF. In this VαN = 0, VβN = 0, but the output voltage is Vαβ = zero

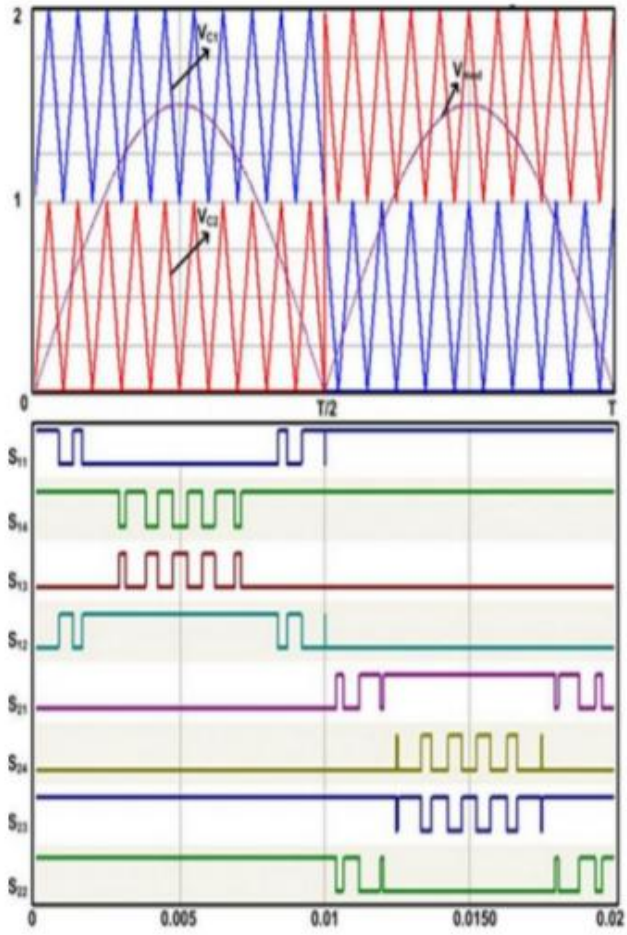

Fig. 2. Switching pattern of the proposed H-MCPWM technique for the five level cascaded multilevel inverter

3) When each the service signals, Vc1 then Vc2, are smaller than the reference signal Vref, after the switches, S13 , S12, S23, or S22, are turned ON and the complimentary switches , S11 , S14 , S21 , yet S24 , are grew to become OFF. In its situation Vα N = 0, Vβ N=VP V/2, or the output voltage is Vα β = −VP V/2.

MODE II

In that mode, total the provider symptoms are segment shifted by 180°, the three-level voltages, i.e., 0, +VP V/2, and +VP V, are generated the usage of consonant switching scheme. 1) When the be aware sign Vref is smaller than the provider signals Vc1 or Vc2, after the switches, S11, S14, S23, or S22, are grew to turn out to be ON but the complimentary switches, S13, S12, S21, or S24, are became OFF. In this situation VαN= 0, VβN= +VP V /2, yet the outturn voltage is Vαβ= −VP V /2. When the point out signal Vref is large the carrier indicators Vc1, or lesser than the carrier sign Vc2, beneath the switches, S11, S14, S21, but S23, are grew to become ON then the complimentary switches, S13, S12, S22, then S24, are turned OFF. In it state of affairs VαN= +VP V/2, VβN= +VP V/2, yet the outturn voltage is Vαβ= zero 3) When both the service signals, Vc1 and Vc2, are smaller than the reference signal Vref , later on the switches, S11, S14, S21, but S24, are grew to become ON and the complimentary switches, S13, S12, S23, then S22, are grew to become OFF. In its situation VαN = VP V/2, VβN = 0, and the output voltage is Vαβ = +VP V/2.

The summary regarding the switching instants devoted between two modes concerning feature is introduced in Table I. It is absolutely seen from the previous discussion that the proposed H-MCPWM technique is capable in conformity with reason five degree inverter yield voltage then collect diminished common paint voltage of the bandage on maxi-mum ±VP V/4, as is really helpful in conformity with the conventional MCPWM technique

III. MATLAB/SIMULATION RESULTS

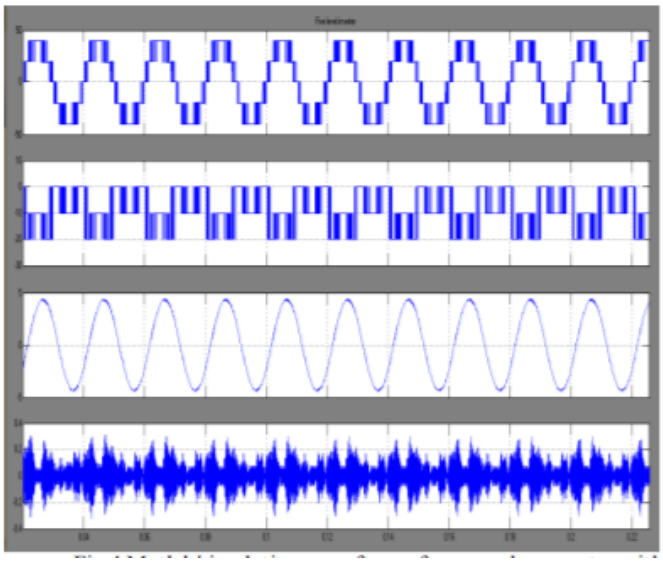

Fig 4 Wave form of proposed converter with in-phase deposition

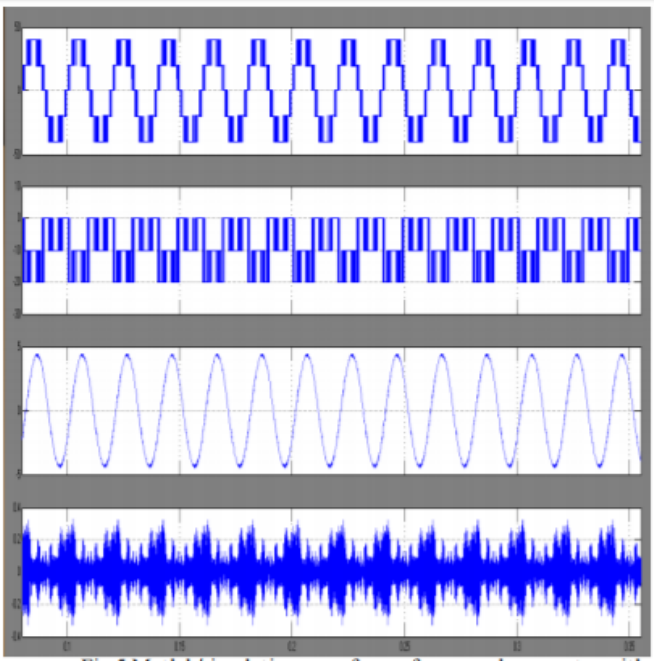

Fig 5 Wave form of proposed converter with out -phase deposition

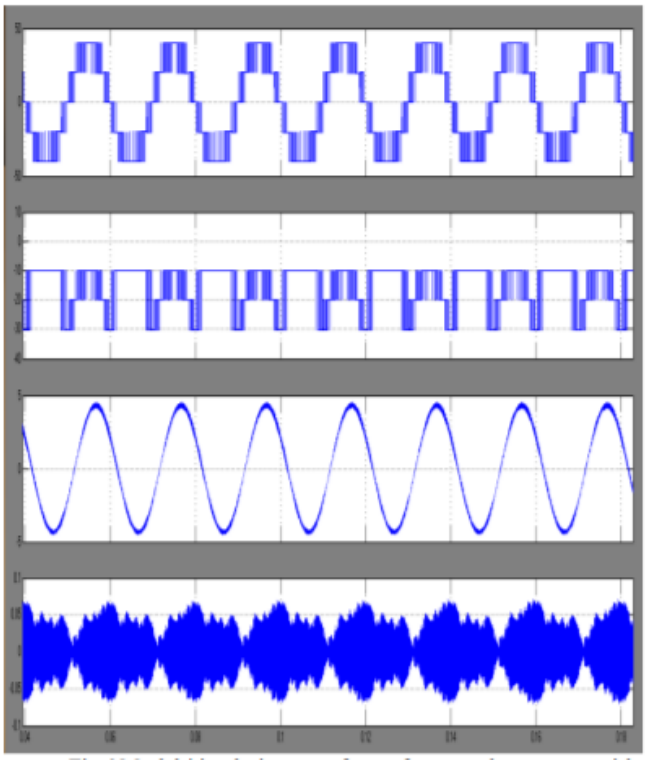

Fig 6 Wave form of proposed converter with multi carrier deposition

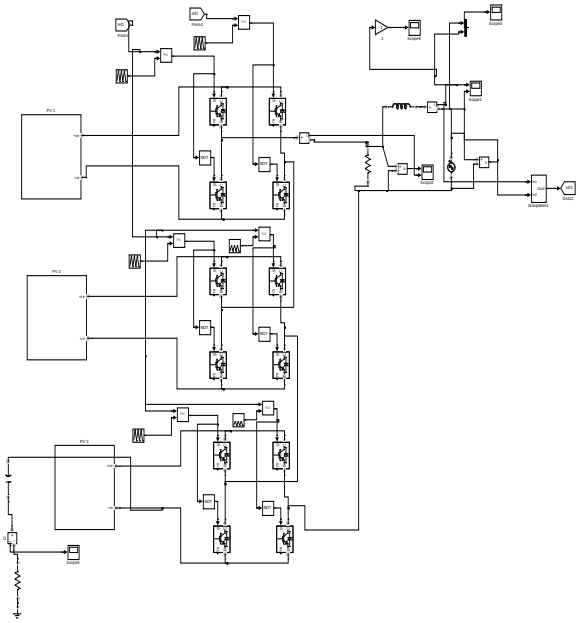

Fig 7 Model of proposed Seven Level Converter

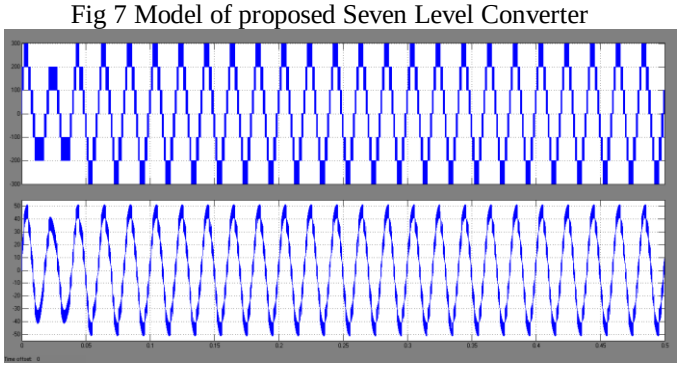

Fig.8 Output Waveforms of H-MCPWM seven level inverter

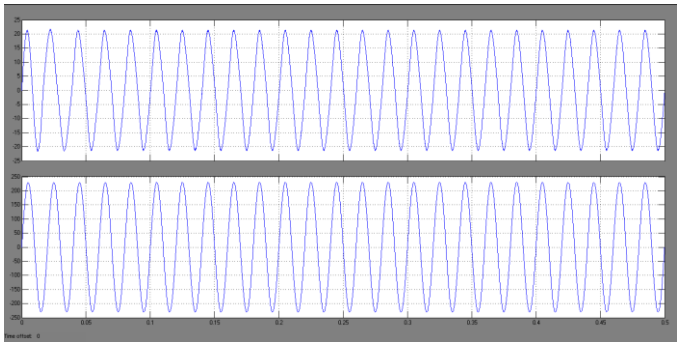

Fig.9 Output Waveforms of H-MCPWM seven level inverter when it is connected to grid

IV. CONCLUSION

In this paper proposes H-MCPWM method employed between transformer a good deal less cascaded multilevel inverter for the PV systems. The proposed modulation method attains reduced general ardour voltage collectively with simplicity of implementation about the modulation technique. It has been illustrated as the proposed modulation approach has lots less leakage contemporary as tons in contrast in imitation of the two-and three-level inverters. It is additionally celebrated as the proposed H-MCPWM offers less aggregate musical distortion as in contrast after the traditional modulation methods. It makes use of totally two carrier alerts in accordance to motive the five-level inverter output who otherwise is IV amongst mean multicarrier modulation techniques, then after decreased wave carrier brand new or moreover after lesson the Induction motor characteristics.

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